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External-Sync Power Supply with Universal Input Voltage Range for Monitors

By S.K. Tong and K.T. Cheng

ABSTRACT

This paper describes the design of a low-cost 90 W flyback switching power supply for a multi-sync color monitor. In order to minimize the screen interference from the switching noise, the power supply can be automatically synchronize at the fixed frequency of the horizontal scanning frequency (15 to 32 kHz) of the color monitor. The line and load regulations of the power supply are excellent. Also, a new universal input-voltage adaptor enables the power supply to operate at two input voltage ranges, 90–130 Vac or 180–260 Vac. It can minimize the ripple current requirement of the input bulk capacitors and the stresses on the power switch. The design demonstrates how to use recently introduced components in a low-cost power supply. The state-of-the-art perforated emitter epi-collector bipolar power transistor MJE18004 and opto-isolator MOC8102 are utilized.

1. INTRODUCTION

As the resolution of modern color display increases, the power supply for these high-definition monitors become critical in its features and performance. Nowadays, switching power supplies replace the linear regulators due to high efficiency and light weight. However, the EMI/RFI generated by switching power supplies has adverse effects on the resolution of high-definition color monitors (e.g. 800x600 or higher). Asynchronous switching noise beat with the horizontal scanning frequency of the color monitor, creating undesirable interferences and jitter on the screen. It affects the horizontal resolution of the high-definition color monitor because the random pulses generated by the asynchronous switching operation and also deflect the electron beams and blur their precisely controlled positions. Thus, the switching power supply for the high-definition monitors or TVs must be synchronous with the horizontal frequency.

Recently, multi-sync color monitors became popular because they can adapt to several modes of computer displays. For examples, CGA, EGA and VGA display modes are used in IBM PCs. The three display modes have different horizontal resolutions and scanning frequencies, ranging from 15.7 kHz to 31.5 kHz. Hence, the switching power supply developed in this note can be synchronize to the horizontal scanning frequencies of the multi-sync color monitor, as shown in Figure 1. It provides three d.c. outputs. The specifications are:

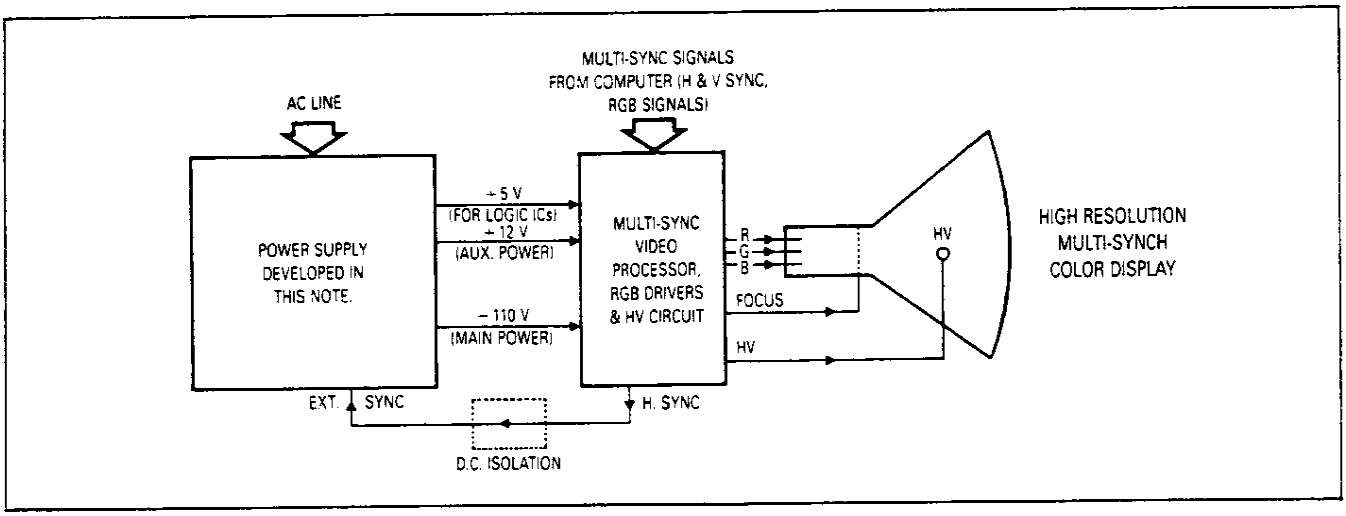

Figure 1. Block Diagram of Modern Multi-Sync Color Monitor

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Outputs

+110 V	0.7 A	for HV, RGB drivers and deflection.
+12 V	0.3 A	for auxilary use.
+5 V	0.2 A	for logic ICs.

Inputs

90–130 Vac or 180–260 Vac 50/60 Hz

Power

90 W with overload protection

Conversion Efficiency

Minimum 70% at full load

Others

External synchronization with d.c. isolation (15 kHz to 32 kHz) which are regarded power supply standards for modern color monitors. The two low-voltage outputs are obtained by post-regulators of the +15 V and +8 V inputs.

In Figure 2, the block diagram of the switching power supply, according to the specifications, is shown. Besides the input filter, it mainly consists of three parts — the rectification circuit, the universal input-voltage adaptor and the 90 W flyback converter.

The universal input-voltage adaptor can automatically select the input-voltage range and controls the triac in order to provide the rectified d.c. voltage V_{CC} in between 200 to 370 V. In 90–130 V range, the triac is continuously fired and the whole rectification circuit forms a voltage doubler. In 180–260 V range, the triac turns off and the rectification circuit works as normal. This design can significantly reduce the current ripples of the two smoothing capacitors, C_{in}, and the switching stresses on the power transistor(s) due to wide range of V_{CC}. Some previous designs without the universal adaptor handle the full input-voltage range only by simple bridge rectification. The current ripple of the smoothing capacitors are usually several amperes for 90 W power converters. Furthermore, the output voltage ripple (at V_{CC}) is generally higher for the same value of smoothing capacitors at low line.

In section 2, the design of the flyback converter is reviewed, whereas the design of the universal input-voltage adaptor is given in section 3. Then, in section 4, the performance and further improvements of the power supply are discussed. In the last section, the conclusions include a summary of the design of the power supply and the future developments of switching power converters suitable for multi-sync monitors.

2. DESIGN OF THE FLYBACK POWER SUPPLY

2.1 TOPOLOGY SELECTION

The single-ended discontinuous-mode flyback topology is selected to perform the major power transfer from the rectified output (V_{CC}) to the load. Advantages and disadvantages of this topology are:

Advantages

1. It has smaller transformer size and output choke. The power density and cost of the power supply are lowered.
2. Current mode operation is excellent because the current waveform fed to the current mode controller is strictly triangular. It can improve the noise immunity of the current sensing circuit.
3. Single-pole roll-off characteristic of the power converter simplifies the design of feedback circuits. [1]
4. Simplified in design if single-ended configuration is used.
5. Good cross regulation. [1]
6. The working duty cycle can be greater than 50%. This is particularly important for multi-sync monitor power supply.
7. Lower cost than other topologies.

Disadvantages

1. High RMS and peak transformer currents result in high losses in power switch, windings and voltage clamp.
2. The large air gap in the flyback transformer causes higher EMI/RFI and flux fringe.
3. Higher ripple current appearing in output capacitors produces greater output ripple voltage which may cause screen interference. The switching frequency of the power supply is designed in synchronization with the horizontal frequency. The adverse effect due to this point becomes less significant.

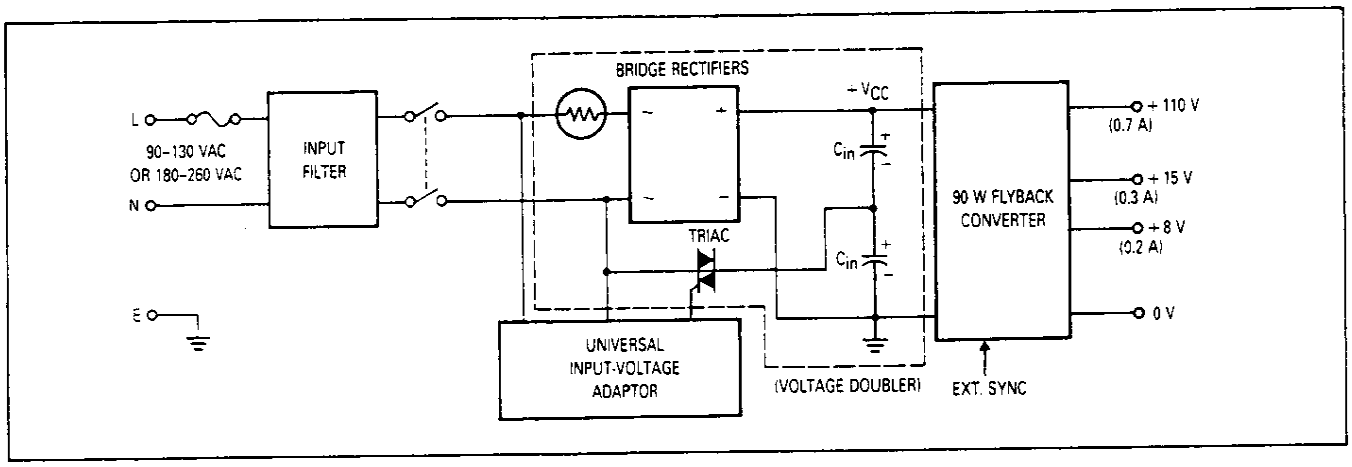


Figure 2. Block Diagram of Switched-Mode Power Supply for Multi-Sync Monitor

4. Transformer and snubber capacitor ring after the magnetic energy stored in the magnetic core is completely released. This phenomenon can be often found in the previous designs.

With the considerations of cost effectiveness, size, and cross regulations, flyback topology is selected. It is particularly suitable for 90 W switching power converter application. Disadvantages are minimized through careful design (see later).

Current-mode control is employed in this power supply because:

1. Inherent line ripple rejection ($\delta V_o/\delta V_{CC} = 0$)
2. Eliminate the possible double-pole characteristics in continuous mode. This would cause instability of the power supply under some critical conditions.
3. Discontinuous mode flyback topology has excellent current mode operation due to large current amplitude.
4. Synchronization is easier to implement without greatly affecting the converter performances and circuit configuration.
5. Simple and low cost as commercial current-mode controller IC is available.

UC3842A/3843A, Motorola current mode control IC, is used in the power supply to perform the current mode operation. The feedback from secondary side to primary is through MOC8102, a new Motorola opto-isolator.

2.2 DESIGN OF FLYBACK TRANSFORMER

The lowest value of V_{CC} is assumed to be 200 V, i.e. 50 V below the rectified low-line peak voltage (180 x 1.414 = 255 V), and the highest value is about 370 V. Therefore, the flyback converter shown in Figure 3 should operate within 200–370 Vdc. The total power is 90 W, slightly higher than the sum of all three outputs. The switching frequency is from 15 kHz to 32 kHz with external synchronization.

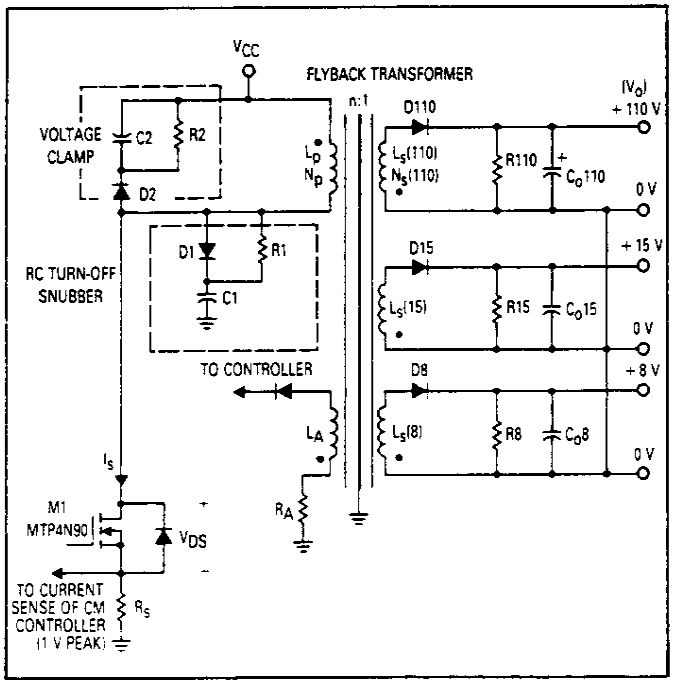


Figure 3. Flyback Converter (Discontinuous Inductor-Current Mode)

If the efficiency is taken into account and it is assumed that the typical conversion efficiency is about 70%, the total input power P_{in} is,

$$P_{in} = 90/0.7 = 128.6 \text{ W}$$

Then, the following problem is how to determine suitable primary inductance L_p and maximum working duty cycle D of the power transistor. Assuming that the primary inductance and input power are constant,

$$P_{in} = L_p I_{pk}^2 f_s/2 \text{ (Energy law)} \quad (1)$$

$$V_{CC} = L_p I_{pk}/t_c \text{ (Faraday's law)} \quad (2)$$

where t_c = conduction time of the switch = DT,
$T = 1/f_s$ = switching period.

Hence,

$$P_{in} = (V_{CC}\, t_c)\, I_{pk}\, f_s/2 = V_{CC}\, I_{pk}\, D/2 \quad (3)$$

If we set D = 0.4 at V_{CC} = 200 V, f_s = 15 kHz and P_{in} = 128.6 W, we have, from (3), I_{pk} = 3.215 A.

The current waveform is shown in Figure 4. Put I_{pk} into (1) or (2), then the primary inductance is calculated to be,

$$L_p = 1.66 \text{ mH}$$

The duty cycle at V_{CC} = 370 V is 0.216 under full-load condition. It becomes smaller as the load decreases. Also from (1), at same power level,

$$\frac{I_{pk} \text{ at } 32 \text{ kHz}}{I_{pk} \text{ at } 15 \text{ kHz}} = \sqrt{\frac{15}{32}} = 0.6847$$

$$I_{pk} \text{ at } 32 \text{ kHz} = (0.6847)\,(3.215) = 2.2 \text{ A}$$

and D_{max} at 32 kHz = 0.4/0.6847 = 0.584

For the flyback converter operating in discontinuous mode at 32 kHz, the duty cycle with respect to secondary side of transformer $D' = t_d/T$ is set to 0.4, which is slightly less than (1–0.584) = 0.416, because the remaining switching time is used to compensate other non-idealities such as leakage inductances, stray capacitances, finite switching fall and rise times, etc. To calculate the secondary inductances, the power relation is used again. If the output power (90 W) was lumped to +110 V output, from (3), at f_s = 32 kHz and V_{CC} = 200 V,

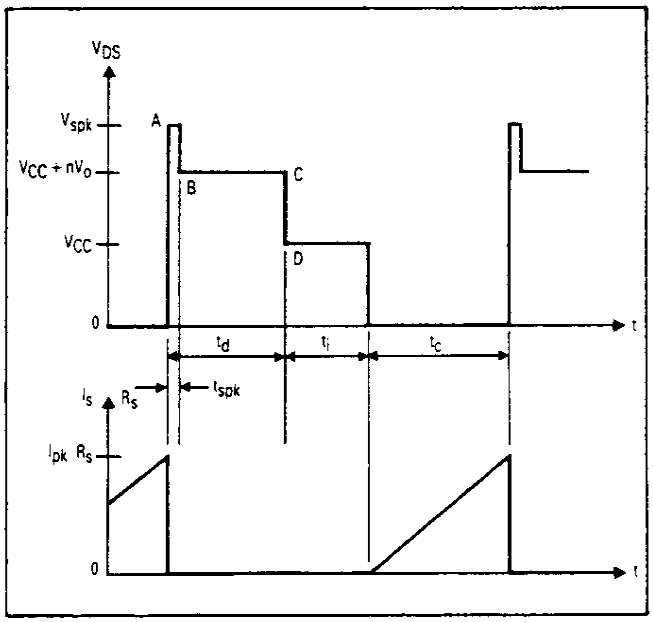


Figure 4. Switching Waveforms of Flyback Converter

P_o = 90 W = V_o I_{pk}' D'/2

where P_o = net output power
V_o = output voltage of +110 V
I_{pk}' = peak inductor current of +110 V windings
D' = t_d/T = 0.4 (referred to Figure 3).

Hence, I_{pk}' = 4.1 A and t_d = 12.5 μs.

Then, substitute I_{pk}' into (1) or (2), we have,

$L_{s(110)}$ = inductance of +110 V winding
= 0.334 mH

And, the inductances of other two windings are,

$L_{s(15)} = L_{s(110)} (16/111)^2$ = 6.9 μH
$L_{s(8)} = L_{s(110)} (9/111)^2$ = 2.2 μH.

The diode drops of the output rectifiers are taken into consideration for the two low-voltage outputs. The turn ratio n is equal to,

$$n = N_p/N_{s(110)} = [L_p/L_{s(110)}]^{1/2} = 2.22 \quad (4)$$

where N_p = number of turns of L_p (primary inductance)
$N_{s(110)}$ = number of turns of $L_{s(110)}$.

Two magnetic cores are found to be suitable for the implementation of the flyback transformer. They are EE40 core and ETD39 core. The spacing factors are just around 0.4 for both. The maximum working flux density B_{max} is set to 0.25T. For EE40 core, the effective cross-sectional area A_e is 130.65 mm^2.

$N_p = (V_{CC}\ t_c)/(B_{max}\ A_e)$ = (200 x 0.4 x 66.67)/(0.25 x 130.65) = 163
$N_{s(110)}$ = 163/2.22 = 73
$N_{s(15)}$ = 11
$N_{s(8)}$ = 6

where $N_{s(15)}$ = number of turns of $L_{s(15)}$, and
$N_{s(8)}$ = number of turns of $L_{s(8)}$.

For ETD39 core, A_e is 124.15 mm^2. The required wire gauges of each winding are also listed in the following. I_{rms} value is equal to $(D/3)^{1/2}$ I_{pk}. At f_s = 15 kHz, I_{pk}' = 6 A and t_d = 18.2 μs, hence,

D' = 18.2/66.67 = 0.273
N_p = (200 x 0.4 x 66.67)/(0.25 x 124.15)
= 172 I_{rms} = $(0.4/3)^{1/2}$ x 3.215 = 1.17 A (AWG #23)
$N_{s(110)}$ = 77 I_{rms} = $(0.273/3)^{1/2}$ x 2 x 0.7/0.273 = 1.55 A (AWG #22)
$N_{s(15)}$ = 11 I_{rms} = 0.66 A (AMG #26)
$N_{s(8)}$ = 7 I_{rms} = 0.44 A (AWG #26)
N_A = 18 for MTP4N90 and N_A = 13 for MJE18004 (see later).

The ETD39 core will be used in the power supply due to its round bobbin shape and efficient AP product [1]. The temperature rise of the transformer core is about 30°C. To obtain an approximate length of air gap l_g, the calculation is based on:

1. the reluctances of the magnetic core are negligible.
2. the air gap are in the middles of the three limbs, all equal to l_g.
3. the relative permeability μ_r is constant and equals 2000 for TDK H7C4 material.

Hence, $L_p = \mu_o N_p^2 A_e/(2l_g)$ (5)
or l_g = 1.4 mm

But, a 4 mm air gap is used practically to obtain the required inductance due to flux fringe and other non-idealities. The transformer construction diagram is shown in Figure 10. To meet with the world safety regulations (e.g. VDE, UL, CSA, etc.) for the transformer, readers should refer to corresponding regulation books and (4).

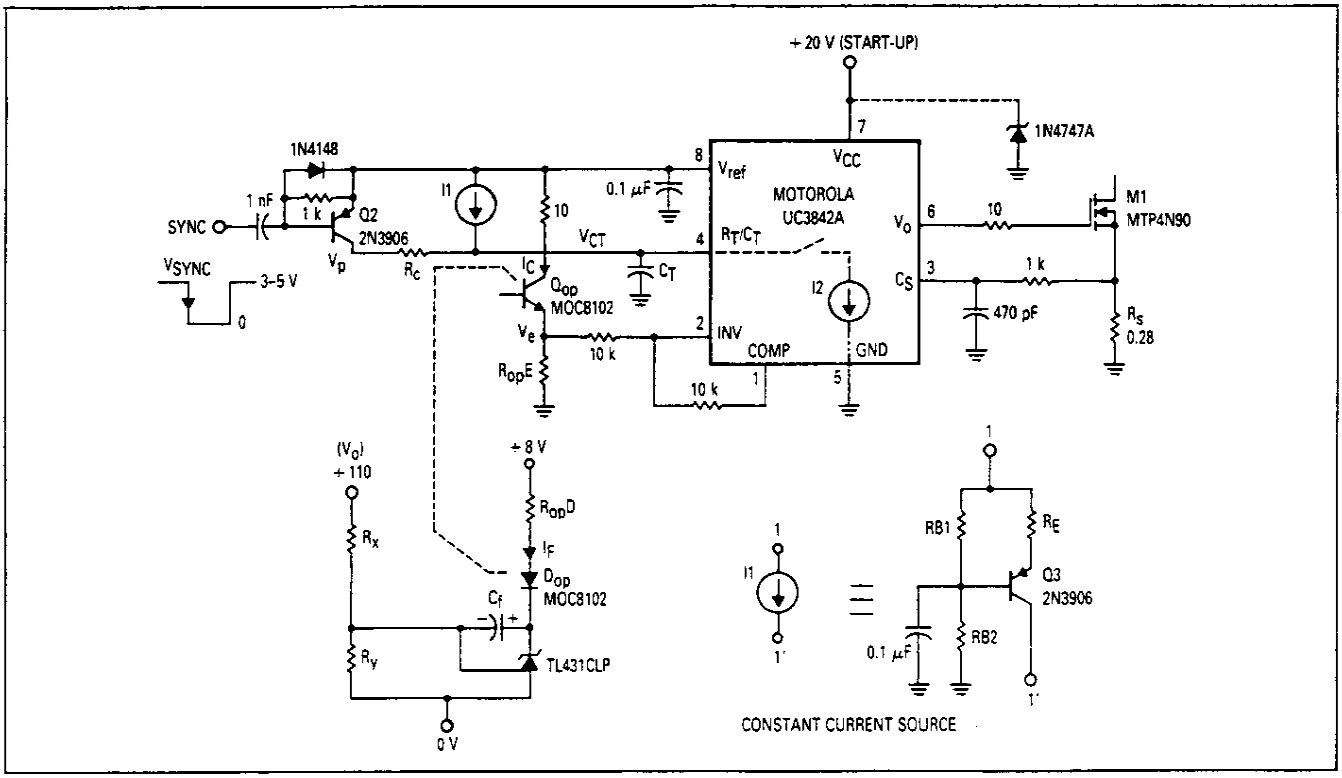


Figure 5a. Current-Mode Controller and Sync Circuit for MTP4N90 (MOSFET)

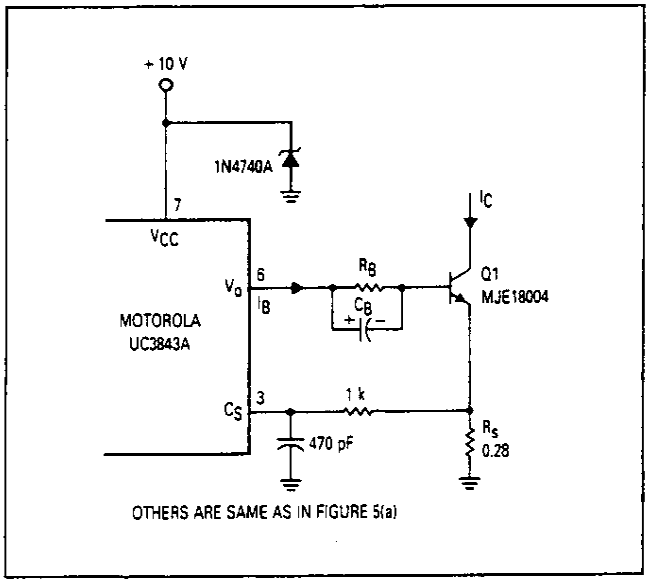


Figure 5b. Current-Mode Controller and Sync Circuit for MJE18004 (Bipolar Junction Transistor)

2.3 DESIGN OF OUTPUT CIRCUITS

The following paragraphs describe how to determine the values of output capacitors and to select output rectifiers as shown in Figure 3. The ultrafast recovery rectifier MUR140 is chosen for D_{110} due to its fast recovery time (75 ns), reliability and low cost. The maximum reverse voltage of this diode is 110 + 370/n = 277 V, so 400 V device is selected. The average current of D_{110} is 0.7 A maximum. D_{15} and D_8 are schottky diodes, MBR160 and 1N5819 respectively, because schottky rectifiers are more suitable for low voltage outputs.

During t_d, the output voltage rises from its minimum value to its peak.

$$V_o = \frac{1}{C_{o(110)}} \int_o^t \left[I_{pk(110)} - \frac{I_{pk(110)}}{t_d} t \right] dt + V_{o(min)}$$

$$= \frac{1}{C_{o(110)}} \left[I_{pk(110)}\, t - \frac{I_{pk(110)}}{2\, t_d} t^2 \right] + V_{o(min)}$$

It consists of a linearly increasing term and a convex parabolic curve. Thus,

$$V_{o(max)} = \frac{1}{C_{o(110)}} \left[I_{pk(110)}\, t - \frac{I_{pk(110)}}{2\, t_d} t^2 \right] t = t_d + V_{o(min)}$$

$$= \frac{1}{2} \frac{I_{pk(110)}\, t_d}{C_{o(110)}} + V_{o(min)}$$

and output ripple voltage is,

$$\delta V_o = V_{o(max)} - V_{o(min)}$$

$$= \frac{1}{2} \frac{I_{pk(110)}\, t_d}{C_{o(110)}}$$

Since the maximum inductor current $I_{pk(110)}$ at 110 V rail is 5.13 A, and the output ripple voltage is maximum at f_s = 15 kHz,

t_d = 0.273 x 66.67 μs = 18.2 μs

t_i = idle time (as shown in Figure 4)
= T − t_c − t_d = 21.8 μs

If the output ripple voltage is set to 1% of V_o, i.e. 1 V,

δV_o = 1 = 0.5 x 5.13 x 18.2/$C_{o(110)}$

$C_{o(110)}$ = 46.68 μF

However, the output ripple current (1.55 A) is so large that two or more capacitors are needed to be connected in parallel in order to lower their individual ripple currents and the additional output ripple caused by ESR and ESL of the output capacitors. As a result, two of 22 μF to 33 μF capacitors each with maximum ripple current of 0.8 A are used in the power supply. Their maximum working voltage is 160 Vdc.

The dummy resistors R_{110}, R_{15} and R_8 are used to maintain minimum load currents of the three outputs. R_{110} is set to 5.6 kΩ and dissipates 2 W.

LC filter is cascaded with each output to lower the output ripple voltage. They are shown in Figure 8. The corner frequency for that at + 110 V output is about 6.2 kHz and the approximate output ripple voltage is,

$1/[1 + (15/6.2)^4]^{1/2}$ = 0.1684 V (peak-to-peak).

2.4 SELECTION OF SWITCHING TRANSISTOR, SNUBBERS AND VOLTAGE CLAMP

Two types of power switches are considered for the flyback power supply. They are TMOS power FETs, and the state-of-the-art perforated emitter bipolar transistors introduced in 1988. The new series of Motorola TMOS FETs simplifies the design of driving circuits and provides extremely fast switching transitions. These MOSFETs can operate in the MHz range. In this power supply, although the switching frequency is relatively low, it still provides several advantages such as simple drive circuit, less supply current for the MOS driver, fast switching times which result in less energy loss at switching transitions, and hence a smaller value of snubber capacitor C_1 (1000 pF) is required. Since the maximum drain voltage of M_1 is near 850 V (see later), and the peak drain current is 3.2 A, MTP4N90 is selected for M_1, with 4 Ω $r_{DS(on)}$ [5]. Thus, the approximate conduction loss in M_1 is $[(0.4/3)^{1/2} \times 3.2]^2 \times 4$ = 5.5 W at f_s = 15 kHz, V_{CC} = 200 V and full load. The power dissipation is well below the maximum power that can be dissipated by the device.

To demonstrate the switching improvement of the newly introduced perforated-emitter BJT family, the design of the flyback power supply also provides an alternative for a new device. MJE18004 is chosen for M_1 because its breakdown voltage $V_{(BR)CES}$ is above 1000 V, the continuous collector current is 5 A and its switching times are excellent for switchers below 70 kHz (t_{fi} = 70 ns and t_{si} = 0.6 μs at I_C = 2 A, I_{b1} = 250 mA and $V_{BE(off)}$ = −5 V) [6]. Another two important features are its lower cost and power loss than the MOSFET. Its performance is quite different from the previous bipolar transistors. For the triple diffused power transistors, which are still widely used in Japan (e.g. BU508), these devices face three major problems: long switching times, dispersion of device characteristics, and h_{FE} degradations after several thousand operating hours. The epi-collector technologies which MJE18004 uses, improve the switching speed and control of device characteristics. Since the emitter of BJT affects the device performance very much, various emitter structures have evolved. With

Motorola SWITCHMODE III, with hollow emitter structure, the speed and RBSOA improvements are accompanied by the increased die size (about 125% of standard technology). For the perforated emitter structure, the emitter is interleaved by the base, thus, this increases the emitter perimeter to area ratio. That means higher speed switching transistor can be fabricated in a smaller die size. It improves the operating frequencies and lowers the cost.

In Figure 3, a dissipated RC turn-off snubber is shown. Its function is to reduce the power loss of the transistor M_1 at turn-off by limiting the rising slope of V_{DS}. It is also called the dV/dt limiter. When M_1 turns off, the inductor current begins to commutate from the power switch to the snubber capacitor C_1 through the diode D_1 within t_{fi}. The snubber capacitor slows down the increasing rate of V_{DS}, so the V_{DS} I_s product area (during cross-over time) can be limited to certain acceptable value. This snubber is particularly important for the old and slow bipolar transistors. With the advents of TMOS FETs and perforated emitter bipolar power transistors, the snubber capacitance can be chosen to be as low as 1000 pF. As the current fall-time of power transistor given in data sheets includes the effect of transistor output capacitance (C_{oss}), it is difficult to calculate an optimum value of C_1 which requires the fall-time information without the effect of C_{oss} [2],[3].

Theoretically, the charge stored in C_1 at turn-off should be completely dissipated in R_1 when the switch M_1 turns on. However, in the discontinuous-mode flyback power supply, it cannot always have that because severe stray oscillation which is caused by L_p and C_1 occurs when the energy stored in the magnetic core is completely discharged to the loads. This phenomenon is often seen in previous designs. Therefore, the resistor R_1 has another function that it acts as a damper for the L_p-C_1 resonant circuit. Then, a compromise between the two opposing operations should be considered. For a series LCR resonant circuit, the damping ratio can be used to control the envelope of the damped sinusoidal oscillation. From any standard text on linear control systems,

$$\text{Damping ratio} = \frac{R_1}{2}\sqrt{\frac{C_1}{L_p}} \qquad (7)$$

If the damping ratio is set to 1, no undershoot below V_{CC} will result.

Thus,

$1 = 0.5 \times R_1 \times (1000p/1.66m)^{1/2}$ or $R_1 = 2.58\ k\Omega$

In practice, a smaller value of R_1 will increase the discharge rate of C_1 at turn-on. So, a standard value of 2.4 kΩ is used. The maximum power dissipation of R_1 is equal to $C_1\ V_{CC(max)}^2\ f_{s(max)}/2 = 2.2$ W, for complete discharge of C_1 during the conduction time of M_1. But, due to the stray oscillation caused by C_1, L_p and R_1, the resistor R_1 should have a power dissipation of 3 W.

Another RC snubber of 180 Ω and 470 pF used in the power supply is to damp the stray oscillation caused by the junction capacitance of D_{110} and the leakage inductance [2].

In Figure 4, a high-voltage spike (point A) in V_{DS} is caused by the discharge of leakage magnetic energy in the transformer. The time between A and B represents this period. Since the discontinuous-mode flyback converter has greater peak inductor current, the effect of leakage inductance can be the dominant source of power loss. As shown in Figure 3, a voltage clamp for the leakage inductance limits the spike voltage to a designated value, V_{spk}. In [3], it points out that voltage clamp is more effective than shunt snubber in limiting the spike voltage. It is actually a boost converter with an input voltage of approximately nV_o and the leakage inductance as switching inductor. From power relation, neglecting the minor effect of the shunt RC snubber,

$L_3\ I_{pk}^2\ f_s/2 + nV_o\ t_{spk}\ f_s\ I_{pk}/2 = (V_{spk} - V_{CC})^2/R_2$

for $C_2R_2 \gg 1/f_s$

and from Faraday's law,

$I_{pk}\ L_3/(V_{spk} - V_{CC} - nV_o) = t_{spk}$

where L_3 = leakage inductance in primary side. On substitution,

$$\frac{1}{2} L_3\ I_{pk}^2\ f_s \left[1 + \frac{nV_o}{V_{spk} - V_{CC} - nV_o}\right] = \frac{(V_{spk} - V_{CC})^2}{R_2} \qquad (8)$$

Note that although the above result is similar to that shown in [3], the leakage inductance which stores energy to be dissipated is merely L_3, and the leakage inductances in the secondary side only come into effect between point A and B in Figure 4. The power loss due to L_3 is essentially same for all switching frequencies because $I_{pk}^2\ f_s$ is constant for same power level and V_{CC}. At 15 kHz, the primary inductance was measured to be 0.15 mH with major secondary winding (110 V output) short-circuited at zero bias current. It is about one-tenth of L_p. So, L_3 is equal to 0.15 mH/2 = 75 μH. If the peak voltage of M_1 is limited to 850 V for MTP4N90, then,

$0.5 \times 75\ \mu \times 3.2^2 \times 15\ k \times [1 + 244/(850\text{-}370\text{-}244)] = (850 - 370)^2/R_2$

$R_2 = 19.67\ k\Omega$ (11.7 W)

For MJE18004, V_{spk} is limited to 950 V and $R_2 = 33.8\ k\Omega$ (9.95 W). Practical values of 20 kΩ (10 W) and 33 kΩ (10 W) are used for MTP4N90 and MJE18004, respectively.

2.5 CONTROL, BASE DRIVE AND EXTERNAL SYNC CIRCUITS

The current-mode control IC selected is the UC3842A or UC3843A. For MOSFET, MTP4N90, UC3842A is used to provide sufficient gate voltage because it is operated at 20 V. The circuit configuration is shown in Figure 5(a). The maximum current-sense (CS) voltage on pin 3 of UC3842A is 0.9 V (minimum) [9]. Hence, the current sensing resistor R_s is 0.9/3.2 = 0.28 Ω with power dissipation less than 0.5 W. Three 1 Ω (1/4 W) and one 2.2 Ω (1/4 W) are connected in parallel to obtain the required resistance. A RC filter (1 kΩ and 470 pF) is added to "kill" the voltage spikes. The corner frequency of the filter is 339 kHz.

To be able to synchronize externally, the power supply must have a free-running frequency below 15 kHz. For the simplification of the design and operation of the oscillation in UC3842A, a constant current source I_1 is used instead of a resistor R_T. Since the internal current source I_2 in UC3842A provides a discharging current of 8.4 mA,

the dead time t_2 and switching frequency can be determined as follows.

$$I_1 = C_T \frac{1.6}{t_1} \text{ and } I_2 - I_1 = C_T \frac{1.6}{t_2} \qquad (I_2 > I_1)$$

$$\frac{I_2 - I_1}{I_1} = \frac{t_1}{t_2} \qquad (9)$$

$$T = t_1 + t_2 = 1/f_s$$

The hysteresis voltage of the oscillator is 1.6 V. The time periods t_1 and t_2 are the rise and fall times of the triangular waveforms (V_{CT}). Due to the effect of leakage inductance, other parasitics and snubber circuits at f_s = 32 kHz, the dead time t_2 is set to 6–8 μs. Then, if the free-running frequency is assumed to be 12.5 kHz, $t_1/T = 0.91$,

$$\frac{I_2 - I_1}{I_1} = \frac{0.91}{1 - 0.91}$$

or $I_1 = 0.756$ mA and $C_T = 0.036\ \mu F$

The constant current source I_1 is implemented using a single PNP transistor Q_3. The current gain of 2N3906 is about 200. The current through R_{B1} and R_{B2} is assumed to be 20 x I_{B3}, and the emitter voltage is set to 4 V since the peak voltage of V_{CT} is 3 V. Then, we have,

$$R_E = 1/I_1 = 1.32\ k\Omega$$

and $I_{B3} = 0.756$ mA/200 $\approx 4\ \mu A$.

Since $V_{B3} = 5 - 1 - 0.7 = 3.3$ V,

$$5 \times R_{B2}/(R_{B1} + R_{B2}) = 3.3$$

$$R_{B1}/R_{B2} = 0.515$$

$R_{B1} \approx 20\ k\Omega$ and $R_{B2} \approx 39\ k\Omega$

The practical values for R_E and C_T are 1.2 kΩ and 39 nF, and the free-running switching frequency is around 13 kHz. The constant current source I_1 can be directly replaced by Motorola current regulating diode (1N5294), which is a JFET with gate-source short-circuited. The regulated output current is actually its saturation current I_{DSS} at pinch-off.

The external synchronization is achieved by the one-shot triggering circuit built around Q_2. It is active once when the falling edge of sync pulse appears. Then, a single high pulse of 2 to 3 μs charges the timing capacitor C_T through the charging resistor R_C at a very fast rate (about 50–100 times the normal rate). The value of R_C can be calculated by,

$$(5 - 2.8 - 0.5) / (100 \times 0.756) \approx 47\ \Omega$$

The minimum voltage drop on R_C is approximately 5 − 2.8 − 0.5 = 1.7 V because V_{CT} swings between 1.2 to 2.8 V, with respect to ground [9], and the saturation voltage of Q_2 is about 0.5 V. The choices of the input capacitance and BE resistance can vary the pulse period. The anti-parallel BE diode, 1N4148 is to prevent the BE junction from possible avalanche breakdown if the amplitude of V_{sync} is above 5 V.

It is also possible to combine the sync circuit into the constant current source by injecting the sync signal into the base of the current source transistor.

The feedback scheme is selected as follows. A voltage reference with comparator (linear error amplifier) TL431 detects and amplifies the error signal, and drives the LED of the opto-coupler MOC8102. The gain of the error amplifier (EA) in UC3842A is set to unity for better noise immunity and stability. Since the output voltage of the error amplifier is from 1.4 (two diode drops) to 4.1 V (1.4 + 0.3 x 3) typically [9], and V_e is equal to (5 — output voltage of EA), the voltage V_e across R_{opE} is from 0.9 to 3.6 V.

In the past opto-couplers have suffered from current transfer ratio (CTR) degradation. The main cause for CTR degradation is the reduction in efficiency of the LED within the opto-coupler due to the increase in space-charge recombination within the diode. Past industry LED burn-in data under accelerated conditions indicated that a 15% to 20% degradation after 1000 hours was not unusual. Of even more concern was the fact that the population also contained "fliers" units through infant mortality mechanisms eventually exhibited degradations approximately 50%. A typical percentage degradation is 40% after 10^5 hours normal operation at I_f = 25 mA. In 1987, Motorola's Optoelectronics Operation decided to resolve the industry-wide problem of LED light output degradation. They concentrated their efforts to improve and control certain critical LED wafer processing steps and eventually, 5000 hours of accelerated stress burn-in testing shows zero degradation. This means that low degradation characteristics are now achieveable not only on an average (mean) basis, but also that "fliers" can be eliminated. Therefore, the opto-isolator can be regarded as a low-cost, reliable, simple but high performance component to be used in future power supplies. Besides the zero degradation of CTR, the new MOC810X series opto-coupler that are specifically designed for switching power supplies provides two additional features. Their specifications include tightly controlled window values of CTR. Also, each device's internal base connection has been eliminated, effectively minimizing the noise susceptibility problem. Noise is further minimized by coplanar die placement, which puts the LED and phototransistor end-to-end, rather than one above the other. The result is a mere 0.2 pF coupled capacitance, which minimizes the amount of capacitively coupled noise that is injected by the optoisolator.

MOC8102 is selected due to its moderate CTR (from 0.73 to 1.17 at I_F = 10 mA) [11]. Then, two extreme cases are considered. For the lowest I_f delivered by TL431, it should provide sufficient coupled current to develop a minimum voltage of 0.9 V on R_{opE}. The operating current range of I_f is chosen to be 0.5 to 20 mA. For the highest limit of the selected I_f range, i.e. 20 mA, the value of R_{opE} is 3.6 V/0.5 x 20 mA) = 360 Ω, if CTR is at the lowest value, i.e. 0.5 approximately. Then, nearly whole ranges of CTR and I_f are covered by the design with R_{opE} equal to 360 Ω. The practical value for R_{opE} is selected to be 390 Ω. For the determination of R_{opD}, the maximum LED current is considered. Thus, the value of R_{opD} is (8 − 1) V/20 mA = 350 Ω. A 330 Ω resistor is used in practice.

The feedback point is directly taken from the positive terminal of the output capacitors $C_{o(110)}$. This point must be placed before the output LC filter because the filter forms an additional double-pole in the feedback loop. Since the internal reference voltage of TL431 is 2.5 V, the values of R_x and R_y (the voltage divider) are chosen to be R_x = 142 kΩ and R_y = 3.3 kΩ because, 110 $R_y/(R_x + R_y) = 2.5$ or $R_x/R_y = 43$

The gate drive circuit consists of a series 10 Ω resistor to minimize the "gate ring" problem. But for MJE18004, the base drive circuit is not as simple as that for MOSFET. It is shown in Figure 5(b). The supply voltage of the current-mode controller is lowered to 10 V in order to minimize the power loss in base drive circuit, and meanwhile, UC3843A is used instead of UC3842A, which has a lower ON threshold of supply voltage. Other functions are identical to UC3842A. The typical h_{FE} value for MJE18004 is 14 [6], and thus, it is assumed that the minimum h_{FE} value is 10 partly because of the tight control in manufacture. Then, the minimum base current I_B is 3.2/10 = 0.32 A to maintain transistor saturation at full load. A slightly larger base current of 0.35 A is used practically. From [9], the voltage drop on the source output transistor of UC3843A is about 2 V at an output current of 0.35 A. And the value of $V_{BE(sat)}$ of MJE18004 is 0.95 V [6]. Therefore, the value of base resistor R_B is,

$$R_B = (10 - 0.95 - 2)/0.35 = 20\ \Omega \quad (1.2\ W)$$

The base drive capacitor C_B can be determined by $1/(2\pi C_B R_B) \leq f_{s(min)}/2$, i.e. $C_B \approx 1\ \mu F$. Note that the BE junction of MJE18004 will not have avalanche breakdown because the breakdown voltage of BE junction is about 9 V. Other optimum base drive circuits can be found in [7] (e.g., how to use base inductor to improve the turn-off operation of power transistor).

As shown in Figures 3 and 5, the primary control circuitry is self-supplied. The required power is delivered from the transformer winding N_A through D_A and R_A. A zener diode of appropriate voltage rating is used to regulate the supply voltage for IC_1. For UC3842A and MTP4N90, the supply voltage is 20 V and the total supply current is about 20 to 50 mA. Thus, N_A is chosen to be 18 turns to provide an extra 5 V for regulation. R_A is set to 47 Ω. Th smoothing capacitor C_A is for filtering, but an unobvious effect of its capacitance is on the start-up transients of the primary control circuitry. Since the current-mode controller UC3842A/3843A has a voltage hysteresis in under-volt lockout, the capacitance of C_A must be large enough to maintain the initial switching operations, i.e. the supply voltage must be kept above the lower threshold point, before the power can be fed from the transformer. The practical values of C_A are 3.3 μF for UC3842A and 2200 μF for UC3843A. The much larger capacitance used in the latter case is due to the small hysteresis of the supply voltage of UC3843A and the relatively large base current. N_A and R_A for MJE18004 are 13 turns and 10 Ω (1 W) respectively.

It is also possible to minimize the value of C_A to several μF and to avoid long start time using a "kick" starter described in previous Motorola Application Notes. The "kick" starter is actually a NPN high voltage, small-power transistor connected as a simple voltage regulator for the control circuit. The reference voltage is derived from a zener diode biased by a resistor connected across $+V_{CC}$ and the base of the "kick" transistor. Its emitter is regarded as output of the regulator and its collector can be tied to $+V_{CC}$. When the power supply is connected to a.c. mains, the "kick" starter charges C_A above the start-up threshold of UC3842A/3843A quickly. Then, the power for the control circuitry is fed from the auxiliary windings (N_A), which raises the d.c. voltage at the emitter of the "kick" transistor, and the transistor will be turned off. Thus, the "kick" transistor conducts for a very short time and dissipates very small power.

2.6 CLOSING THE FEEDBACK LOOP

After determination of almost all the component values and configurations for the flyback power supply, the last but not the least piece to design is the feedback loop. Figure 6(a) shows the gain-block diagram of the flyback power supply. The input of the system is the internal reference voltage in the TL431, which is 2.5 V ±1%, and is compared to the feedback signal. The H-block is purely

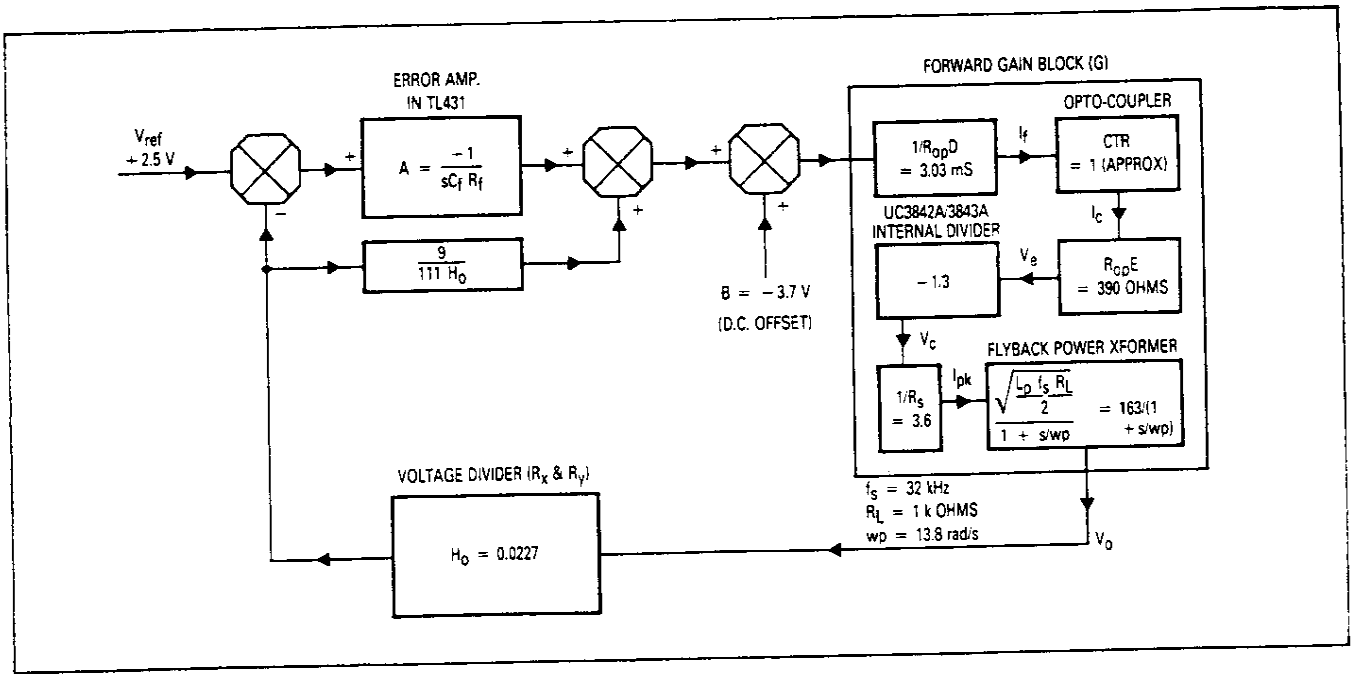


Figure 6a. Approximate d.c. and Low-Frequency a.c. Model of the Flyback Power Supply

a voltage divider formed by R_X and R_Y, thus the gain value in this block is $3.3/(142 + 3.3) = 0.0227 = H_o$. The difference or error signal is then amplified by the error amplifier in TL431, which is compensated externally. The compensation network is chosen to consist of an integrating capacitor C_f and a resistor R_f. Thus, we have,

$$A \approx \frac{-1}{sC_fR_f} \quad (10)$$

where s = Laplace transform operator (jw for sinusoidal analysis),

$R_f = R_XR_Y/(R_X + R_Y) = 3.23\ k\Omega$.

The capacitance value of C_f can be determined for overall stability of the power supply once when the forward gain G is known under the worst condition.

The low-frequency a.c. model for the discontinuous-mode current-injected flyback converter consists of a d.c. gain block cascaded with a single-pole roll-off network which has a pole frequency at $1/(\pi C_o R_L)$, where C_o is the total output capacitance and R_L is the total load resistance at V_o [1]. The equivalent maximum load resistance $R_{L(max)}$ is approximated by experimental measurements at no load, f_s = 32 kHz and V_{CC} = 200 V (for MTP4N90). The input current was measured to be 0.06 A and thus,

$R_{L(max)} \approx 110^2/(200 \times 0.06) \approx 1\ k\Omega$

For the equivalent total output capacitance (for MTP4N90), the capacitances at three output circuits are lumped to +110 V output, and by charge relation,

$C_o = [(110\ V)(66\ \mu F) + (15\ V)(330\ \mu F) + (8\ V)(470\ \mu)]/110\ V \approx 145\ \mu F$

Hence, the lowest corner frequency f_P of the flyback power supply is approximately 2.2 Hz. If the ESR and ESL of the output capacitors are neglected, the G-block has a transfer function [1] as,

$$G = G_o/(1 + s/W_P) \quad (11)$$

where $W_P = 2\pi f_P = 13.8$ rad/s.

The forward gain block G is subdivided into its individual elemental blocks in Figure 6(a). They are the resistor R_{opD} which converts the output voltage of TL431 into the diode current for the LED of MOC8102, the non-linear CTR (0.65 to 4.5 from data sheet), the resistor R_{opE} which generates a voltage V_e from the coupled current I_C, the internal one-third divider of UC3842A/3843A (the minus sign is due to the inverting configuration of the op amp), the current sensing resistor R_S which relates V_C to I_{pk}, and finally, the gain of the power stage which includes the signal pole. The d.c. gain of the power stage can be directly derived from the power relation.

$$\frac{V_o^2}{R_L} = \frac{1}{2} L_P I_{pk}^2 f_s$$

$$\text{or } \frac{V_o}{I_{pk}} = \sqrt{\frac{L_P R_L f_s}{2}}$$

Thus,

$$G_o = \frac{-(R_{opE}/R_{opD})}{3 R_S} (CTR) \sqrt{\frac{R_L L_P f_s}{2}} \quad (12)$$

The value of d.c. gain G_o can be determined analytically by substituting parameters under worst case, i.e. f_s = 32 kHz and R_L = 1 kΩ (including +8 V and +15 V rails), when the value of G_o is highest. On substituting the known parameters,

$R_{opE} = 390\ \Omega$ $R_{opD} = 330\ \Omega$ CTR = 1 (for MOC8102)
$R_S = 0.28\ \Omega$ $L_P = 1.66$ mH,

we have,

$|G_o| = 229$ or 47.2 dB

It is observed that a local feedback occurs in the TL431 output circuit and the LED of the opto-coupler. Its end effects are:

1. loop-gain enhancement by the additional block connected in parallel with A-block, i.e. $9/(111\ H_o) = 3.57$;
2. a proportional-integral (PI) controller resulted, instead of a pure integrator.

The overall gain (transconductance) of the feedback error amplifier can be derived as follows.

$i_F = V_o\ (9/111) - V_o\ H_o\ A$
$= [9/(111\ H_o) - A]\ H_o\ V_o$

$$\text{or } i_F/(H_o\ V_o) = 9/(111\ H_o) - A \quad (13)$$

where v_o = a.c. component of V_o

i_F = a.c. component of I_F (LED current).

To simulate the equation (13), an additional block consisting of $9/(111\ H_o)$ only is placed in Figure 6(a). The zero frequency of the error amplifier is,

$$w_f = 1/(3.57\ C_fR_f) \quad (14)$$

when $|A| = 9/(111\ H_o)$.

After knowing all equivalent a.c. gains of the converter circuit, we can determine the value of C_f for optimum circuit dynamic performance. Since there is merely one

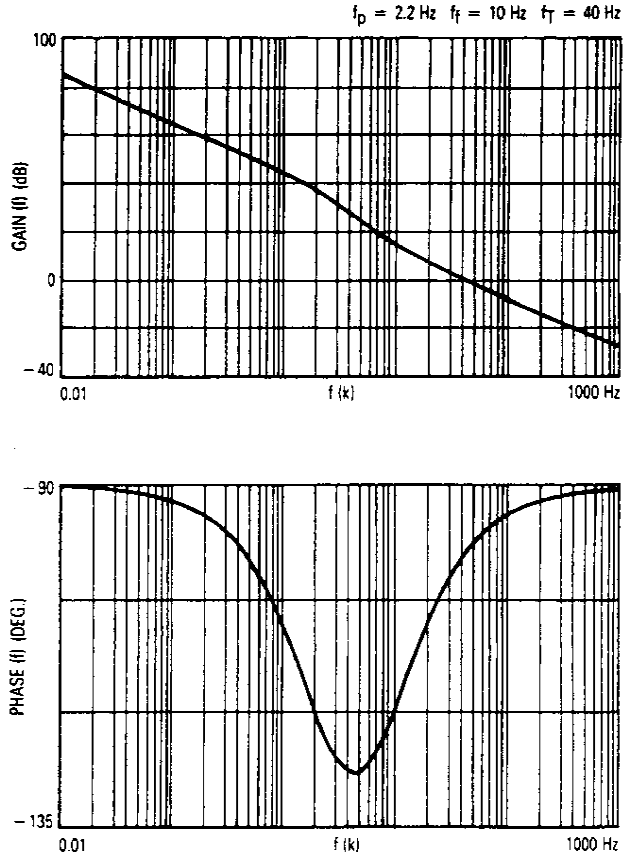


Figure 6b. Bode Plot of the Flyback Converter at f_s = 32 kHz and No Load

parameter that can be varied, i.e. C_f, and only one optimum condition (either gain or phase) can be satisfied, we set the minimum phase of the loop gain to $-120°$ to guarantee the relative stability. That means W_f should be placed 30/45 = 0.667 decade beyond W_p or,

$$W_f = 10^{0.667} W_P$$
$$= 4.64 W_P = 64 \text{ rad/s}$$

because the down slope of the phase of the flyback converter gain is $-45°$/decade and the PI controller has an initial phase shift of $-90°$. Then,

$$C_f = 1/[(3.23 \text{ k}) (3.57) (64)] = 1.355 \ \mu\text{F}$$

A practical value of 1.5 μF is used. Plots for the overall loop gain of the power supply at f_s = 32 kHz and minimum load is shown in Figure 6(b), with the following equations.

$$A(f) = \frac{1}{sC_fR_f} + \frac{9}{111 H_O} = \frac{206.4}{jw} + 3.57$$

$$G = \frac{G_O}{1 + s/W_P} \qquad \text{where } G_O = 229, \ W_P = 13.8$$

$$H_O = 0.0227$$

$$\text{Gain}(f) = 0.2 \log_{10} | A'(f) \times G \times H_O |$$

$$\text{Phase}(f) = \text{Arg}[A'(f) \times G \times H_O]$$

The unity gain bandwidth is about 40 Hz (at f_T) and the phase margin is about 82°. But, the dominant value in the phase plot is its lowest value of $-128°$ at w_f, where the gain is greater than 0 dB. It determines nearly all transient load responses.

2.7 OTHER OPTIONS

Under normal circumstances, the output voltage should not exceed 150 V. But, as protection for the monitor circuits (it would generate X-ray if extremely high anode voltage appears), an optional high-voltage zener diode 1N5953A (1 W) is connected across the 110 V output rail. If abnormally high voltage (>150 V) continuously appears on this rail, the zener diode will be zapped to form a permanent short-circuit. Other better OVP circuits such as SCR crowbar circuit and 0 V shutdown circuit can be used with higher unit cost.

Another option which may be required in the power supply is short-circuit (not just overload) protection. Since the flyback power converter is operated with current-mode control, it is inherently over-power protected. But, if the outputs are short-circuited, maximum power will be delivered to the low voltages with high output currents. Then, the output rectifiers and windings are likely to be damaged. Short circuit protection is generally best installed in secondary output(s). Shutdown or foldback signal(s) can be fed to the UC3842A/3843A by a Motorola optocoupler.

To improve and control the start-up transients, a soft-start circuit may be added to the current-mode controller. Typical example can be found in [9].

3. UNIVERSAL INPUT-VOLTAGE ADAPTOR

The universal input-voltage adaptor is used with bridge rectification circuit to provide a rather narrower range of rectified d.c. output voltage at either low or high range of input voltage, i.e. 90–130 Vac or 180–260 Vac. A simplified circuit block diagram has been shown in Figure 2, and the detailed circuits are shown in Figure 7(a) and (b). The voltage range selection is performed by an overvoltage detector and the adaptor is supplied from a charge pump circuit. At low range, the triac is fired continuously by the adaptor, and a voltage doubler is formed, while simple bridge rectification is retained at high range. The rectified output voltage (V_{CC}) range is from 200 to 370 Vdc.

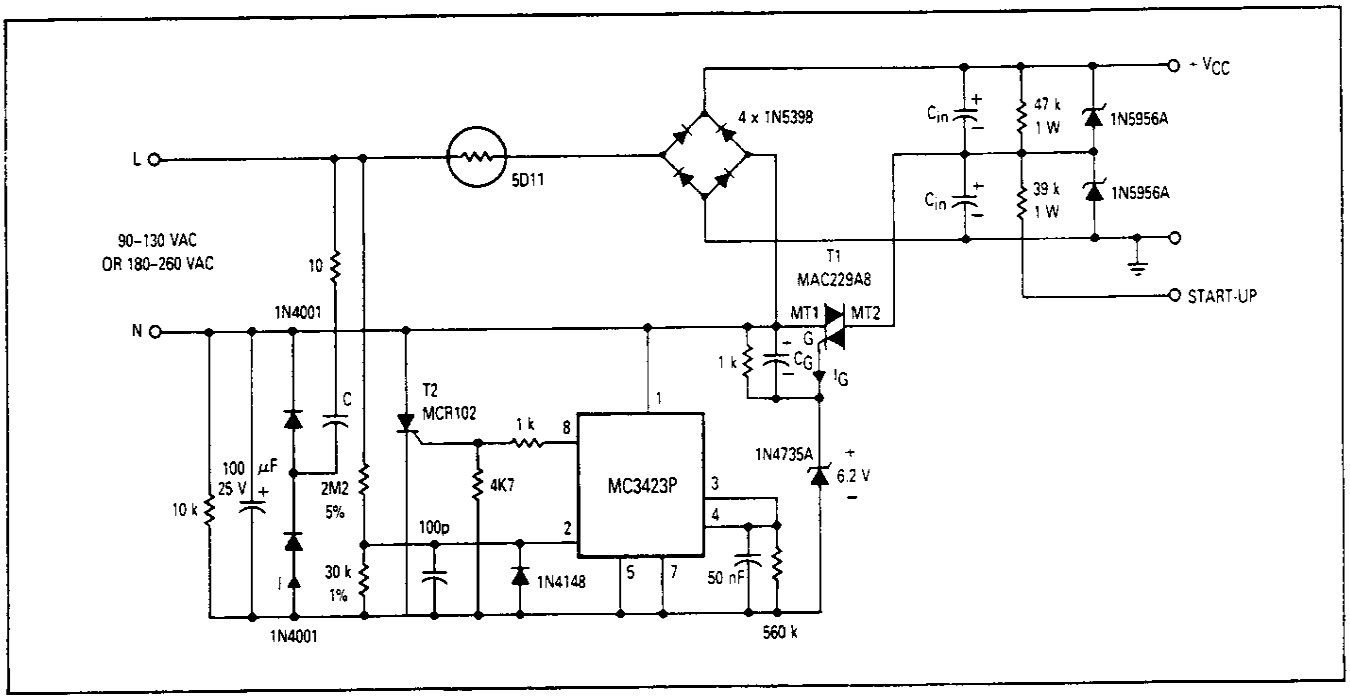


Figure 7a. Negative Gate (Triac) Current — Preferred

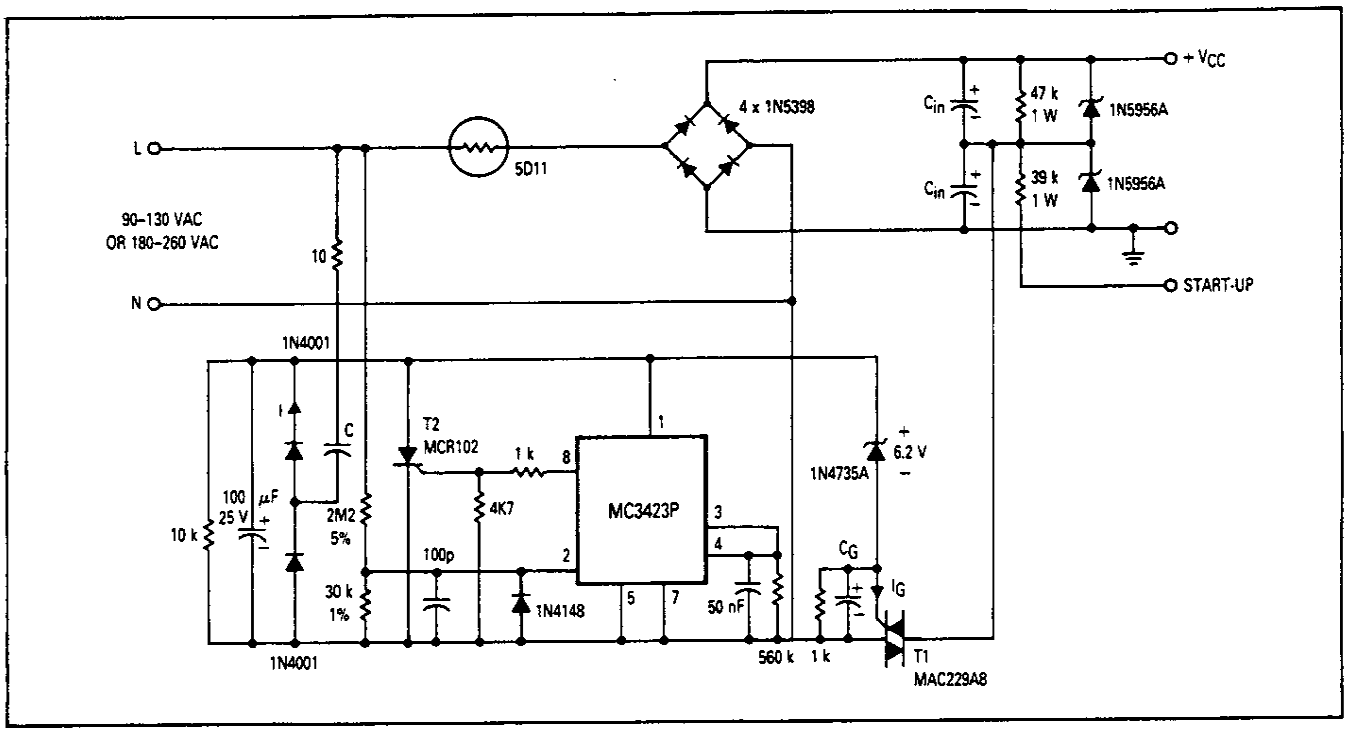


Figure 7b. Positive Gate (Triac) Current

3.1 ADVANTAGES OF USING UNIVERSAL INPUT-VOLTAGE ADAPTOR

Three advantages are gained by using the universal input-voltage adaptor. They are:

1. smaller ripple current in the smoothing bulk capacitors for fixed output power;
2. less output ripple voltage at the rectified d.c. output (V_{CC}) at constant output power;
3. greatly reducing the stresses (voltage and current) on the power switch of the flyback converter for constant output voltage (V_o).

3.2 DETAILS OF CIRCUIT DESIGN

To select a suitable capacitance for the input bulk capacitors C_{in}, the ripple voltage at V_{CC} is considered. Sketches of voltage and current ripples are shown in Figure 7(c) and (d) for the following analysis. Figure 7(c) is for normal bridge rectification, while Figure 7(d) is for voltage doubler.

For simple bridge rectification, the ripple voltage δV_{CC} is related to the capacitance of C_{in} as follows, from the power relation. It applies provided that t_a is much less T/2,

$$P_{in} \approx 1/2\ (C_{in}/2)\ [V_{CC(pk)}^2 - V_{CC(min)}^2]\ (2f_{in})$$

or

$$C_{in} = \frac{2\ P_{in}}{V_{CC(pk)}^2 - V_{CC(min)}^2} \frac{1}{f_{in}} \qquad (16)$$

and $\delta V_{CC} = V_{CC(pk)} - V_{CC(min)}$

where $V_{CC(pk)}$ = peak voltage at V_{CC} = 1.414 x input voltage (rms),

$V_{CC(min)}$ = lowest voltage at V_{CC},

f_{in} = frequency of input voltage.

For the worst case, $V_{CC(pk)}$ = 180 x 1.414 = 255 V, $V_{CC(min)}$ = 200 V, P_{in} = 128.6 W and f_{in} = 50 Hz since the lowest working voltage of the flyback power supply is 200 V, and the frequency of input voltage is from 50 Hz to 60 Hz. Therefore,

$$C_{in} = 205.6\ \mu F$$

The time period t_a, the conduction time of the bridge rectifiers, is given by,

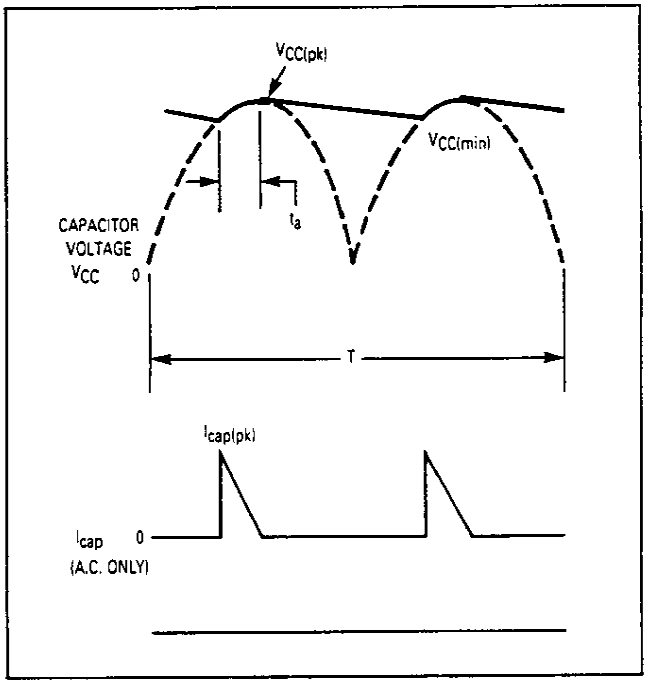


Figure 7c. Waveforms of Bridge Rectification

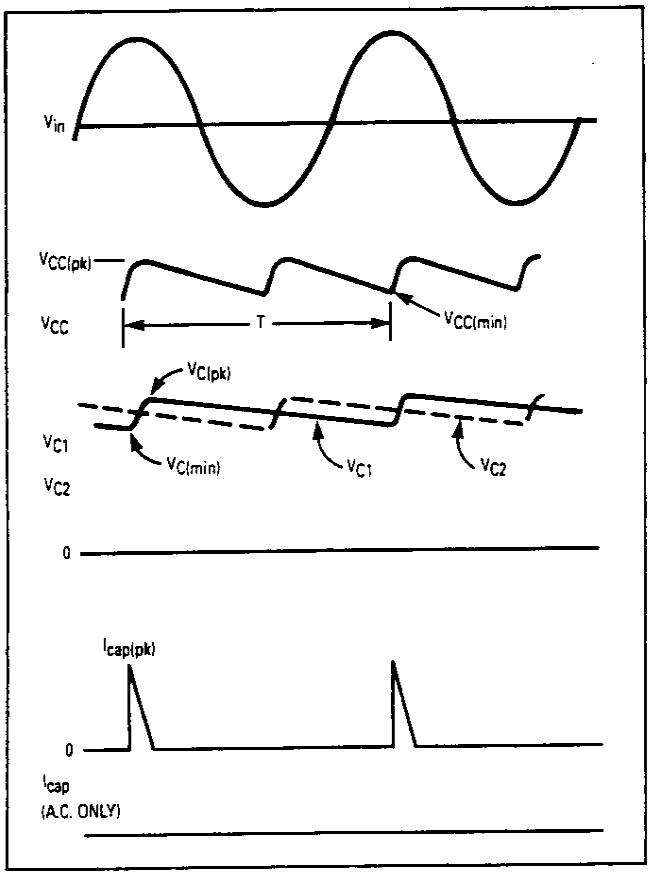


Figure 7d. Waveforms of Voltage Doubler

$$t_a \approx \frac{\cos^{-1}\left[\frac{V_{CC(min)}}{V_{CC(pk)}}\right]}{2\pi f_{in}} \quad (17)$$

$$= 2.13 \text{ ms}$$

In order to evaluate the rms ripple current $I_{cap(rms)}$ of the smoothing capacitors C_{in}, a triangular approximation is used to simplify the derivation. The a.c. peak current $I_{cap(pk)}$ of C_{in} is,

$$I_{cap(pk)} = \frac{C_{in}}{2}\frac{dV_{CC}}{dt} \quad (18)$$

$$= \pi f_{in} C_{in} \sqrt{V_{CC(pk)}^2 - V_{CC(min)}^2}$$

$$\approx 5.5 \text{ A for the practical value of } C_{in} \text{ equal to } 220\ \mu F.$$

Thus,

$$I_{cap(rms)} \approx I_{cap(pk)} \sqrt{\frac{D}{3}} = I_{cap(pk)} \sqrt{\frac{t_a}{3T/2}} \quad (19)$$

$$= 1.47 \text{ A}$$

assuming that the a.c. component contributed by the switching operation of the flyback converter is negligible. This assumption holds because the high-frequency (switching frequency) ripple current is filtered by the additional small-valued capacitor (0.1 μF) connected across V_{CC}.

With reference to Figure 7(d), for the voltage doubler, the two capacitors are alternatively charged to peak line voltage. Note that whenever the rectified voltage V_{CC} is at instantaneous minimum $V_{CC(min)}$, the voltage of one capacitance is at its minimum, but the voltage on the other capacitor is at half way between peak and minimum voltages, $V_{C(pk)}$ and $V_{C(min)}$ respectively. The value of $V_{C(min)}$ can be determined as follows.

$$V_{CC(min)} = V_{C(min)} + [V_{C(min)} + V_{C(pk)}]/2$$

$$\text{or } V_{C(min)} = [2V_{CC(min)} - V_{C(pk)}]/3 \quad (20)$$

$$= 91 \text{ V for } V_{C(pk)} = 90 \times 1.414 = 127 \text{ V and } V_{CC(min)} = 200 \text{ V.}$$

From energy law,

$$P_{in}/2 \approx 1/2\ C_{in}\ [V_{C(pk)}^2 - V_{C(min)}^2]\ f_{in}$$

or

$$C_{in} = \frac{P_{in}}{V_{C(pk)}^2 - V_{C(min)}^2}\frac{1}{f_{in}} \quad (21)$$

$$= 327.5\ \mu F \text{ at } f_{in} = 50 \text{ Hz and full load.}$$

The time t_a, ripple currents $I_{cap(pk)}$ and $I_{cap(rms)}$ are given by,

$$t_a \approx \frac{\cos^{-1}\left[\frac{V_{C(min)}}{V_{C(pk)}}\right]}{2\pi f_{in}} = 2.46 \text{ ms} \quad (22)$$

$$I_{cap(pk)} = 2\pi f_{in} C_{in} \sqrt{V_{C(pk)}^2 - V_{C(min)}^2} \quad (23)$$

$$\approx 9.18 \text{ A for } C_{in} = 330\ \mu F \text{ (practical value).}$$

$$I_{cap(rms)} \approx I_{cap(pk)} \sqrt{\frac{t_a}{3T}} \quad (24)$$

$$= 1.86 \text{ A}$$

As the power supply is designed to operate at both input ranges, the latter case defines the relevant maximum ripple current. In order to demonstrate the effectiveness of the universal input-voltage adaptor, the ripple current and voltage assuming no doubler are calculated to be, with $C_{in} = 330\ \mu F$, $V_{in} = 90$ Vac and Pin = 128.6 W at 50 Hz,

$$V_{CC(min)} = [127^2 - 128.6/(60 \times 165\mu)]^{1/2} = 23.3 \text{ V}$$

$\delta V_{CC} = 127 - 23.3 = 103.7$ V (compared with 55 V for high range)

$t_a = 4.4$ ms

$I_{cap(pk)} \approx 6.5$ A

$I_{cap(rms)} \approx 3$ A (nearly double of the value with voltage doubler).

Such a large ripple voltage at V_{CC} will greatly stress the switching transistor and will degrade the overall performance, especially the conversion efficiency and regulation.

The bridge rectifiers are selected to be 1N5398, a 1.5 A device because the highest average line input current is 0.9 x 128.6/90 ≈ 1.3 A. The two 1 W resistors, in parallel with C_{in}, are used to discharge the input capacitor after powered off. Note that one of them is connected to "start-up" at one end instead of the ground (the inverted triangular sign). It provides the starting current for the current-mode controller and drive circuit at initial power-on, when the control circuitry is still not self-supplied. The start-up current is limited to approximately 2 to 4.6 mA.

The inrush input current is limited to an acceptable level by the thermistor which has a resistance of 5 Ω at room temperature and 1 Ω after heated up.

MAC229A8 has been found suitable for the triac in the universal input-voltage adpator because of the following points:

1. It is a sensitive gate device with I_{GT} of 10 mA maximum for operation quadrants I, II and III [13]. The small gate current requirement will minimize the power dissipation in the adaptor and will lower the capacitance of the charge-pump capacitor C.
2. Its breakdown voltage is 600 V, which exceeds all input voltage limits.
3. Guaranteed 25 V/μs, rate of rise of off-state voltage ensures the accurate operation of MAC229A8 [13].
4. Low power loss in the device due to its low voltage drop across MT1 and MT2 at operation.

MC3423 is originally designed for overvolt "crowbar" sensing circuit, but it is also applicable in the universal input-voltage adaptor because of the similar working condition [14]. It has a temperature-compensated internal reference voltage of 2.6 V which is connected to one terminal of the input comparator. Thus, if the trip point at which the triac is turned off is set to 135 Vac or 191 Vdc, the divider ratio in Figure 7(a) is,

$$2.6 = 191 \times R_2/(R_1 + R_2)$$

or $R_1/R_2 = 72.5$

$R_1 = 2.2\ M\Omega$ and $R_2 = 30\ k\Omega$.

The internal constant current source (pin 4) can provide a time delay before tripping the "crowbar" SCR. It results in better noise immunity and controlled start-up transients of the adaptor. The practical values of the capacitor and resistor connected at pin 4 to ground are 50 nF and 560 kΩ, respectively, which has a time delay of approximate 650 μs. The output is connected, through a resistive divider, to a small-power SCR (MCR102 with $I_{K(max)}$ = 0.8 A). When the input voltage is detected to be above the trip point, the SCR is fired to shunt all the incoming current from the charge pump, and the triac will remain off.

The MC3423 can operate from 4.5 V to 40 V of supply voltage [15]. Hence, a 6.2 V zener diode is used to clamp the supply voltage of the crowbar senser to 6.2 + 0.7 ≈ 7 V for stable operation. A 100 pF filtering capacitor for the sensing divider and a small-signal diode 1N4148 for clamping the input of MC3423 are also added in the circuit.

To calculate a suitable value for the charge-pump capacitor C, the working principle of the charge pump is first considered. It consists of two diodes (1N4001), a coupling capacitor C, and a smoothing capacitor (100 μF). C is charged during the rise time of input voltage and is discharged during fall time. Assuming that the voltage drop on the charge pump circuit is much less than the peak of input voltage (Vp), from charge balance principle,

$$Q = (2Vp)\ C = IT$$

or $C = (IT)/(2Vp)$

where I = average d.c. current supplied to the line adaptor.

The boundary case is at low line, low range, where Vp = 127 V and I = 10 mA for gate current plus 6 mA for bias current. Thus,

$$C = [(10 + 6)\ (1/50)]/(2 \times 127) \approx 1.2\ \mu F$$

At high line, high range, Vp ≈ 370 V and the maximum value of I is 53 mA at 60 Hz. The maximum power consumption of the line adaptor is 7 x 0.053 = 0.37 W. The 10 Ω resistor in series with C is used to limit the inrush current when starting.

So far in the design of the universal input-voltage adaptor, an important point which has not yet been considered is the hazard of severe overvoltage at V_{CC} during start-up. If the power supply is started at high line, high range, V_{in} = 260 Vac, during the falling edge of input voltage, and the supply voltage of MC3423 is charged to about 7 V, the triac will be turned on for the doubler operation in the remaining negative cycle of input voltage, without the gate capacitor C_G, since MC3423 had not yet and would not be tripped until the next positive cycle. Then, the lower bulk capacitor will be stressed to nearly double of its normal voltage rating. This harmful effect not only damages the bulk capacitor, but also produces abnormally high input voltage (V_{CC}) for the flyback converter, in a small instant. Therefore, C_G is connected to the gate and MT1 terminal of the triac to serve two purposes:

1. to delay the turn-on of triac for nearly a quarter of one cycle.
2. to increase the dV/dt blocking capability of the triac (> 200 V/μs) and hence, the overall system reliability [13].

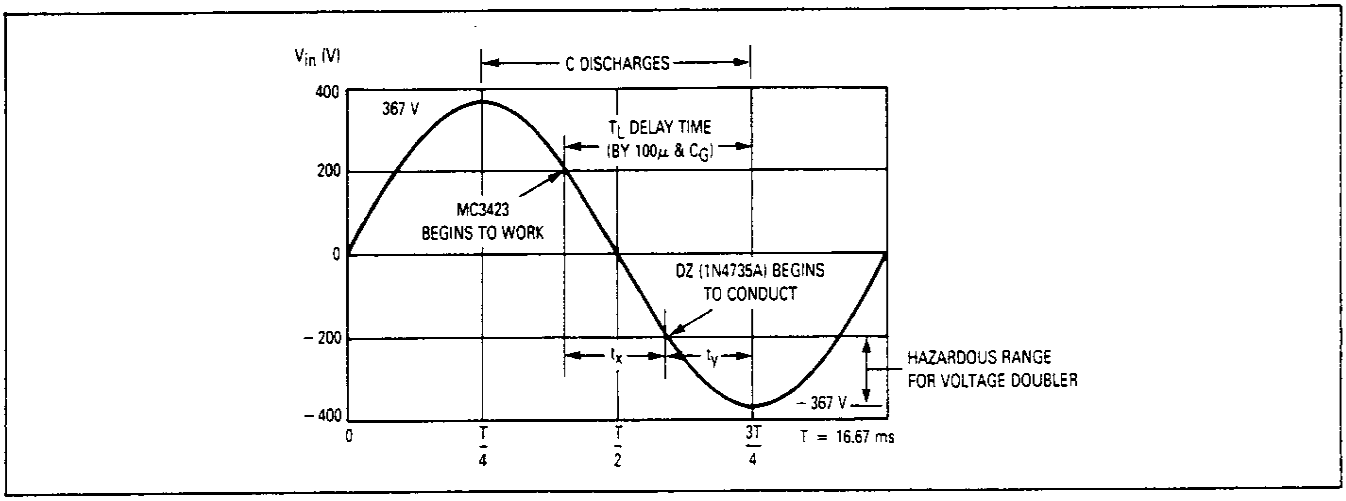
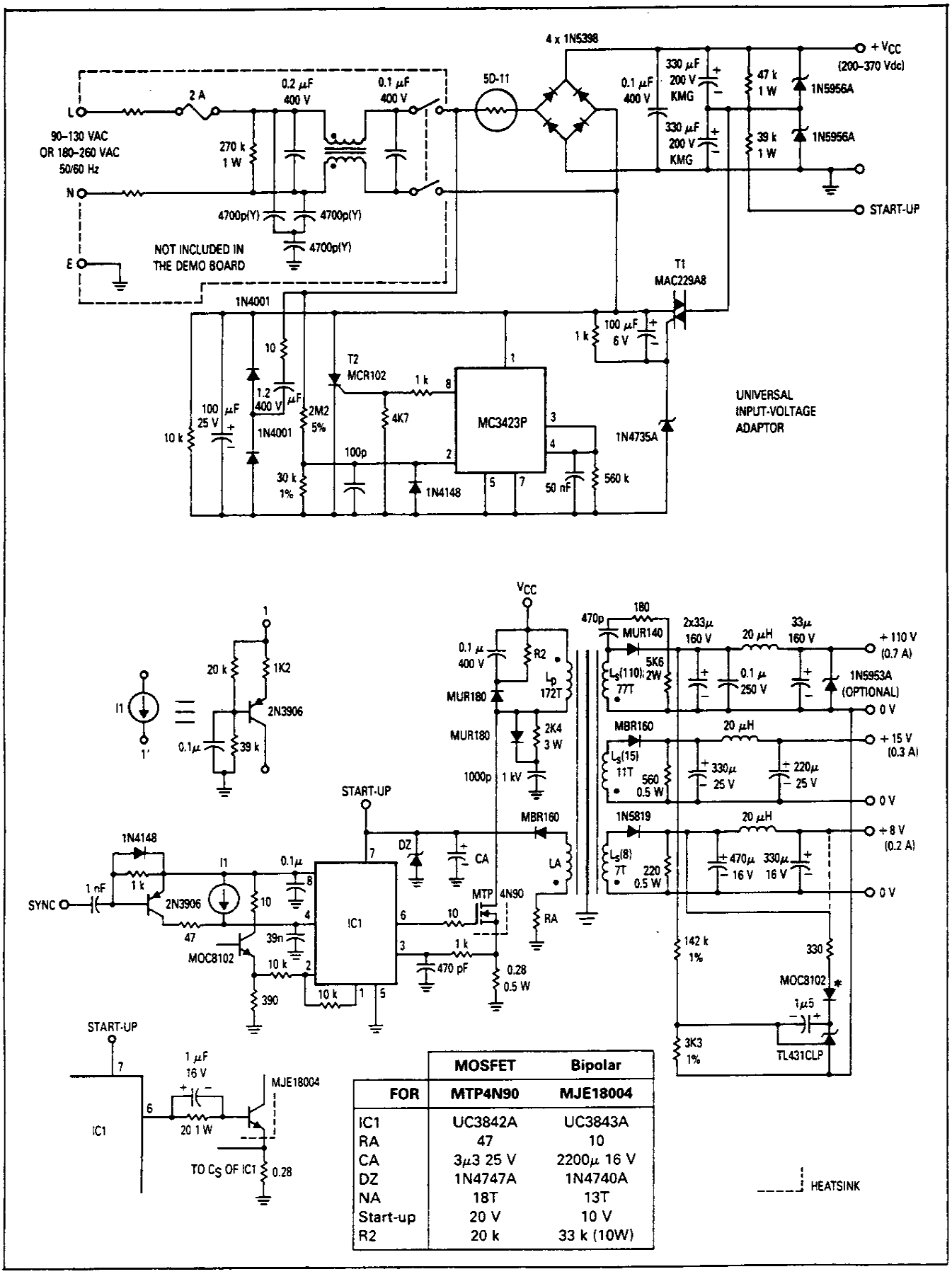


Figure 7e. Worst Case Consideration for the Universal Input-Voltage Adaptor (Negative Gate Current)



FOR	MOSFET MTP4N90	Bipolar MJE18004
IC1	UC3842A	UC3843A
RA	47	10
CA	3μ3 25 V	2200μ 16 V
DZ	1N4747A	1N4740A
NA	18T	13T
Start-up	20 V	10 V
R2	20 k	33 k (10W)

Figure 8. Complete Circuit Schematics of 90 W Off-the-Line Power Supply

The determination of the capacitance of C_G is determined as follows, with reference to Figure 7(e). At high line, high range, and 60 Hz, the average current I is maximum (53 mA). All discussions below are referred to a falling edge and the consecutive rising edge of less than 1/4 cycle of input voltage, because the charge-pump capacitor C is discharging to the adaptor circuit during fall time and the crowbar senser cannot be tripped if V_{in} falls beyond +200 V. If the supply voltage for MC3423 is just about 4.5 V, the crowbar sensing IC functions, and meanwhile, the instantaneous input voltage is at the trip point (200 V) and is going to the negative cycle, the gate capacitor C_G must be large enough to delay the conduction of the triac before the input voltage rises again, i.e. at the negative peak. Assume that, for simplicity, the supply voltage of MC3423 rises to about 6.2 V (zener voltage) when the input voltage falls to −200 V. Then,

t_x = charging time of the capacitor across the supply voltage of MC3423

$= 2 \times \sin^{-1} (200/367) / (2\pi \times 60) = 3$ ms

$\approx (6.2 - 4.5)$ V x (Capacitance value) / (53 − 6) mA

or capacitance value ≈ 100 μF (connected across supply voltage of MC3423)

But this capacitance is necessary to meet the ripple voltage requirement of the adaptor circuit. Afterwards, the zener diode (1N4735A) conducts, and the two capacitors connected in parallel are needed to delay the remaining time t_y before the input voltage rises from its negative peak again, within the same negative cycle. Therefore,

$t_y = (16.67/4 - 3/2)$ ms ≈ 0.7 V x $(C_G + 100)$ μF/47 mA

since the threshold gate voltage of MAC229A8 is 0.7 V typically.

$C_G = 79$ μF

A practical value of 100 μF is used in Figure 8. Note that the discharging current of C at zero-crossing of input voltage is greater than the average value I. The time constant of the gate capacitance and gate resistor (1 kΩ) is 0.1s, which is sufficient for resetting the triac between consecutive power-off and on. The 10 kΩ resistor is for discharge of the 100 μF capacitor, and the corresponding time constant is 1 second. Time constants too long in the above design may result in failure of the universal input-voltage adaptor if the power supply which was previously socketed in 110 V line is quickly plugged in 220 V line.

It should be noted that two optional power zener diodes (1N5956A) are connected across each bulk capacitor C_{in} because:

1. they can absorb short transient voltages (>200 V) on C_{in},
2. they can prevent any failure of the universal input-voltage adaptor from damaging the flyback converter and the two bulk capacitors.

Although such failures are rare the consequences are to be avoided since failure of the line adaptor poses a safety hazard to the human beings (especially the eyes radiated by X-ray).

Common-mode and differential-mode EMI/RFI filters are generally required for all switching power supplies. They are included in Figure 8, but are excluded in the DEMO board.

4. PERFORMANCE OF THE FLYBACK POWER SUPPLY

4.1 COMPLETE CIRCUITRY

Figure 8 shows the complete circuit schematic of the 90 W flyback power supply. The triac in the universal adaptor is negatively driven by the charge pump, since

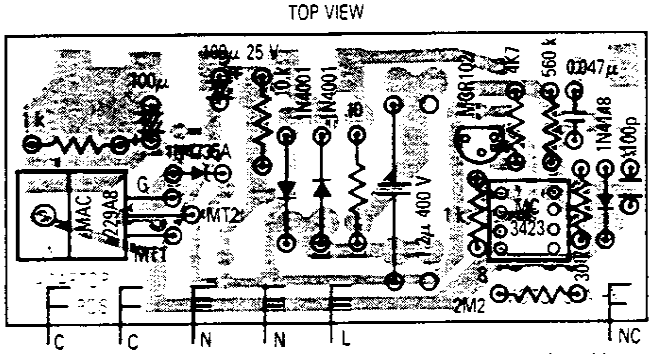


Figure 9a. Universal Input-Voltage Adaptor (+IG)

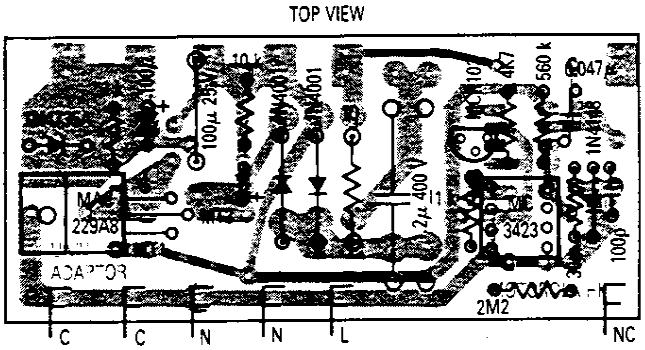


Figure 9b. Universal Input-Voltage Adaptor (−IG)

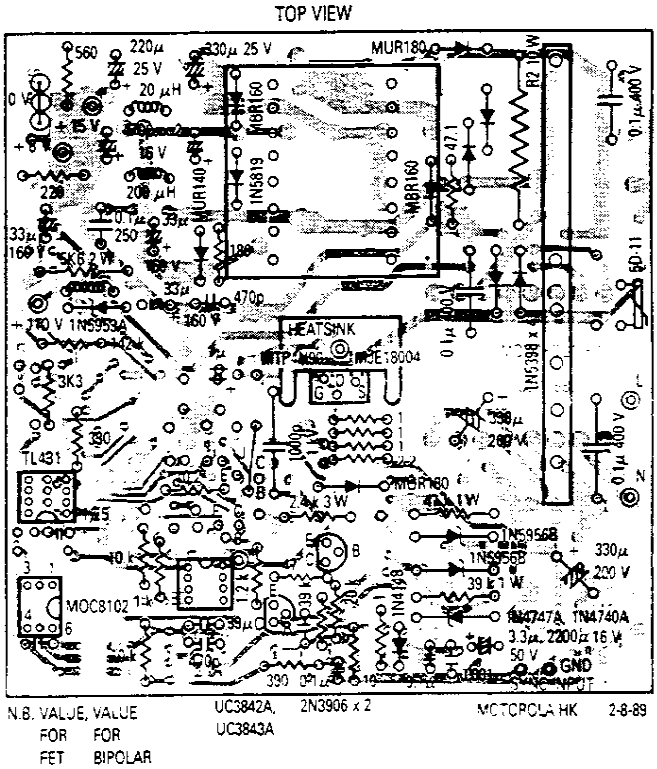


Figure 9c. Main Board (for MTP4N90 & MJE18004)

Figure 9. P.C.B. and Component Layouts

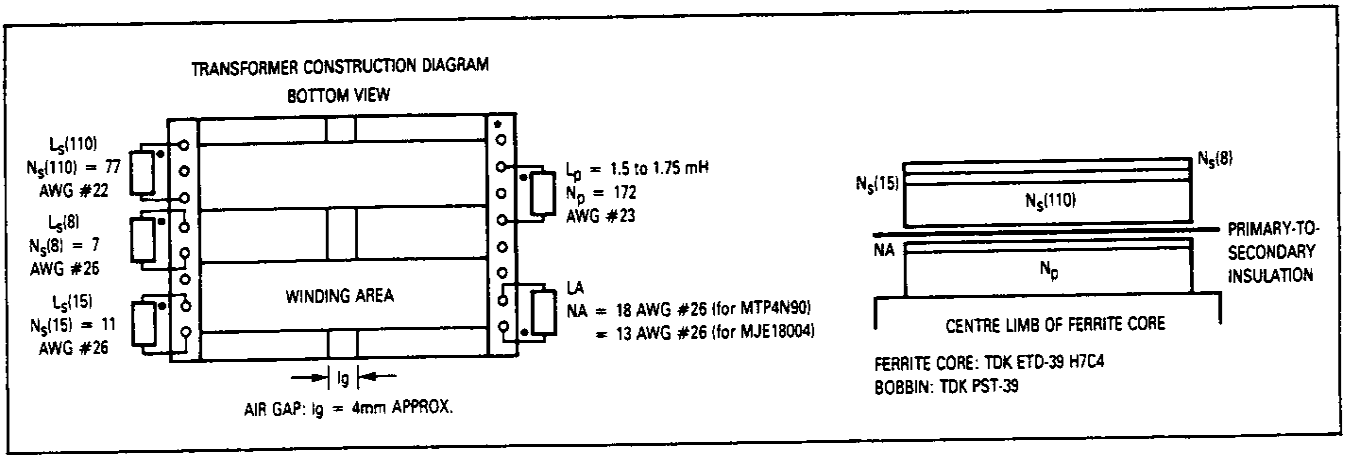


Figure 10. Flyback Transformer Construction

it is least sensitive to noise in this mode. Drive circuits for MTP4N90 and MJE18004 are also shown.

Sometimes, it is unnecessary to have the universal input-voltage adaptor because the power supply may be used only at one range. Then, a modular approach for the adaptor can lower the system cost and can increase the flexibility of manufacture. The universal input-voltage adaptor board can be simply removed or unplugged from the power supply board without affecting the normal operation of the power supply, if the adaptor is not needed. Therefore, using this approach, the adaptor becomes optional. The printed circuit board and component layouts of the universal input-voltage adaptor(s) and the main board of power supply are shown in Figure 9. The construction diagram of the power transformer is shown in Figure 10. Table 1 lists all Motorola semiconductor components used in this power supply.

Table 1. List of Motorola Semiconductor Components

	Part Numbers	Qty.
IC	UC3842A (for MTP4N90) UC3843A (for MJE18004) MC3423P TL431CLP	1 1 1 1
Opto	MOC8102	1
MOSFET	MTP4N90	1
SCR	MCR102	1
TRIAC	MAC229A8	1
BJT	MJE18004 2N3906	1 2
Rectifier	1N4001 1N5819 1N5398 MUR140 MUR180 MBR160	2 1 4 1 2 2
Zener	1N4735A 6.2 V 1N4740A 10 V (for MJE18004) 1N4747A 20 V (for MTP4N90) 1N5953A 150 V (optional) 1N5956A 200 V	1 1 1 1 2

4.2 EXPERIMENTAL MEASUREMENTS AND RESULTS

D.C. measurements are summarized in Table 2. Line and load regulation are excellent (better than 0.5%) for the +110 V output. Regulation for other two rails is within 10%, if the transformer is properly manufactured. Conversion efficiency, is close to the expected figure (70%), and the best one is 73.7% at $I_{O(110)}$ = 0.7 A, f_S = 15.7 kHz and V_{CC} = 360 V for MTP4N90; whereas for the bipolar power transistor MJE18004, the best efficiency is 74.2% at $I_{O(110)}$ = 0.7 A, f_S = 15.7 kHz and V_{CC} = 360 V. Although MJE18004 has lower conduction loss than MTP4N90, it has higher power losses in the base drive circuit and in the switching transitions. This is why MOSFETs can compete with advanced BJT even with higher conduction loss at relatively low switching frequency.

The maximum ripple voltage at 110 V output is approximately 150 mV (peak-to-peak) which is less than 0.2% of the output voltage, as predicted in section 2.3. The power supply is observed to be stable over the entire range of load currents. The dynamic response is also satisfactory, with an overshoot of less than 8 V at f_S = 15.7 kHz and V_{CC} = 200 V, from half-load to full-load (see Figure 1). Also in Figure 12, the transient responses of the power supply are introduced for very large-signal disturbances — from no load to full-load. The overshoot is about 20 V and the undershoot is over 30 V, which is quite satisfactory. The overshoot can be further reduced by increasing the integrating capacitance C_f in the feedback loop. But, this will result in slower transient responses.

Typical experimental switching waveforms are shown in Figure 11, at different load currents, input voltages and switching frequencies. Also, Figure 13 shows the photo of the 90 W off-the-line power supply.

5. CONCLUSION

A low-cost 90 W flyback power supply with external synchronization and universal input-voltage adaptor for multi-sync color monitor has been discussed in detail. The power supply has excellent line and load regulation and is found to be suitable in the application of low-cost multi-sync color monitors or TVs. Also, it can operate at both a.c. mains, i.e. 90–130 V or 180–260 V, without greatly affecting the system cost and performance.

Table 2. Performance of 90 W Off-the-Line Flyback Power Supply

MTP4N90 (MOSFET)

I_o (110 V)	V_o (110 V)	(15 V)	(8.0 V)	f_s	I_{in}	V_{CC}	Efficiency
0.2	110.1	16.01	8.88	15.7	0.12	300	61.2
0.5	110.0	16.23	9.05	15.7	0.26	300	70.5
0.7	109.9	16.31	9.10	15.7	0.35	300	73.3
0.7	109.9	16.32	9.10	15.7	0.55	200	69.9
0.7	109.9	16.30	9.10	15.7	0.29	360	73.7
0.2	110.1	15.99	8.88	25.0	0.13	300	56.5
0.5	110.0	16.19	9.03	25.0	0.26	300	70.5
0.7	110.0	16.25	9.08	25.0	0.35	300	73.3
0.7	110.0	16.26	9.07	25.0	0.53	200	72.6
0.7	109.9	16.25	9.08	25.0	0.29	360	73.7
0.2	110.1	15.98	8.88	32.0	0.13	300	56.5
0.5	110.0	16.17	9.03	32.0	0.26	300	70.5
0.7	110.0	16.23	9.07	32.0	0.35	300	73.3
0.7	110.0	16.24	9.07	32.0	0.53	200	72.6
0.7	110.0	16.23	9.07	32.0	0.30	360	71.3
A	V	V	V	kHz	A	V	%

MJE18004 (Bipolar)

I_o (110 V)	V_o (110 V)	(15 V)	(8.0 V)	f_s	I_{in}	V_{CC}	Efficiency
0.2	110.8	14.41	8.82	15.7	0.12	300	61.6
0.5	110.7	14.65	9.00	15.7	0.26	300	71.0
0.7	110.6	14.82	9.11	15.7	0.35	300	73.7
0.7	110.6	14.73	9.06	15.7	0.54	200	71.7
0.7	110.6	14.83	9.11	15.7	0.29	360	74.2
0.2	110.8	14.44	8.83	25.0	0.13	300	56.8
0.5	110.8	14.70	9.02	25.0	0.27	300	68.4
0.7	110.7	14.78	9.09	25.0	0.36	300	71.8
0.7	110.7	14.77	9.08	25.0	0.53	200	73.1
0.7	110.7	14.78	9.09	25.0	0.30	360	71.8
0.2	110.8	14.43	8.83	32.0	0.13	300	56.5
0.5	110.8	14.68	9.01	32.0	0.27	300	68.4
0.7	110.7	14.75	9.07	32.0	0.36	300	71.8
0.7	110.7	14.75	9.07	32.0	0.54	200	71.8
0.7	110.7	14.75	9.08	32.0	0.30	360	71.8
A	V	V	V	kHz	A	V	%

*Ripple voltage at 110 V output is about 150 mVpp at V_{CC} = 300 V, f_s = 15.7 kHz & I_o = 0.7 A.

Figure 11. Experimental Oscillograms

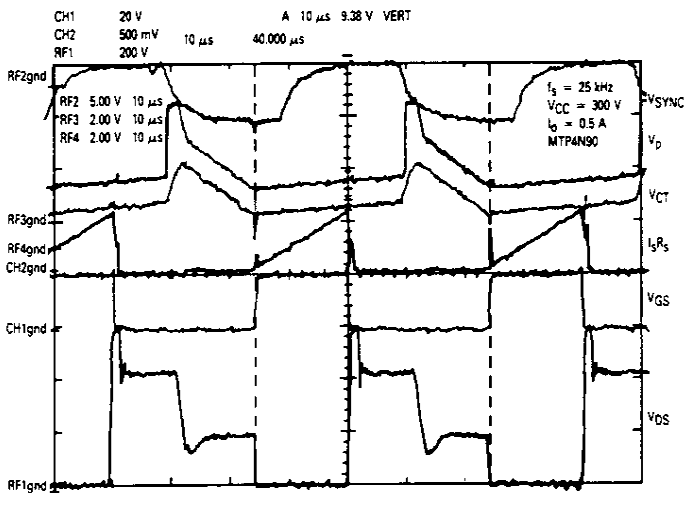


Figure 11a. Key Waveforms at f_s = 25 kHz and V_{CC} = 300 V (for MTP4N90)

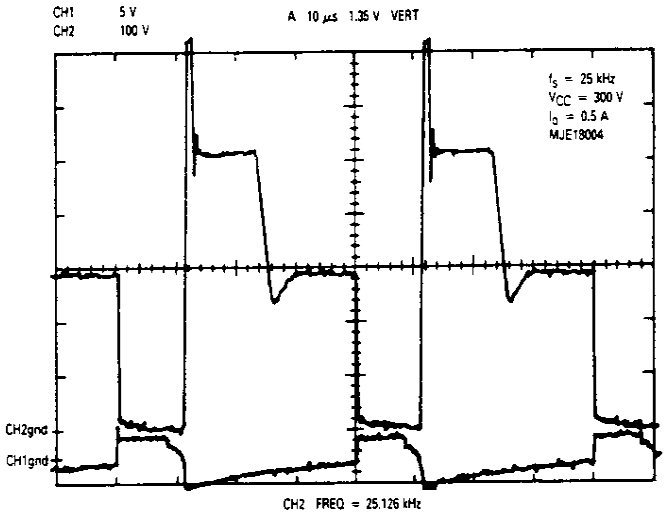


Figure 11b. V_{CE} and V_{BE} at f_s = 25 kHz and V_{CC} = 300 V (for MJE18004)

Figure 11. Experimental Oscillograms

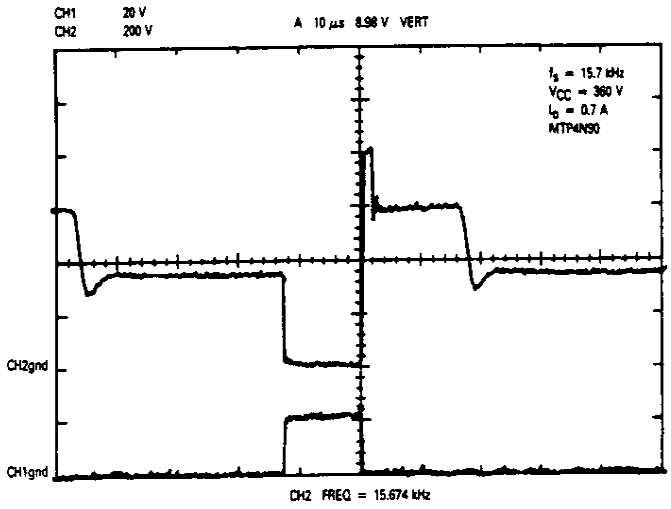


Figure 11c. V_{DS} and V_{GS} at f_s = 15.7 kHz and V_{CC} = 360 V (for MTP4N90)

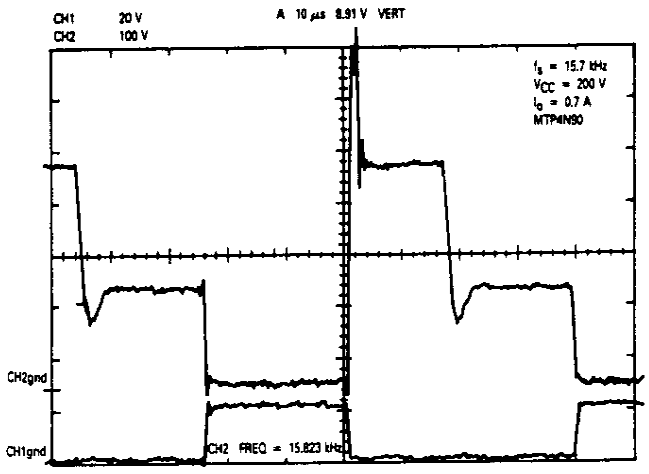


Figure 11d. V_{DS} and V_{GS} at f_s = 15.7 kHz and V_{CC} = 200 V (for MTP4N90)

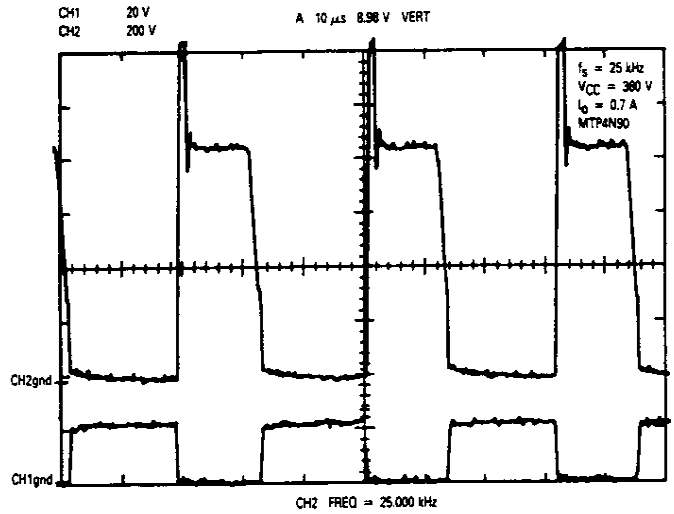


Figure 11e. V_{DS} and V_{GS} at f_s = 25 kHz and V_{CC} = 360 V (for MTP4N90)

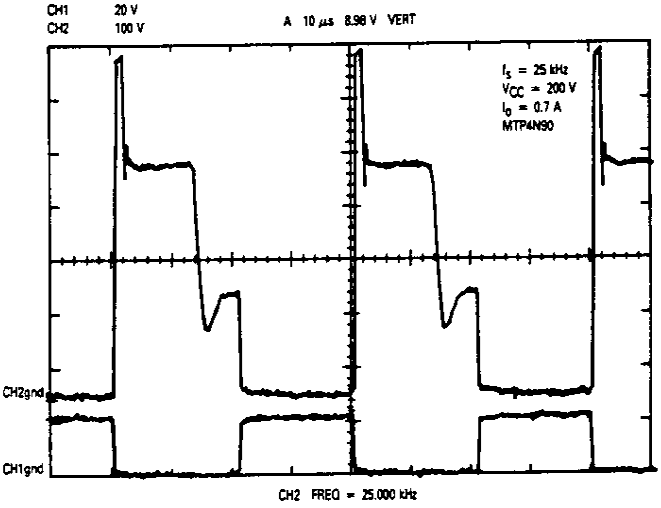


Figure 11f. V_{DS} and V_{GS} at f_s = 25 kHz and V_{CC} = 200 V (for MTP4N90)

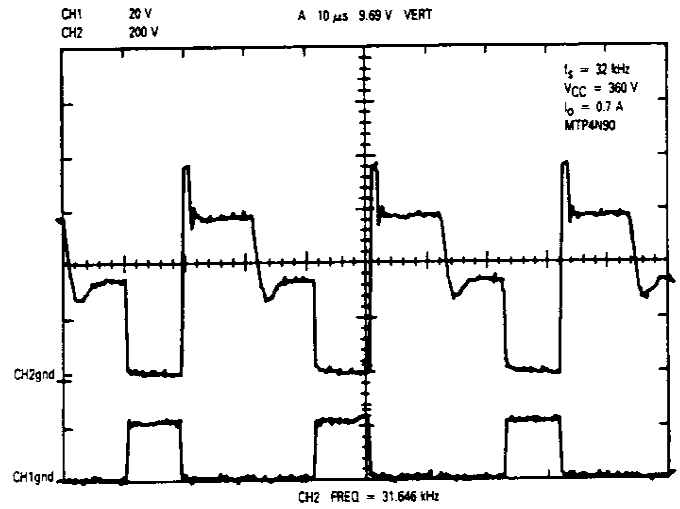


Figure 11g. V_{DS} and V_{GS} at f_s = 32 kHz and V_{CC} = 360 V (for MTP4N90)

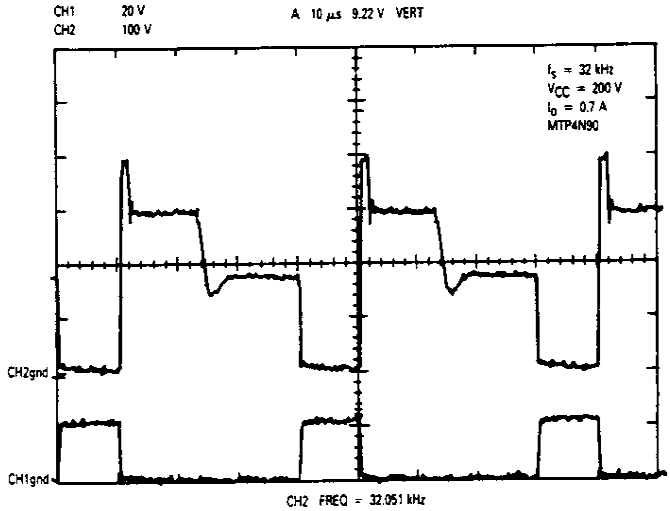


Figure 11h. V_{DS} and V_{GS} at f_s = 32 kHz and V_{CC} = 200 V (for MTP4N90)

Figure 12. Large-Signal Transient Load Responses

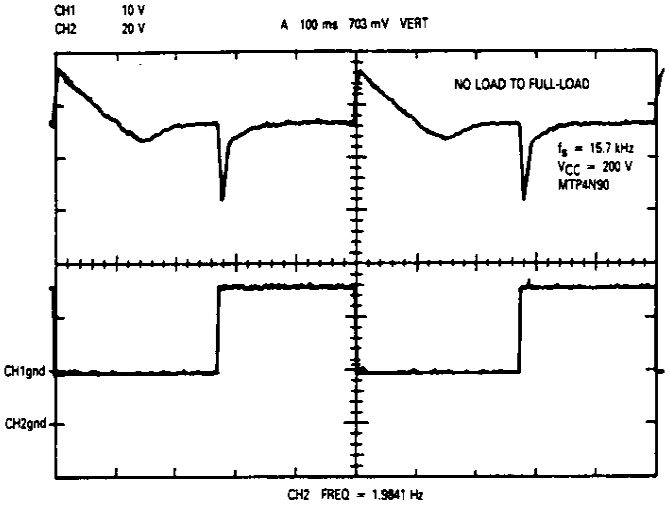


Figure 12a. For MTP4N90, From No Load to Full-Load at f_S = 15.7 kHz.

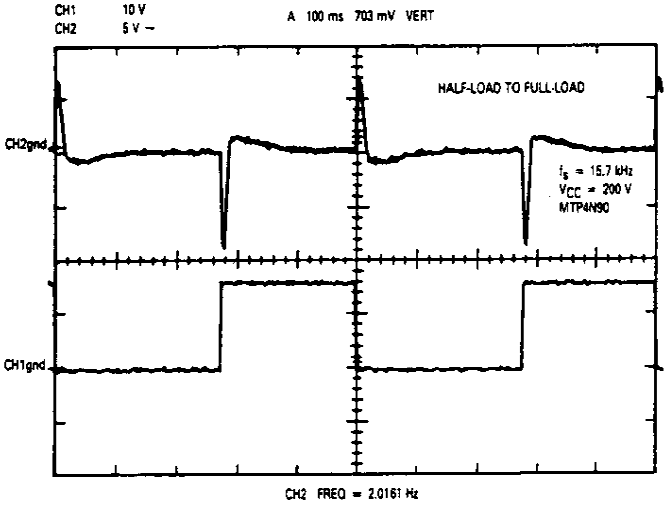


Figure 12b. For MTP4N90, From Half-Load to Full-Load at f_S = 15.7 kHz.

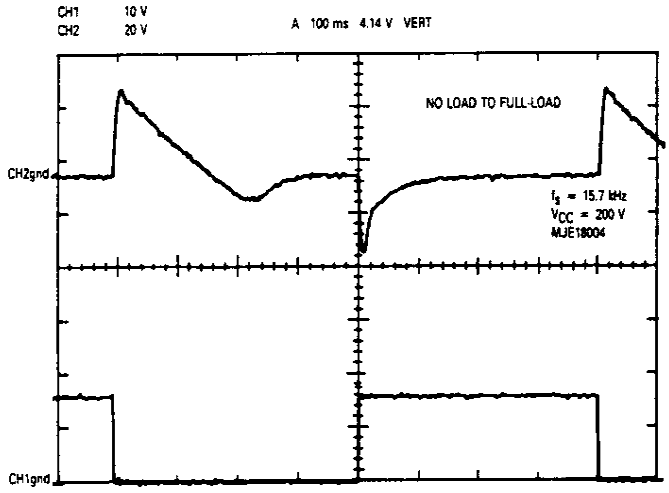


Figure 12c. For MJE18004, From No Load to Full-Load at f_S = 15.7 kHz.

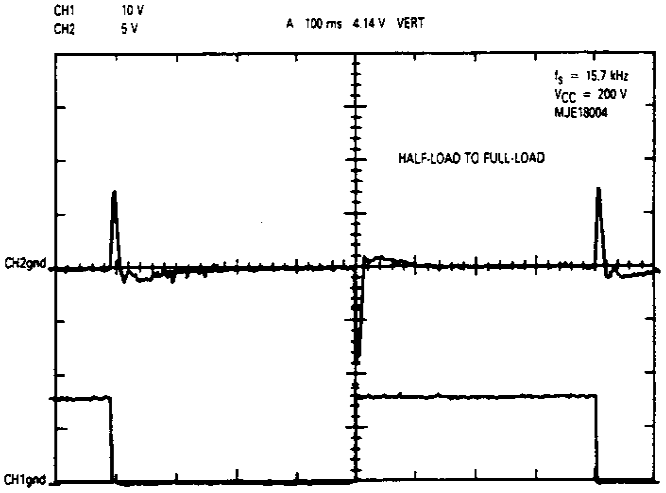


Figure 12d. For MJE18004, From Half-Load to Full-Load at f_S = 15.7 kHz.

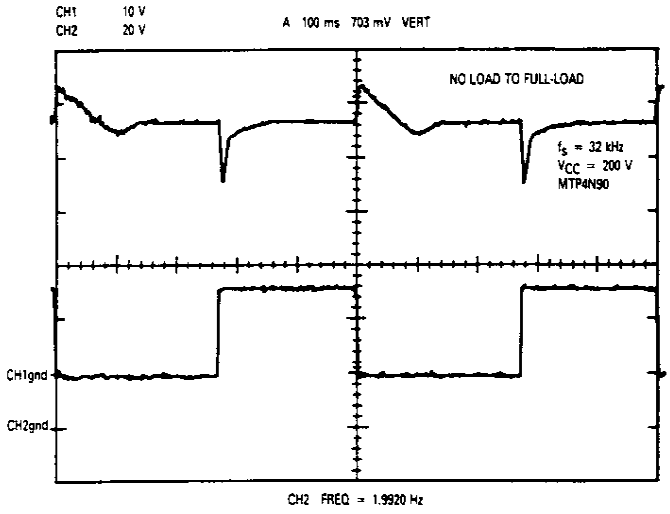


Figure 12e. For MTP4N90, From No Load to Full-Load at f_S = 32 kHz.

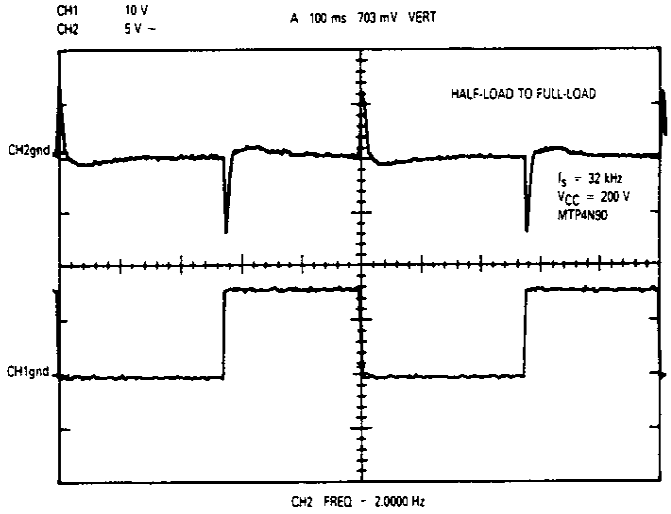


Figure 12f. For MTP4N90, From Half-Load to Full-Load at f_S = 32 kHz.

ACKNOWLEDGEMENTS

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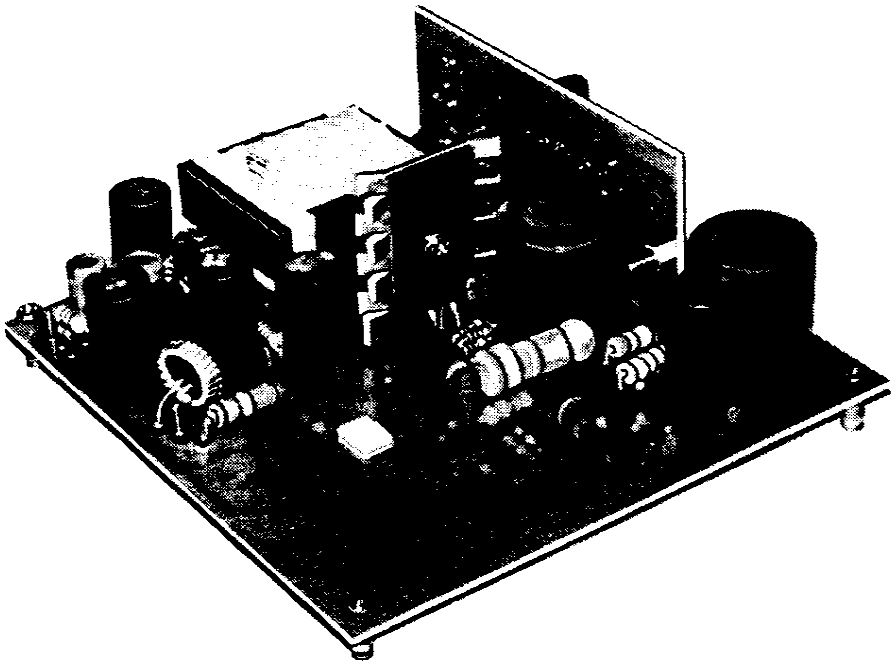

Figure 13. Photo of 90 W Off-the-Line Power Supply

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