MOTOROLA
SEMICONDUCTOR ▬▬▬▬▬▬▬▬▬▬▬▬▬▬▬▬▬▬▬▬
APPLICATION NOTE

AN1020

A High-Performance Video Amplifier For High Resolution CRT Applications

I. INTRODUCTION

This application note describes the superior performance characteristics of Motorola CRT driver transistors in a state-of-the-art video amplifier. In particular, the high speed obtainable with low DC power consumption is shown. A circuit which is insensitive to load variations and interconnect methods is given.

II. APPROACH

The performance requirements for the amplifier are these:

Voltage Gain	20
Rise and fall times	3 nS
Output	40 V p-p min.
Overshoot	5% max.
Load capacitance	8 pF min.
Power supplies	60 V, 5 V, −5 V

The voltage gain is obtained in a transconductance amplifier in the form of a common-emitter, common-base cascode circuit. In this circuit the load capacitance is isolated from the cascode by a set of complementary emitter-followers. Thus, the capacitive loading on the cascode is low, which allows operation at a moderate dissipation level.

The emitter followers are biased at a Class "B" operating point. They conduct only during voltage transitions, while charging or discharging the CRT capacitance. This operation is similar to the way highly efficient C-MOS logic ICs function.

The emitter followers provide a combined output signal from a low impedance, or "stiff" source. This stiff source makes the entire circuit insensitive to load variations and to different methods of connecting the video amplifier to the CRT.

III. THE CIRCUIT

A. The Input Circuit

Refer to the circuit diagram in Figure 1. A fast pulse generator is required for accurate performance data. The Tektronix Model PG502 is a good example of a pulse generator for optimum performance, versatility and price considerations. The pulse generator has a rise time in the range of .8 ns and an output impedance of 50 ohms. A minimum-loss L-pad is used between the generator and the base of the driver transistor, Q1. The impedance level at this point is designed to be 75 ohms. The voltage attenuation of the matching circuit is 0.64.

B. The Cascode Circuit

1. The Common-emitter stage uses an LT1001 transistor in a TO-39 package. The emitter current of 70 mA is supplied from a −5 V source via resistors R4, and R5. For ac, only R4 at 15 ohms is operative. R4 and the built-in emitter-ballast resistor of 1.6 ohms, determine the transconductance of Q1, which is then 60 mA/V.

Both the emitter current and the collector current of this stage follow the base voltage almost instantaneously. Computer simulation has shown that the transition times are less than 1 ns. The transconductance may be increased during the transition times by adding the "peaking-network" R6, C2, C3. Adding this network is very much like adjusting the rise time in the probes of fast oscilloscopes. In the cascade circuit under discussion the "peaking" network compensates rise time deterioration at the collector by speeding up the emitter current of Q1. This procedure must be applied with moderation since it may affect the large-signal swing capability. The resistor, R6, should be equal to or larger than R4. The capacitor, C2, determines the length of time during which "peaking" occurs. The product of R6 and C2 is typically a few nanoseconds. The trimmer, C3, can be used for fine-tuning, but is usually not important and may be omitted. If there is lead inductance associated with the path from the emitter of Q1 through C3 to ground, use of C3 may cause ringing at high frequencies.

2. The common-base stage uses an LT1817 transistor in a TO-117 package. Since the transistor must dissipate continuously some two Watts of DC power, good heatsinking is mandatory. The TO-117 package provides a high-conductance thermal path to a heatsink or chassis. At the same time, it adds only minimal capacitance to the circuit.
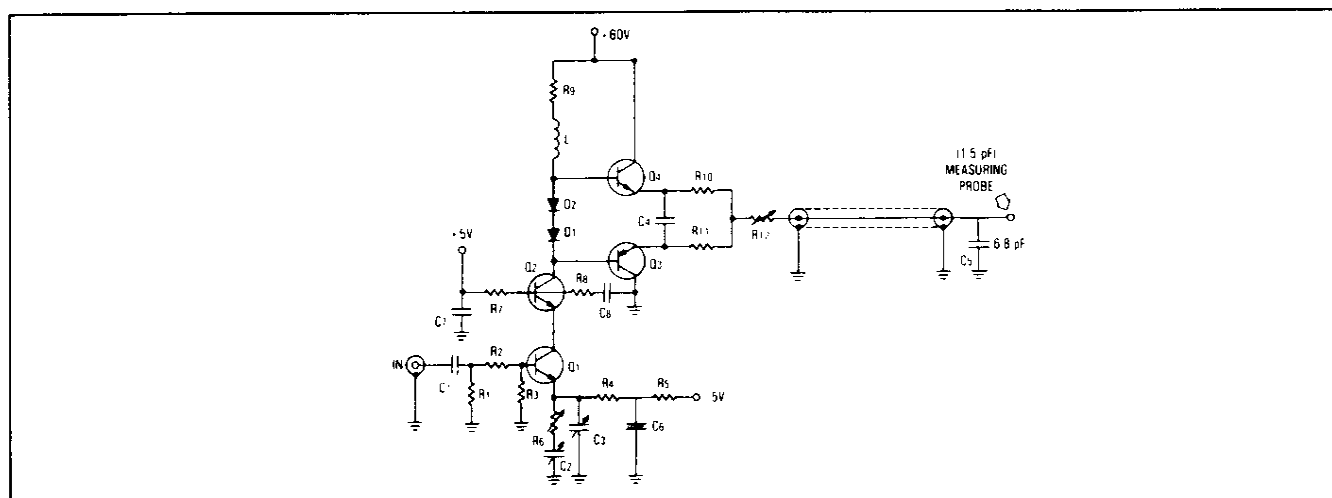

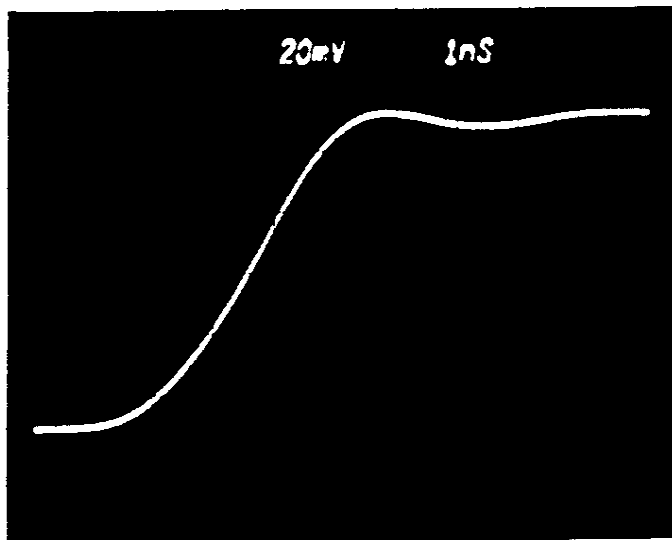**Figure 1. Circuit Diagram of Video Amplifier**
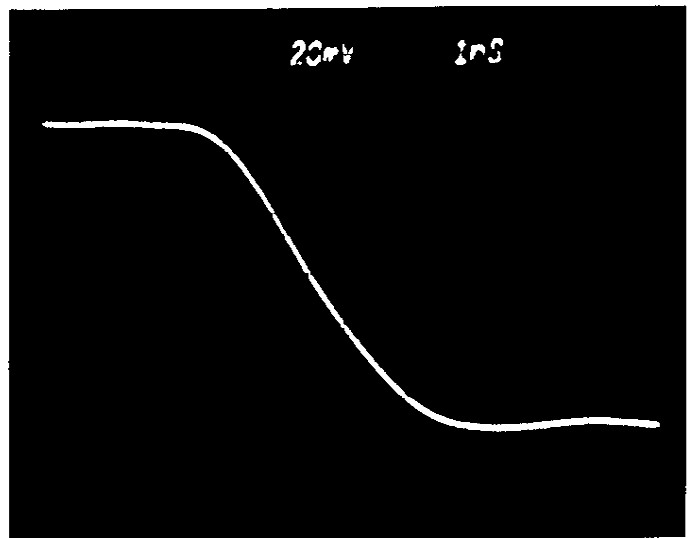
(M) **MOTOROLA** ▬

AN1020

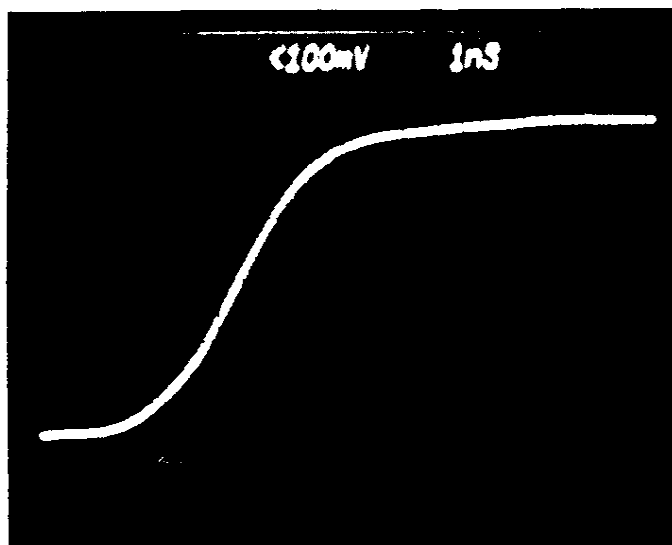Figure 2A. Rise Time at 10 V p-p

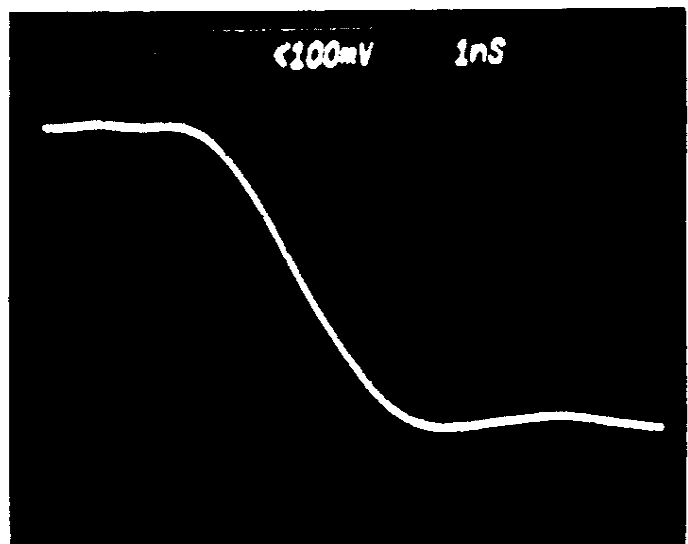Figure 2B. Fall Time at 10 V p-p

Figure 2C. Rise Time at 40 V p-p

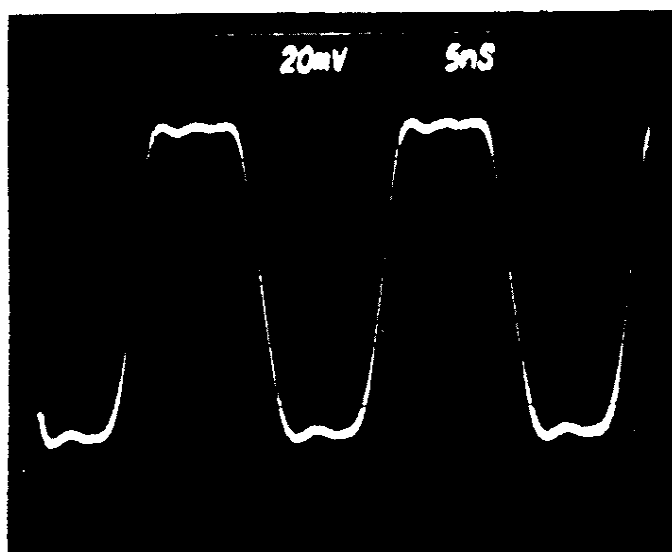Figure 2D. Fall Time at 40 V p-p

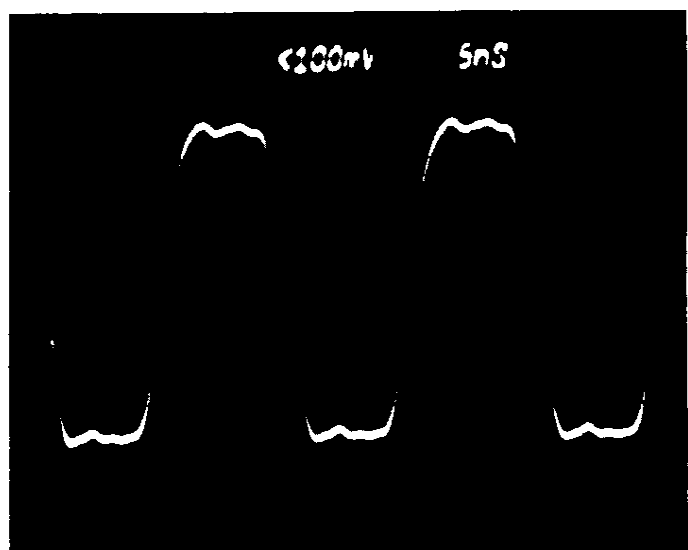Figure 2E. 10 nsec Pixels 10 V p-p

Figure 2F. 10 nsec Pixels 40 V p-p

The common-base stage has near unity current gain and acts as an impedance transformer, providing a current source at its collector. This current charges the combined collector capacitances of Q2, and the emitter-followers, Q3 and Q4, which add up to about 5 pF at the operating point. To this total one must add about one pF of stray capacitance. A load- or "pull-up" resistor of 430 ohms is used at the collector of the common-base transistor, Q2. The rise time at this point may be calculated to be:

$$t_r = .35 \cdot 2 \cdot Pi \cdot 430 \cdot 6 \, pF = 5.7 \, nS$$

This value is improved by the addition of a peaking coil of .22μH. Theoretically, the rise time could be reduced by up to 40% (without overshoot) by optimizing the inductance. Due to the non-linear nature of the capacitances to be compensated for here, different effects result for rise and fall times. This situation requires a compromise resulting in a practical improvement of less than the theoretical transition time. Nevertheless, 3 ns transition times are obtained at the collector of Q2 by means of the emitter peaking discussed earlier.

The LT1817 is packaged in a common-base configuration. This means that the transistor base is connected to two symmetrical low-inductance base leads. As is well known, base-lead inductance may cause instabilities in common-base configurations. To prevent this from happening, base damping resistors, R7 and R8, have been added. The value of these resistors depends on the device bias point and the circuit layout. If oscillations occur, they would be near a Gigahertz or higher, and therefore may not be seen on anything but a sampling oscilloscope. They will affect rise times and output swing capability. Instabilities may be easily detected with a spectrum analyzer connected to the input jack of the video amplifier. Enough signal will feed back through the collector capacitance of Q1 to reach the analyzer.

3. The emitter-followers, Q3 and Q4, are a complementary pair of transistors, LT1829 and LT5839, in TO-39 packages. The transistors are biased to the threshhold of conduction by two diodes, D1 and D2. These diodes should be relatively large, slow rectifier types, each providing no more than 0.6V of bias with a forward diode current of 70mA. The diodes have low, largely capacitive impedances at high frequencies, and should be connected with short leads between the bases of Q3 and Q4.

The emitter followers provide temporary charging currents to the output circuit whenever the voltage across the load is changed. In case of a

display with high contrast and many transitions, the current in Q3 and Q4 may become appreciable, causing the transistors to heat up. The elevated junction temperature shifts the bias point from Class "B" in the direction of "AB."

If the emitters of these transistors were connected directly, a DC component of current would flow from the 60 V supply through the devices to ground. This "pole-current" would further heat up the junctions and might lead to thermal runaway. In the circuit described, this situation is prevented from occurring through the use of the emitter stabilizing resistors R10 and R11. Using capacitor, C4, prevents deterioration of the dynamic operation of the circuit.

A simpler, more primitive way to avoid thermal problems, is to use only one bias diode, or none at all. Doing this, however, has serious effects on the gray scale linearity at mid-range.

4. The output circuit. The LT1839 and LT5839 transistors have excellent peak current handling capabilities. Their emitter currents react virtually instantaneously to the base voltage. Even when supplying several hundred milli-amperes of peak charging current, the base-to-emitter gain holds up well. It is therefore possible to drive more elaborate load configurations than a bare capacitance. This ability may ease interconnect problems. The circuit described in Figure 1 is powerful enough to accommodate a piece of shielded cable between the CRT and the video amplifier. A twin-lead line or a single wire connection may also be used instead of the shielded cable. The circuit is not only able to drive elaborate interconnect networks, but also to handle substantially larger CRT capacitances without significant penalties in rise and fall times. For instance, this circuit is capable of driving 15 pF with 3.8 ns transition times.

In all cases, the presence of additional reactive circuit elements causes the output circuit to have resonances which will cause ringing or overshoots, if the output circuit is not properly damped. To this end, a variable resistor, R12, is included in the circuit. When adjusted for critical damping, the waveform will look smooth across the load capacitance.

In the demonstration circuit, (Fig. 1), a 6.5 pf chip capacitor simulates the CRT cathode capacitance. It is connected across a special jack, which has been designed for the Tektronix FET probe, Type 6201. Probe, jack and chip have a combined capacitance of 8pF. The FET probe may be used in conjunction with Tektronix sampling scopes or real-time scopes with band-widths of 300 MHz or more.

One may be tempted to use slower instruments, such as a 200 MHz type, and correct mathematically for the additional transition time contributed by the scope. We do not recommend this approach since slower scopes appear to produce wave shape distortions which lead to misleading rise-time values.

IV. AMPLIFIER PERFORMANCE

Figure 2 contains photographs showing rise and fall times at 10 V and 40 V peak-to-peak swing. Also shown are some response curves generated by the well-known circuit analysis program SPICE. Careful modelling of the semiconductors used, according to the theory of Gummel and Poon, resulted in good agreement between computer and laboratory-generated performance data. In addition, computer analysis offers insights, which cannot be obtained by practical measurements.

Shown in Figure 3 are the superimposed plots of the input voltage at the base of Q1 and the output voltage across the CRT capacitance. The second set of plots, Figure 4, displays the collector-current wave form of Q1 and the combined emitter circuits of the complementary set of emitter followers. The collector current of Q1 shows clearly the effect of "peaking," introduced by the emitter circuit components, R6, C2 and C3. Note that under full swing conditions (40 V p-p output), the waveforms are not quite symmetrical. The effect on the transition times of the output voltage, however, is minimal.

The example shown in both Figures 3 and 4 corresponds to a pixel-time of 10 ns, which is the practical minimum for a system with 3 ns transitions. When operating continuously at this rate, approximately 25mA of average current flows in each one of the emitter-followers. This causes a significant rise in case temperature for these devices. It is therefore recommended that clip-on heat radiators be used. There is no electrical penalty for this measure, since the collectors are on ground potential.

Heatsinking becomes absolutely mandatory if one explores the limits of the amplifier by operating at 100 MHz and beyond.

V. CONCLUSION

An amplifier was developed which meets all needs of a high-resolution CRT monitor. While practical considerations played an important part in the circuit realization, the primary purpose was to demonstrate transistor capability. It is hoped that enough background information was given to allow the reader to tailor his circuit to his specific needs.

TIME	V (100)				
*) --------	0.0000-01	1.5000+01	3.0000+01	4.5000+01	6.0000+01
+) --------	-1.5000+00	-7.5000-01	0.0000-01	7.5000-01	1.5000+00

TIME	V (300)				
*) --------	-2.0000-01	-1.0000-01	0.0000-01	1.0000-01	2.0000-01
+) --------	0.0000-01	3.7501-02	7.5000-02	1.1250-01	1.5000-01
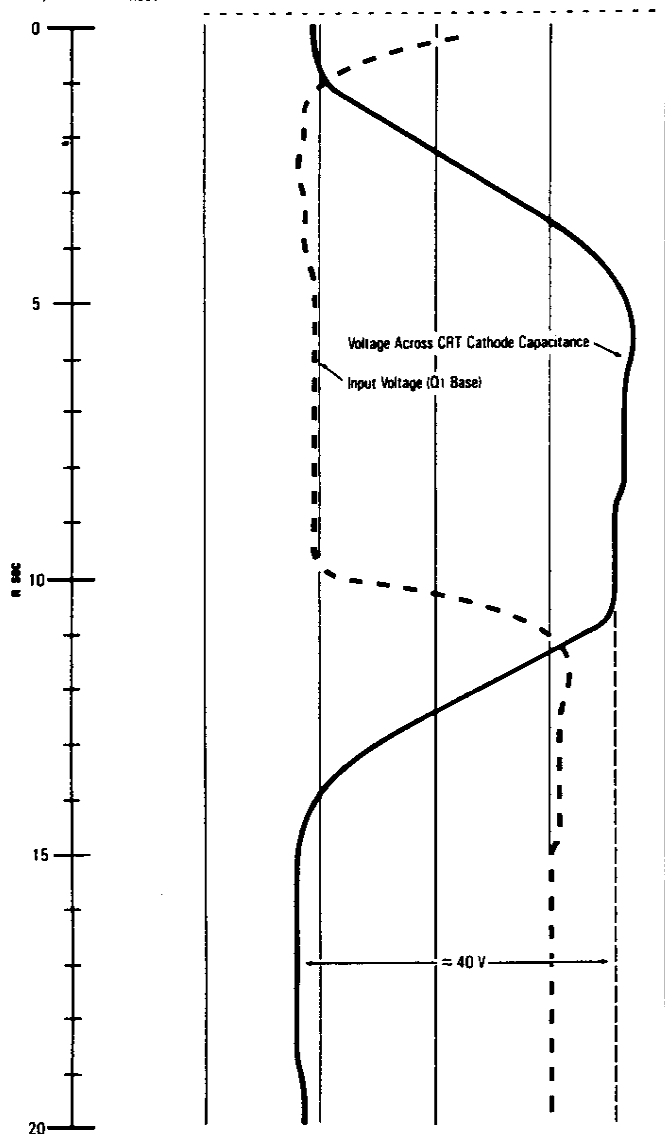
Figure 3. Computer Generated Voltage Plots

Voltage Across CRT Cathode Capacitance
Input Voltage (Q1 Base)
≈ 40 V
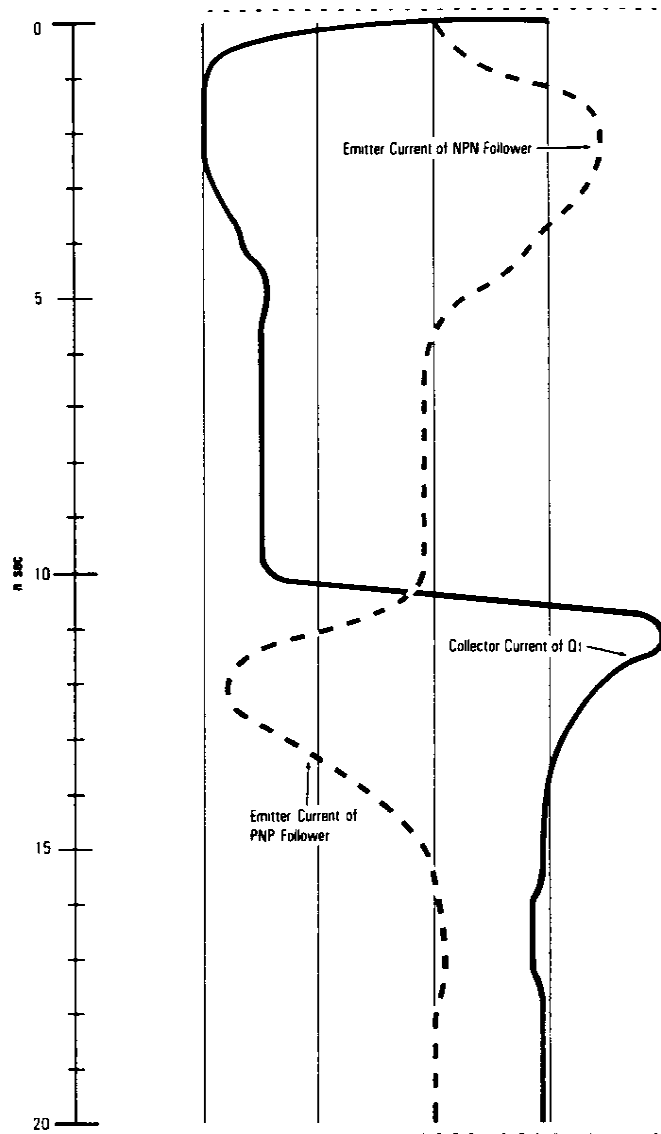
Figure 4. Computer Generated Current Waveforms

Emitter Current of NPN Follower
Collector Current of Q1
Emitter Current of PNP Follower

MOTOROLA

ClibPDF - www.fastio.com