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NTSC Decoding Using the TDA3330, with Emphasis on Cable In/Cable Out Operation

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PREFACE

The TDA3330 is a composite video to RGB Color Decoder originally intended for PAL and NTSC color TV receivers and monitors. The data sheet is oriented toward picture tube drive, rather than cable level outputs. This application note is intended to supplement the data sheet by providing circuits for video cable drive, such as used in video processing circuits, frame store, and other specialized applications, and to expand upon the functional details of the TDA3330.

CIRCUIT CONSTRUCTION TECHNIQUES

The best solution is a single or double sided PC board, such as shown in Figure 11, with as much ground plane as possible. The oscillator components at Pins 8 and 9 must be close to the pins. A low profile socket is acceptable for prototyping. Wirewrap is definitely not recommended. In most respects the part is not sensitive to layout, except for the oscillator, however, unwanted picture artifacts, beats and noise are much easier to control with a good ground plane layout.

MEASURING THE OSCILLATOR

The oscillator amplitude at Pin 9 should be about 400 mV_{pp}, measured with an ordinary 4.0 pF/10 MΩ scope probe. Keep in mind that the oscillator frequency is 3.58 MHz and is part of a phase-locked loop with only a few hundred Hz pull-in range. The scope probe loading is enough to push the oscillator into or out of lock. It is recommended that Pin 9 be observed initially to ascertain that it is running, and then leave Pins 8 and 9 alone. A procedure for adjustment will be covered later. Of course, an output buffer (emitter follower) can be connected to Pin 9, permanently, and the Pin 9 tuning capacitor reduced accordingly.

THE SANDCASTLE INPUT

"Sandcastle" is a familiar term to European TV engineers. It is basically a 0 V baseline with a 4.0 V blanking pulse and a 10 V burst-gating pulse on top of it, as shown in Figure 1. Sometimes the expression "super sandcastle" is used, which means that composite blanking is present, i.e. vertical and horizontal blanking, in addition to the burst-gating pulse. Sometimes the vertical blanking is 2.5 V and the horizontal is 4.0 V, sometimes both are at 4.0 V. In the TDA3330, the blanking portion is only used to provide a blanking waveform at the blanking output, Pin 11, which is used to supply "extra" blanking in the picture tube driver application. Pin 11 is not used in other applications, so the blanking portions of the "sandcastle" are not required. For the "cable to cable" decoder, all that the TDA3330 really needs at Pin 15 is the burst-gate pulse. Pin 16 should be grounded.

The burst-gate pulse has 3 functions:

1. Gating the color IF gain control (ACC) so that IF gain is adjusted to keep burst amplitude constant;
2. Setting the black level in the R, G, B outputs, and
3. Gating the color phase detector (APC) so that the VCO can be phase-locked to the burst. See the block diagram in Figure 2.

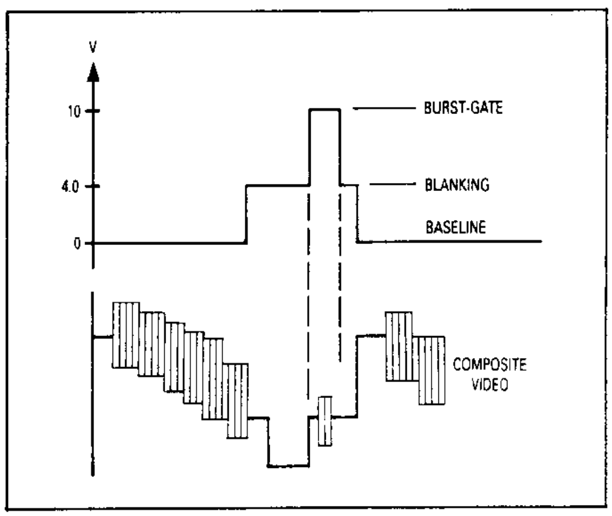


Figure 1. Sandcastle

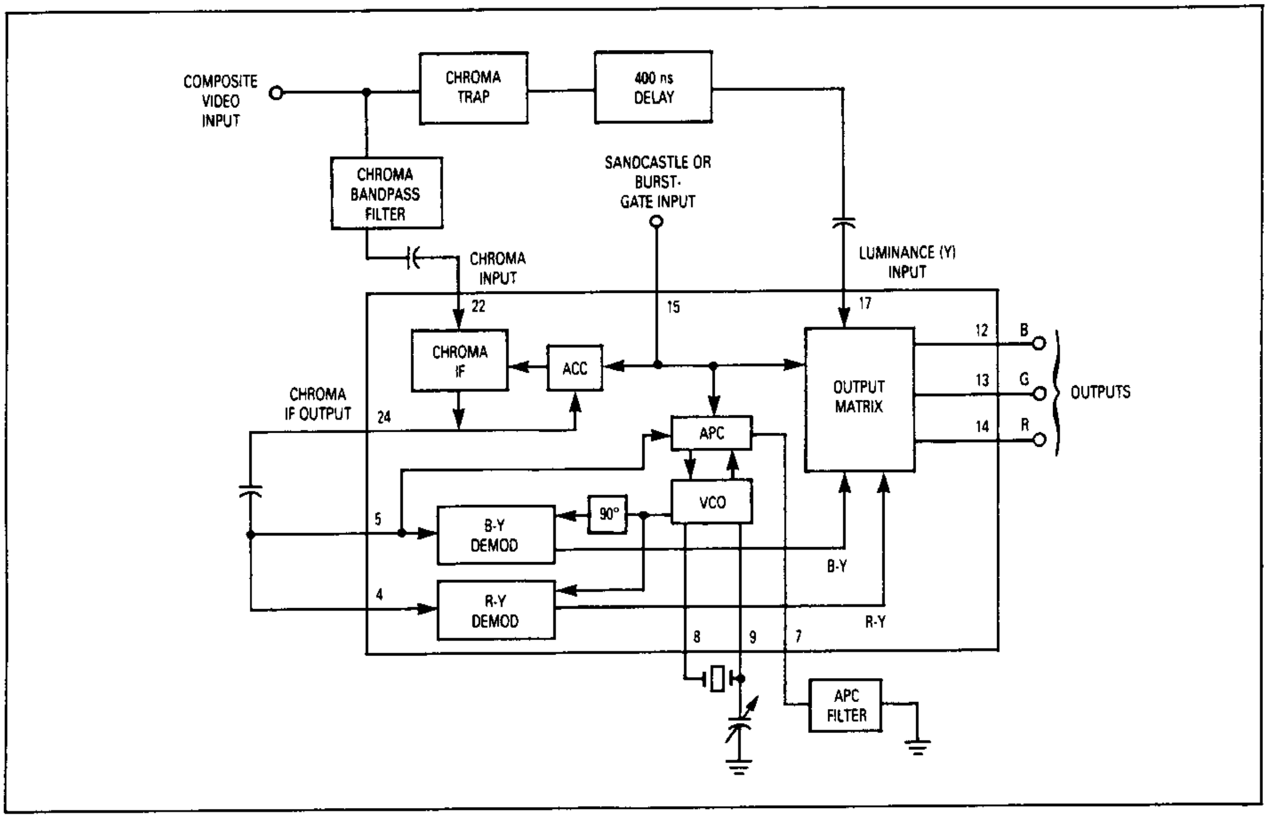


Figure 2. Simplified Block Diagram for NTSC Mode

It is important that the burst-gate pulse into Pin 15 be at least 8.0 V and timed correctly with respect to incoming video, as shown in Figure 3. If the gate pulse is too late or too wide it will still be present after the blanking has ended, leading to serious errors in black level, color level and VCO lock. The burst-gate pulse can sometimes be obtained from the same equipment that supplies the video, or it can be generated by a couple of one-shots and a sync separator; see Figure 4. Another method is to separate sync. Use a one-shot pulse stretcher to make an 8–8.5 μs wide pulse for Pin 15, and then put the separated sync into Pin 16. (Pin 16 could be called the "burst-gate inhibit"). This will prevent the first part of the Pin 15 pulse from gating sync, which would upset the black level clamping function; see Figure 5.

THE LUMINANCE PATH

The outputs at Pins 12, 13 and 14 are positive-going video, with the sync pulse almost completely removed. The black level of the output remains constant as the **contrast, saturation** and **hue** are changed. The **contrast** control changes both luminance and chrominance together, so that, for example, output color bar waveforms maintain the same shape. The DC level of all outputs is moved by the **brightness** control, with no change in the peak to peak signal amplitude. The **brightness** control can change black level from 1.4 V to about 6.7 V as the control voltage on Pin 18 is raised from about 2.0 V to 5.0 Vdc. See Figure 6. The **contrast** control, Pin 19, is at maximum at 5.0 Vdc; the output is reduced 6.0 dB when the control is 3.5 Vdc, and is reduced about 40 dB when the control voltage is 1.0 Vdc.

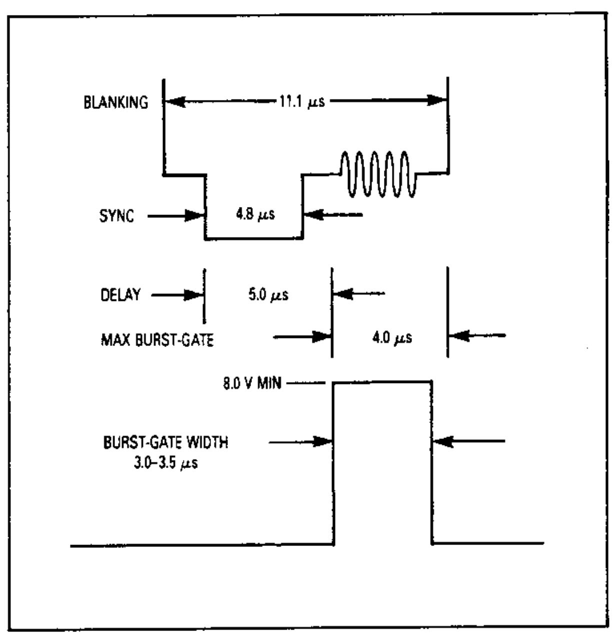


Figure 3. Burst-Gating

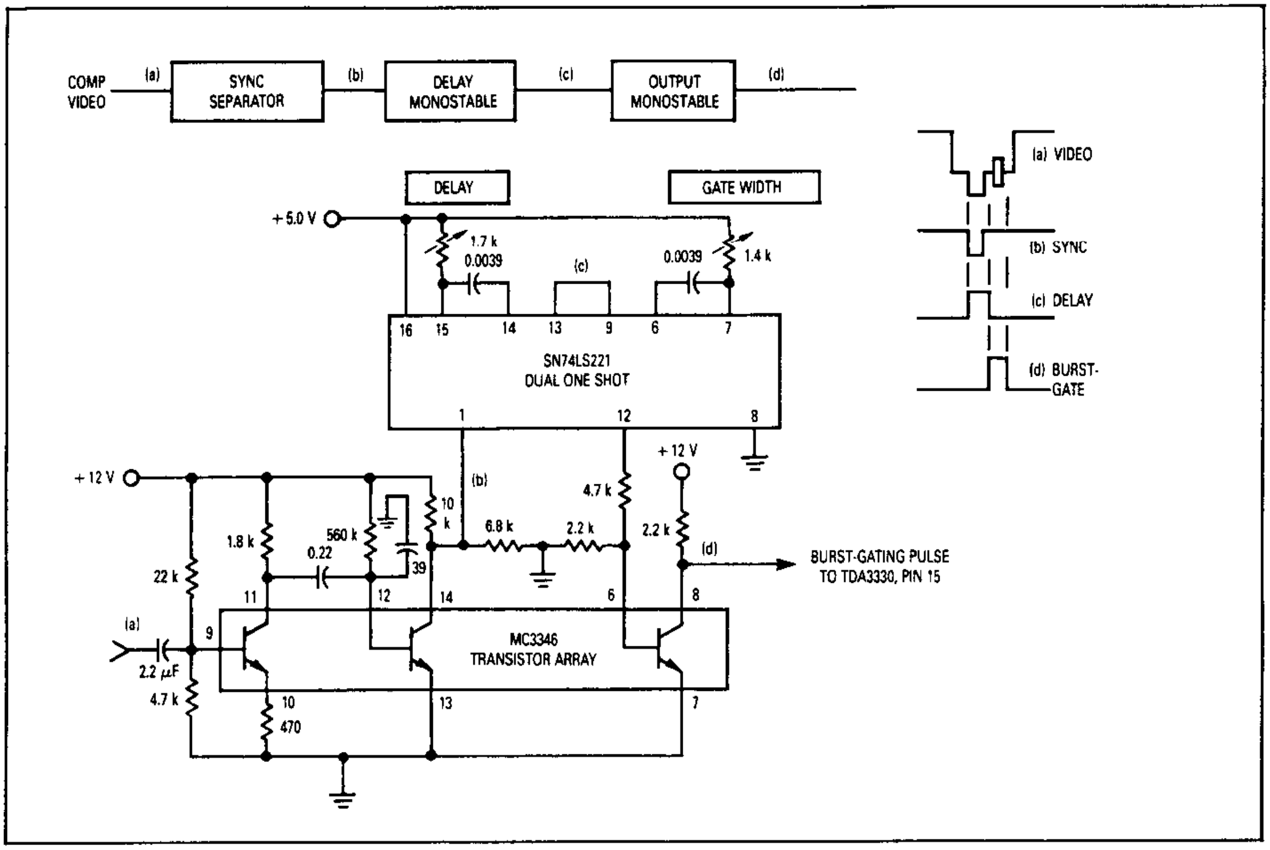


Figure 4. Method of Obtaining Burst-Gate from Composite Video

The maximum output voltage, black to white, is about 7 times greater than the *black* to *white* level at Pin 17. For a composite input signal of 1.0 V_{pp}, there is 0.5 V_{pp} at Pin 17, due to the delay line matching resistors. This is about 0.35 V_{pp} *white to black* and gives about 2.5 V_{pp} max at the outputs. The input to the total circuit can be doubled to 2.0 V_{pp}, which then yields about 5.0 V_{pp} at Pins 12, 13, and 14. However, note that any change in input amplitude requires readjustment of the **saturation** control for correct chroma/luma proportion. This is because the luminance component directly follows the input, while the color component is almost unchanged due to the ACC of the color IF. Therefore, it is important to note that the TDA3330 can be set up to work with different levels of input, but it is not automatically compensated for input changes. Also note that at 5.0 V_{pp} out and max **brightness** (black level out 6.7 V) there will be clipping of the positive peaks. The upper limit for the output is about 10 V.

Troubleshooting note: If a proper (positive) video signal is AC coupled into Pin 17, and a proper burst-gate is applied to Pin 15, there should be video out, regardless of any aspects of the color processing portions of the IC.

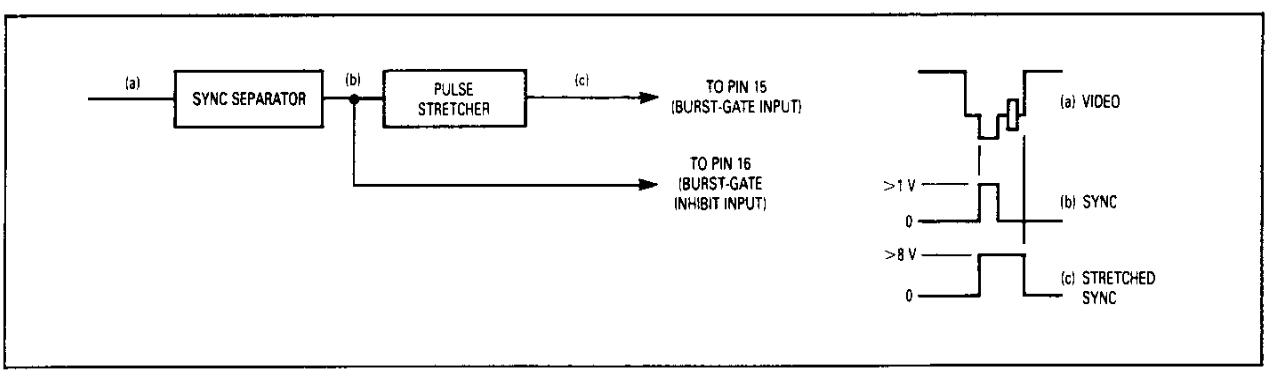


Figure 5. Alternate Method of Gating from Video

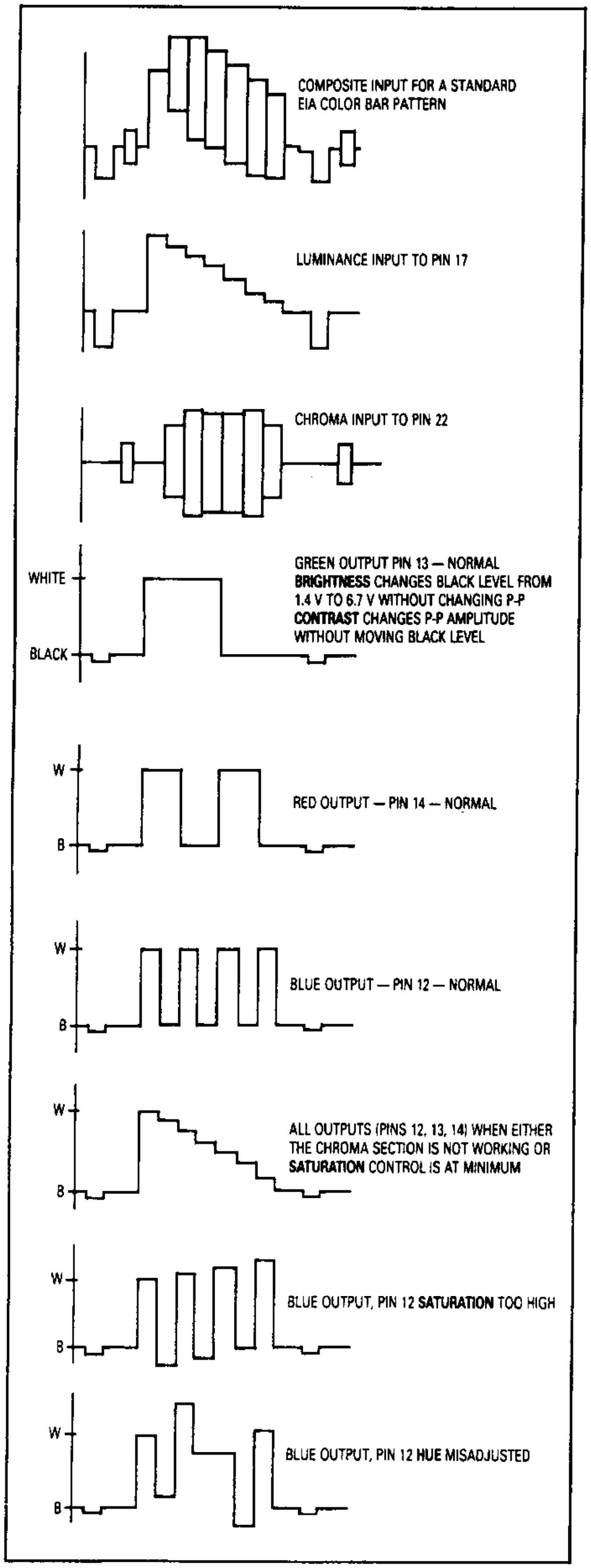


Figure 6. Some Normal and Other Waveforms

THE CHROMA PATH

The chroma input is derived from the composite input by a simple 3.58 MHz single-tuned bandpass circuit with about ±0.5 MHz (6 dB) bandwidth. The chroma portion of a color bar pattern should look like Figure 7. The circuit components recommended in our application circuit should yield about 100 mV_{pp} of burst at Pin 22, but anything from 10–200 mV_{pp} will work. The output of the chroma IF is at Pin 24, where the burst should be about 150 mV_{pp}. There may or may not be chroma present, depending on the **contrast** and **saturation** control settings. (Both controls have exactly the same effect at Pin 24, changing the picture chroma amplitude between the burst pulses.)

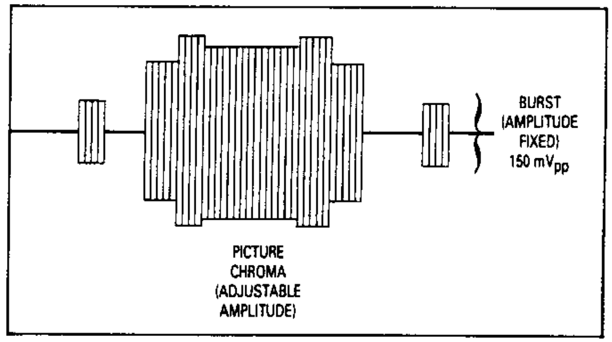


Figure 7. Chroma IF Output, Pin 24

Troubleshooting note: If there is 1.5 V_{pp} of burst at Pin 24, the burst-gating pulse is either too small or incorrectly positioned in time.

The chroma IF output from Pin 24 is coupled to the chroma demodulators, Pins 4 and 5 by a small capacitor. (Note: 100 pF performs better than the 1.0 nF on the data sheet; it reduces luminance component feedthrough.) Tweaking of demodulator balance to reduce residual chroma subcarrier in the outputs can be done at Pins 4 and 5 by the trimmer technique shown in Figure 8. This is a fine tuning which is usually not needed, but is available for the demanding application.

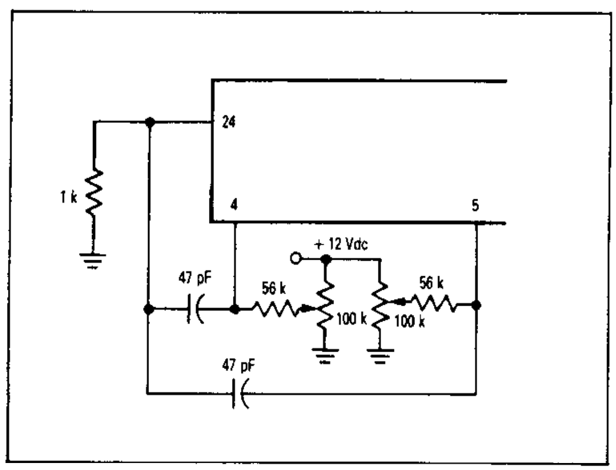


Figure 8. Optional Tweak of Demodulator Balance

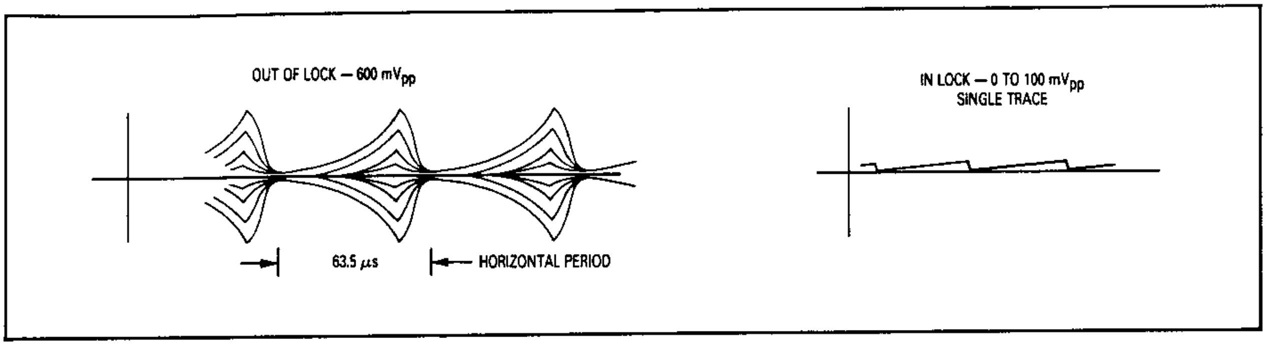


Figure 9. VCO Lock — Voltage at Pin 7

COLOR LOCKUP

If the required chroma is present at Pins 4, 5 (same as Pin 24), and if the oscillator is known to be running, then lockup is just a matter of adjusting the trimmer on Pin 9. As noted earlier, the scope probe cannot be put on the oscillator for this adjustment. Instead, put the scope on the AFC filter, Pin 7. Waveforms as shown in Figure 9 will be observed as the trimmer is adjusted.

Lock-in range is about 18–22 pF with the typical socket and PC board and ordinary (Radio Shack) 3.58 MHz TV crystal.

BUFFERING THE OUTPUTS

In order to be able to drive a cable, it is necessary to provide an output amplifier. The design shown in Figure 10 has two additional benefits:

1. It provides an opportunity to reduce the residual 2nd harmonic of the color subcarrier (7.16 MHz) by means of a trap, and
2. It reduces the DC level another 0.7 Vdc at the emitter of the 2N4401, and an additional 2:1 reduction due to the 75 Ω series R into the 75 Ω cable. Therefore, the black level into the cable can be as low as 0.35 V, for the minimum brightness control setting.

MISCELLANEOUS GREMLINS

It has been reported from the field that the internally supplied NTSC mode switch current (I3 in Figure 12 of the data sheet) is occasionally insufficient. This is characterized by a decoder which intermittently decodes and then "color kills." In the killed mode, Pin 3 is above 1.5 V and Pin 2 is below 0.7 V, which holds the **saturation** control low (off). This can be fixed by putting 22 k from Pin 3 to V_{CC}. This supplies additional current into Pin 3, causing an internal latch to pull Pin 3 low (have faith), and returns Pin 2 to an open state so it can be varied by the **Saturation** control.

SUMMARY

The TDA3330 has a wide range of functional capability with relatively simple application circuitry (once understood). It is hoped that this paper will assist users in becoming familiar and satisfied with it.

APPENDIX

Initial Setup Sequence for TDA3330 Evaluation Board

After connecting a Composite Video Signal In and connecting the Sync, Red, Green and Blue outputs to an appropriate RGB monitor, follow the subsequent steps, in order, to adjust the 11 variable components to optimize performance of the RGB decoder:

1. Look at the signal out of the collector of the 2N4402 transistor. Adjust POT #9 so that the Composite Video Signal at this point is 1.0 V_{pp}.
2. Set POTS #2 and 3 to approximately the middle of their values (i.e., 50 kΩ). This helps in making the subsequent adjustments.
3. POT #7 sets the Burst-Gate Width and POT #8 sets the Burst-Gate Delay relative to the Video Sync Signal. Use a dual input oscilloscope and look at the Video In signal and the Burst-Gate Signal at Pin 15 of the TDA3330. Adjust POT #8 so that the Burst-Gate Signal begins ~250 ns after the Sync Signal ends. Next adjust POT #7 so that the width of the Burst-Gate Signal is 3.5–4 µs. Note: See Figure 3.
4. Put the oscilloscope probe on Pin 7 of the TDA3330. Adjust the Variable Capacitor, connected to Pin 9, until the VCO is In Lock. This will happen when the trace signal drops from ~650 mV_{pp} to less than 100 mV_{pp}. Try to make the signal as small as possible, possibly down to dc. (Make tilt flat) Note: See Figure 9.
5. Put the oscilloscope probe on Pin 17 of the TDA3330. Adjust the 10 µH Variable Inductor to minimize Chroma Signal Feedthrough.
6. In order to fine tune chroma demodulator balance, remove the chroma signal from the Composite Video Signal In (or, alternatively, turn the Saturation POT all the way down). Look at the Red output on the oscilloscope and adjust POT #2 to minimize subcarrier from the V Signal (i.e., R-Y) input. Next look at the Blue signal and adjust POT #3 to minimize subcarrier from the U signal (i.e., B-Y) input.
7. POTS #1, 4, 5 and 6 can next be adjusted to optimize picture color quality. Suggestion for doing this is to set Saturation (POT #1) and Brightness (POT #5) to middle and then adjust Contrast (POT #4 and Hue POT #6) till picture colors are approximately right. Next adjust POT's 1 and 5. Repeat the above sequence until satisfied with color quality of picture.

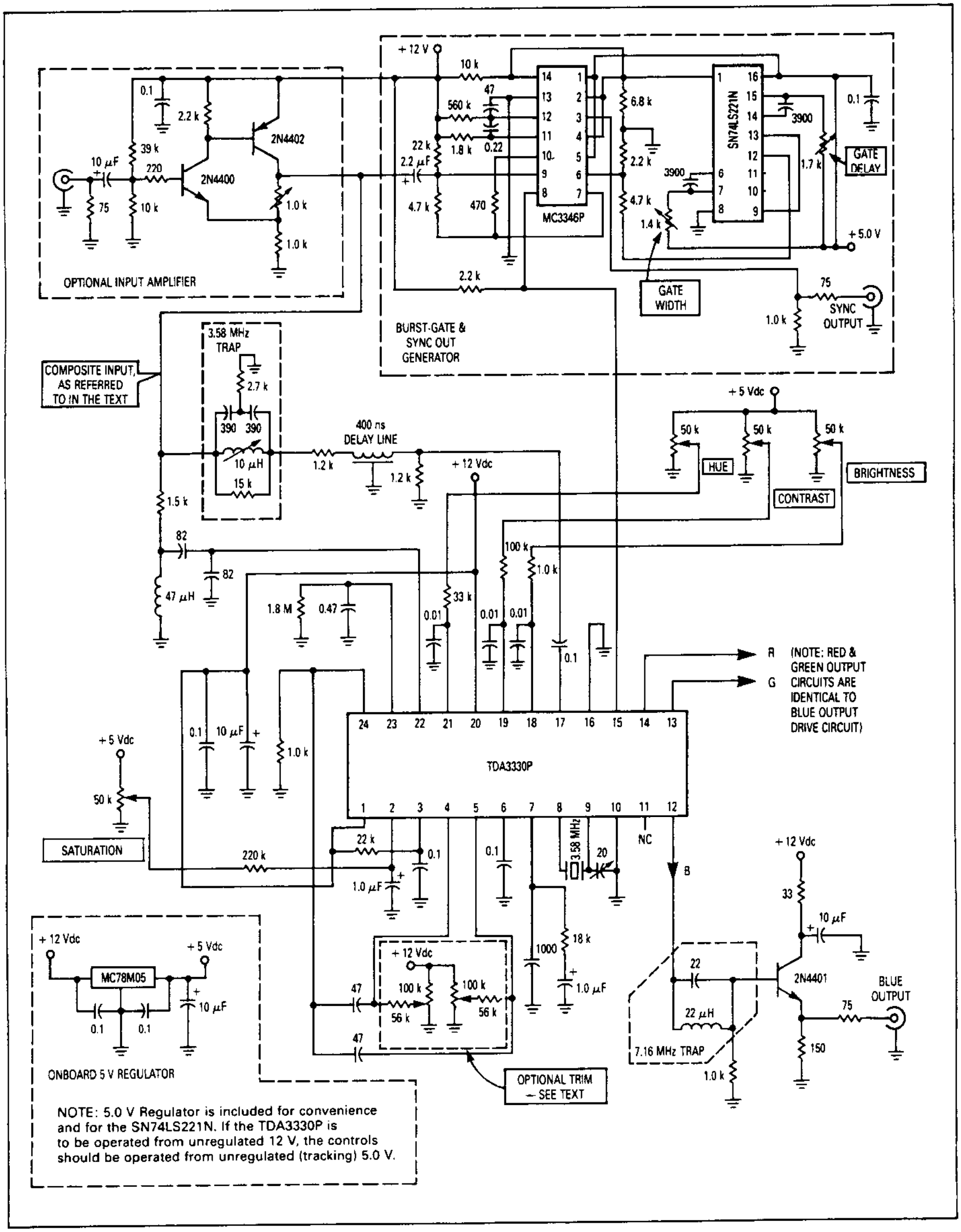
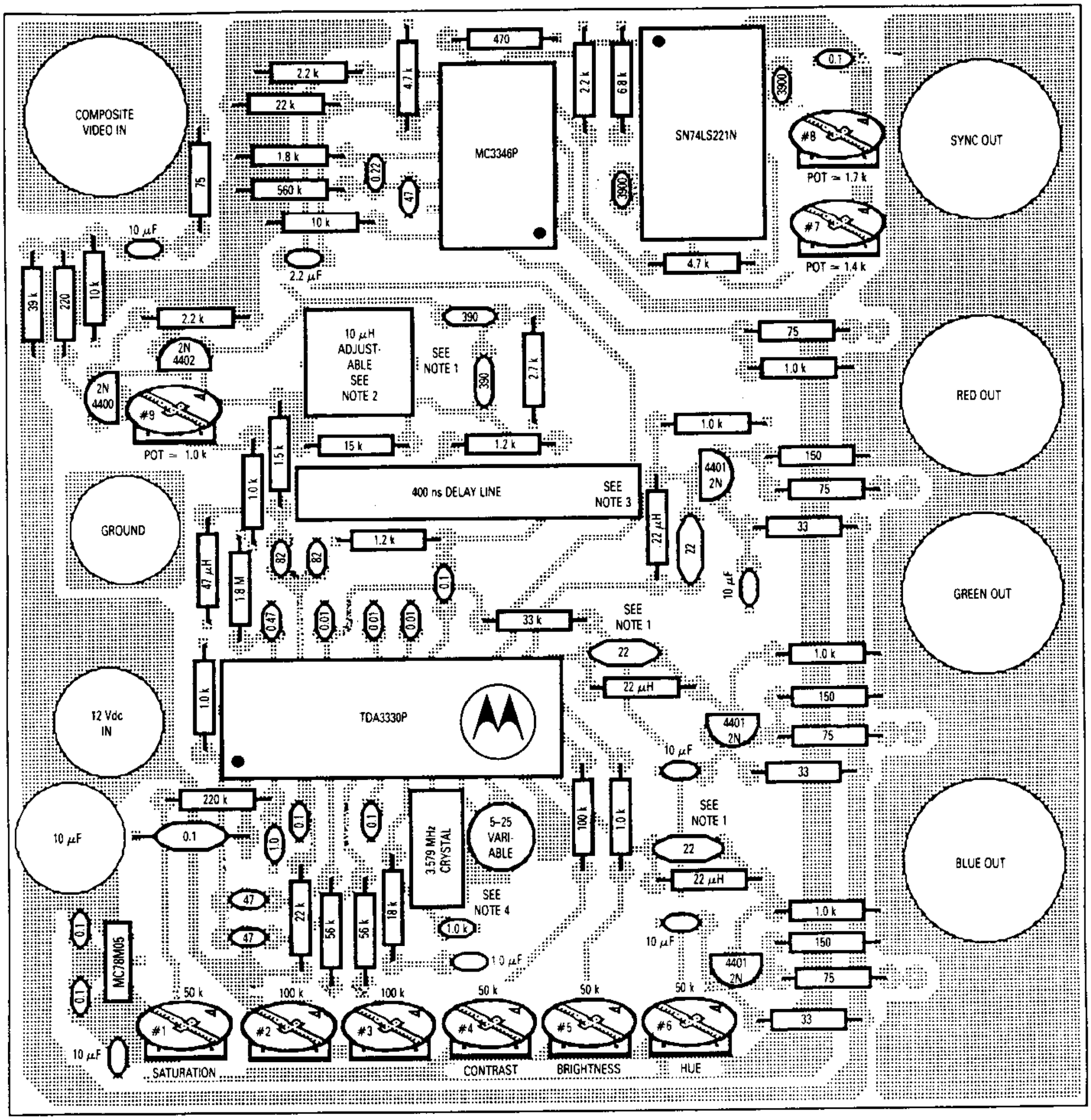


Figure 10. TDA3330 RGB NTSC Decoder Circuit



NOTES: 1. For the 390 pF and the 22 pF capacitors in the 3.58 MHz and in the 7.16 MHz traps, silver mica capacitors should be used for better trap performance.
2. The board layout is for Toko part #BTKANS-9439HM.
3. Board layout will accommodate a Toko or a TDK 400 ns delay line.
4. A 3.58 MHz crystal available through Radio Shack was used.

Figure 11a. TDA3330P RGB NTSC Decoder Evaluation Board, Component Layout

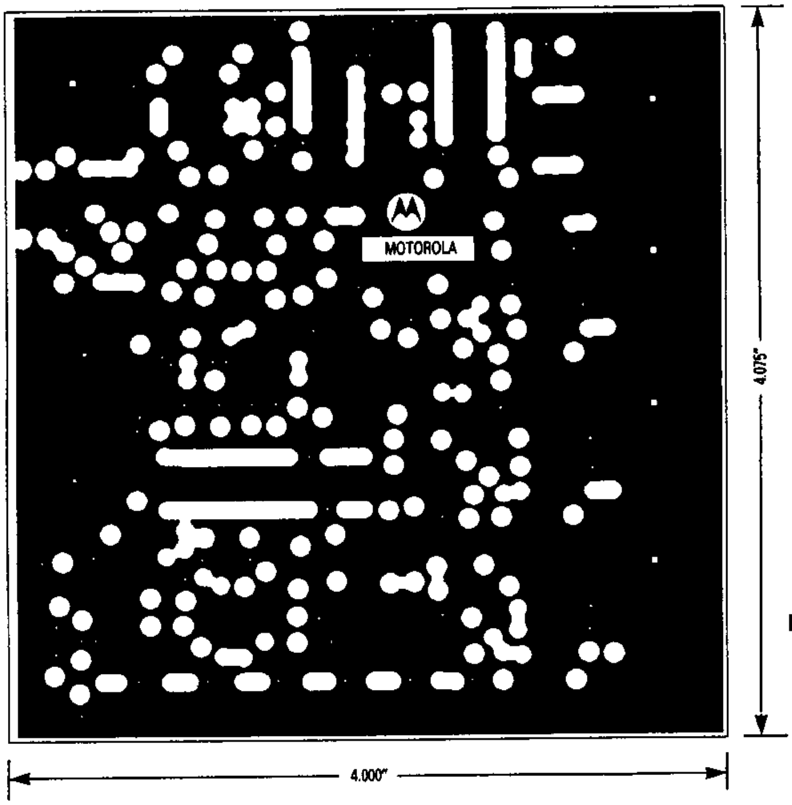


Figure 11b. TDA3330 RGB NTSC Decoder Evaluation Board, Component Side

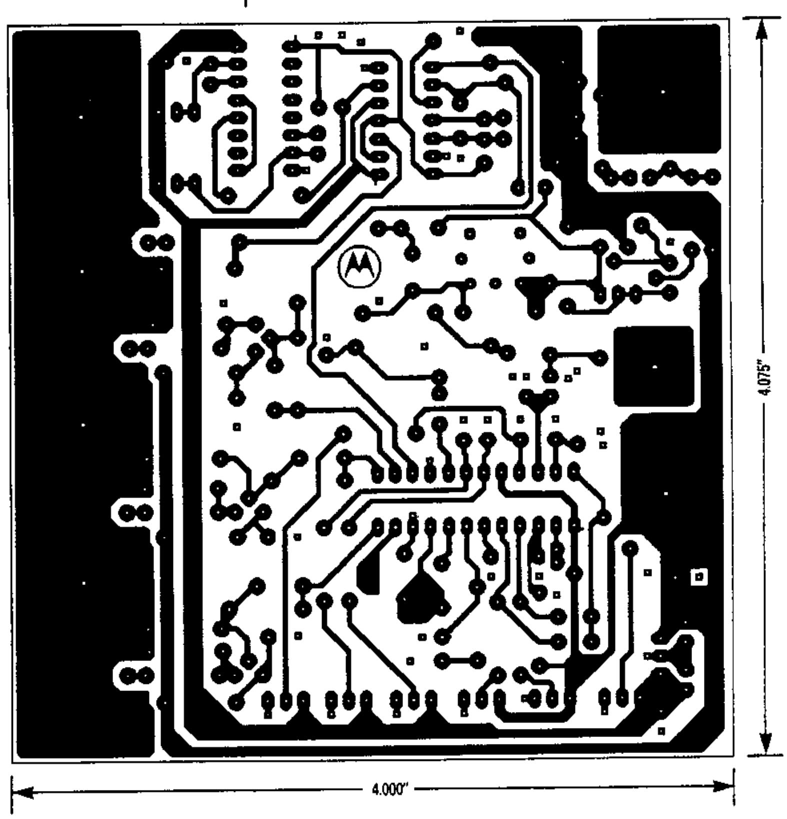


Figure 11c. TDA3330P RGB NTSC Decoder Evaluation Board, Bottomside

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