

# Dual Picoampere Input Current Bipolar Op Amp

**AD706** 

#### **FEATURES**

HIGH DC PRECISION
50 μV max Offset Voltage
0.6 μV/°C max Offset Drift
110 pA max Input Bias Current

**LOW NOISE** 

0.5  $\mu$ V p-p Voltage Noise, 0.1 Hz to 10 Hz

**LOW POWER** 

750 µA Supply Current
Available in 8-Pin Plastic Mini-DIP, Hermetic Cerdip and
Surface Mount (SOIC) Packages
Available in Tape and Reel in Accordance with
EIA-481A Standard
Single Version: AD705, Quad Version: AD704

PRIMARY APPLICATIONS
Low Frequency Active Filters
Precision Instrumentation
Precision Integrators

#### PRODUCT DESCRIPTION

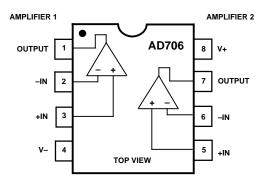
The AD706 is a dual, low power, bipolar op amp that has the low input bias current of a BiFET amplifier but which offers a significantly lower  $I_B$  drift over temperature. It utilizes superbeta bipolar input transistors to achieve picoampere input bias current levels (similar to FET input amplifiers at room temperature), while its  $I_B$  typically only increases by 5× at 125°C (unlike a BiFET amp, for which  $I_B$  doubles every  $10^{\circ} C$  for a  $1000 \times$  increase at  $125^{\circ} C$ ). The AD706 also achieves the microvolt offset voltage and low noise characteristics of a precision bipolar input amplifier.

Since it has only 1/20 the input bias current of an OP07, the AD706 does not require the commonly used "balancing" resistor. Furthermore, the current noise is 1/5 that of the OP07 which makes this amplifier usable with much higher source impedances. At 1/6 the supply current (per amplifier) of the OP07, the AD706 is better suited for today's higher density boards.

The AD706 is an excellent choice for use in low frequency active filters in 12- and 14-bit data acquisition systems, in precision instrumentation, and as a high quality integrator. The AD706 is internally compensated for unity gain and is available in five performance grades. The AD706J and AD706K are rated over the commercial temperature range of  $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ . The AD706A and AD706B are rated over the industrial temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

#### **CONNECTION DIAGRAM**

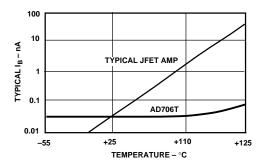
Plastic Mini-DIP (N) Cerdip (Q) and Plastic SOIC (R) Packages



The AD706 is offered in three varieties of an 8-pin package: plastic mini-DIP, hermetic cerdip and surface mount (SOIC). "J" grade chips are also available.

#### PRODUCT HIGHLIGHTS

- 1. The AD706 is a dual low drift op amp that offers BiFET level input bias currents, yet has the low  $I_B$  drift of a bipolar amplifier. It may be used in circuits using dual op amps such as the LT1024.
- 2. The AD706 provides both low drift and high dc precision.
- 3. The AD706 can be used in applications where a chopper amplifier would normally be required but without the chopper's inherent noise.



#### REV. B

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.

© Analog Devices, Inc., 1994

# $\label{eq:AD706-SPECIFICATIONS} \textbf{(@ $T_A = +25^{\circ}$C$, $V_{CM} = 0$ V and $\pm 15$ V dc, unless otherwise noted)}$

_		AD706J/A	AD706K/B	
Parameter	Conditions	Min Typ Max	Min Typ Max	Units
INPUT OFFSET VOLTAGE				
Initial Offset		30 100	10 50	μV
Offset	$T_{MIN}$ to $T_{MAX}$	40 150	25 100	μV
vs. Temp, Average TC		0.2 1.5	0.2 0.6	μV/°C
vs. Supply (PSRR)	$V_S = \pm 2 \text{ V to } \pm 18 \text{ V}$	110 132	112 132	dB
$T_{MIN}$ to $T_{MAX}$	$V_S = \pm 2.5 \text{ V to } \pm 18 \text{ V}$	106 126	108 126	dB
Long Term Stability		0.3	0.3	μV/month
INPUT BIAS CURRENT <sup>1</sup>				<i>p</i>
INPUT BIAS CURRENT	$V_{CM} = 0 V$	50 200	30 110	- 1
				pA
T A TC	$V_{CM} = \pm 13.5 \text{ V}$	250	160	pA
vs. Temp, Average TC	W - 0 W	0.3	0.2	pA/°C
$T_{MIN}$ to $T_{MAX}$	$V_{CM} = 0 V$	300	200	pA
$T_{MIN}$ to $T_{MAX}$	$V_{CM} = \pm 13.5 \text{ V}$	400	300	pA
INPUT OFFSET CURRENT	$V_{CM} = 0 V$	30 150	30 100	pA
	$V_{CM} = \pm 13.5 \text{ V}$	250	200	pA
vs. Temp, Average TC	G.11	0.6	0.4	pA/°C
$T_{MIN}$ to $T_{MAX}$	$V_{CM} = 0 \text{ V}$	80 250	80 200	pA
$T_{MIN}$ to $T_{MAX}$	$V_{CM} = \pm 13.5 \text{ V}$	80 350	80 300	pA
	· Gwi ==3.5		10000	F
MATCHING CHARACTERISTICS		1.50		
Offset Voltage		150	75	μV
. Di C 2	$T_{MIN}$ to $T_{MAX}$	250	150	μV
Input Bias Current <sup>2</sup>		300	150	pA
	${ m T_{MIN}}$ to ${ m T_{MAX}}$	500	250	pA
Common-Mode Rejection		106	110	dB
	$T_{MIN}$ to $T_{MAX}$	106	108	dB
Power Supply Rejection		106	110	dB
	$T_{MIN}$ to $T_{MAX}$	104	106	dB
Crosstalk	@ f = 10 Hz			
(Figure 19a)	$R_L = 2 k\Omega$	150	150	dB
FREQUENCY RESPONSE	E .			
=				
Unity Gain Crossover		0.0		3.477
Frequency		0.8	0.8	MHz
Slew Rate	G = -1	0.15	0.15	V/µs
	T <sub>MIN</sub> to T <sub>MAX</sub>	0.15	0.15	V/µs
INPUT IMPEDANCE				
Differential		40  2	40  2	$M\Omega    pF$
Common Mode		300  2	300  2	GΩ∥pF
INPUT VOLTAGE RANGE				- 112
		112.5	112.5	***
Common-Mode Voltage		±13.5 ±14	±13.5 ±14	V
Common-Mode Rejection				
Ratio	$V_{CM} = \pm 13.5 \text{ V}$	110 132	114 132	dB
	$T_{ m MIN}$ to $T_{ m MAX}$	108 128	108 128	dB
INPUT CURRENT NOISE	0.1 Hz to 10 Hz	3	3	pA p-p
	f = 10 Hz	50	50	fA/√ <del>Hz</del>
INPUT VOLTAGE NOISE	0.1 Hz to 10 Hz	0.5	0.5 1.0	
INFUT VOLTAGE NOISE	f = 10 Hz			$\mu V p-p$ $nV/\sqrt{Hz}$
		17	17	
	f = 1 kHz	15 22	15 22	nV/√Hz
OPEN-LOOP GAIN	$V_O = \pm 12 \text{ V}$			
	$R_{LOAD} = 10 \text{ k}\Omega$	200 2000	400 2000	V/mV
	$T_{MIN}$ to $T_{MAX}$	150 1500	300 1500	V/mV
	$V_O = \pm 10 \text{ V}$			
	$R_{LOAD} = 2 k\Omega$	200 1000	300 1000	V/mV
	$T_{MIN}$ to $T_{MAX}$	150 1000	200 1000	V/mV
OUTDIT CHARACTERISTICS	WILLY WILLY			
OUTPUT CHARACTERISTICS	P - 1010	112	112	
Voltage Swing	$R_{LOAD} = 10 \text{ k}\Omega$	±13 ±14	±13 ±14	V
_	$T_{MIN}$ to $T_{MAX}$	±13 ±14	±13 ±14	V
Current	Short Circuit	±15	±15	mA
Capacitive Load				
Drive Capability	Gain = +1	10,000	10,000	pF

-2-

			AD706J/	A	AD706K/B			
Parameter	Conditions	Min	Typ	Max	Min	Typ	Max	Units
POWER SUPPLY								
Rated Performance			±15			±15		V
Operating Range		±2.0		$\pm 18$	±2.0		±18	V
Quiescent Current, Total			0.75	1.2		0.75	1.2	mA
	$T_{ m MIN}$ to $T_{ m MAX}$		0.8	1.4		0.8	1.4	mA
TRANSISTOR COUNT	# of Transistors		90			90		

#### NOTES

CMRR match is the difference between  $\frac{\Delta V_{OS} \# 1}{\Delta V_{CM}}$  for amplifier #1 and  $\frac{\Delta V_{OS} \# 2}{\Delta V_{CM}}$  for amplifier #2 expressed in dB.

PSRR match is the difference between  $\frac{\Delta V_{OS} \# 1}{\Delta V_{SUPPLY}}$  for amplifier #1 and  $\frac{\Delta V_{OS} \# 2}{\Delta V_{SUPPLY}}$  for amplifier #2 expressed in dB.

All min and max specifications are guaranteed.

Specifications subject to change without notice.

#### ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

Supply Voltage
Internal Power Dissipation
(Total: Both Amplifiers) <sup>2</sup> 650 mW
Input Voltage
Differential Input Voltage <sup>3</sup> +0.7 Volts
Output Short Circuit Duration Indefinite
Storage Temperature Range (Q)65°C to +150°C
Storage Temperature Range (N, R)65°C to +125°C
Operating Temperature Range
AD706J/K 0°C to +70°C
AD706A/B40°C to +85°C
Lead Temperature (Soldering 10 secs) +300°C
NOTES

<sup>1</sup>Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

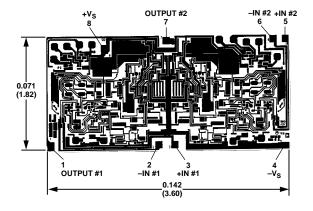
#### **ORDERING GUIDE**

Model	Temperature Range	Description	Package Option*
AD706JN	0°C to +70°C	Plastic DIP	N-8
AD706KN	$0^{\circ}$ C to $+70^{\circ}$ C	Plastic DIP	N-8
AD706JR	$0^{\circ}$ C to $+70^{\circ}$ C	SOIC	R-8
AD706JR-REEL	$0^{\circ}$ C to $+70^{\circ}$ C	Tape & Reel	
AD706AQ	-40°C to $+85$ °C	Cerdip	Q-8
AD706BQ	$-40^{\circ}$ C to $+85^{\circ}$ C	Cerdip	Q-8
AD706AR	$-40^{\circ}$ C to $+85^{\circ}$ C	SOIC	R-8
AD706AR-REEL	$-40^{\circ}$ C to $+85^{\circ}$ C	Tape & Reel	

<sup>\*</sup>N = Plastic DIP; Q = Cerdip, R = Small Outline Package.

#### METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm). Contact factory for latest dimensions.



#### CAUTION -

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD706 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



<sup>&</sup>lt;sup>1</sup>Bias current specifications are guaranteed maximum at either input.

<sup>&</sup>lt;sup>2</sup>Input bias current match is the difference between corresponding inputs (I<sub>B</sub> of –IN of Amplifier #1 minus I<sub>B</sub> of –IN of Amplifier #2).

<sup>&</sup>lt;sup>2</sup>Specification is for device in free air:

<sup>8-</sup>Pin Plastic Package:  $\theta_{JA} = 100^{\circ}$ C/Watt 8-Pin Cerdip Package:  $\theta_{JA} = 110^{\circ}$ C/Watt

<sup>8-</sup>Pin Small Outline Package:  $\theta_{JA} = 155^{\circ}\text{C/Watt}$ 

<sup>&</sup>lt;sup>3</sup>The input pins of this amplifier are protected by back-to-back diodes. If the differential voltage exceeds  $\pm 0.7$  volts, external series protection resistors should be added to limit the input current to less than 25 mA.

## AD706—Typical Characteristics(@ $+25^{\circ}$ C, $V_s = \pm 15$ V, unless otherwise noted)

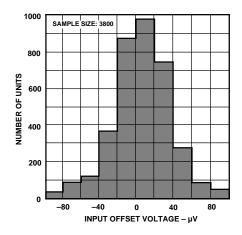


Figure 1. Typical Distribution of Input Offset Voltage

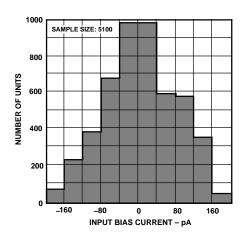


Figure 2. Typical Distribution of Input Bias Current

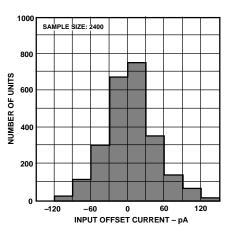


Figure 3. Typical Distribution of Input Offset Current

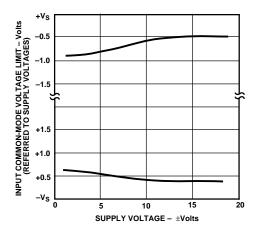


Figure 4. Input Common-Mode Voltage Range vs. Supply Voltage

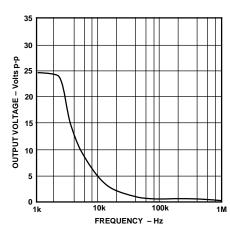


Figure 5. Large Signal Frequency Response

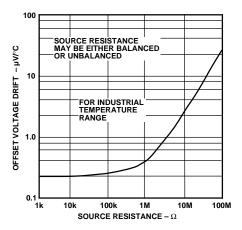


Figure 6. Offset Voltage Drift vs. Source Resistance

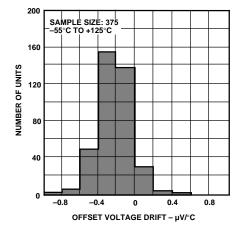


Figure 7. Typical Distribution of Offset Voltage Drift

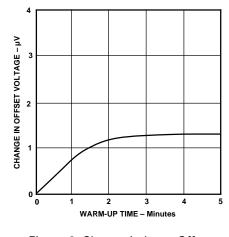


Figure 8. Change in Input Offset Voltage vs. Warm-Up Time

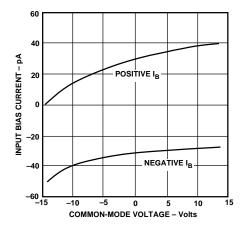


Figure 9. Input Bias Current vs. Common-Mode Voltage

-4- REV. B

### **AD706**

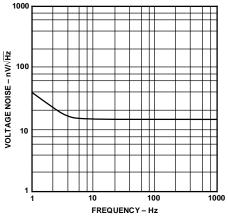


Figure 10. Input Noise Voltage Spectral Density

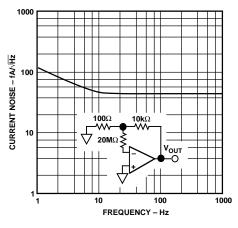


Figure 11. Input Noise Current Spectral Density

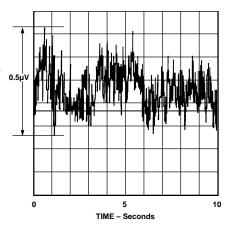


Figure 12. 0.1 Hz to 10 Hz Noise Voltage

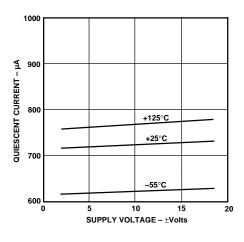


Figure 13. Quiescent Supply Current vs. Supply Voltage

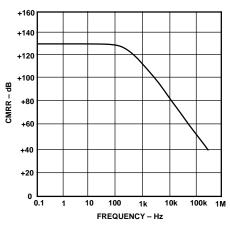


Figure 14. Common-Mode Rejection Ratio vs. Frequency

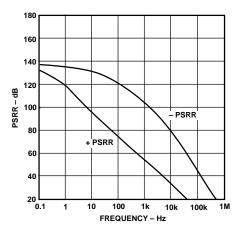


Figure 15. Power Supply Rejection Ratio vs. Frequency

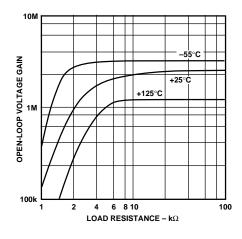


Figure 16. Open-Loop Gain vs. Load Resistance vs. Temperature

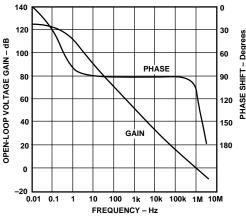


Figure 17. Open-Loop Gain and Phase Shift vs. Frequency

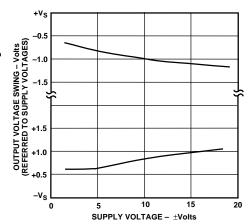


Figure 18. Output Voltage Swing vs. Supply Voltage

REV. B \_5\_

## **AD706**

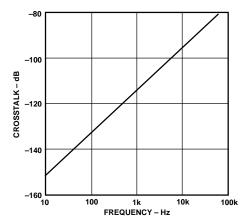


Figure 19a. Crosstalk vs. Frequency

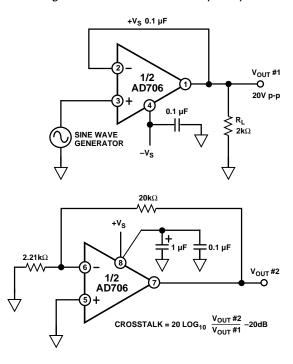


Figure 19b. Crosstalk Test Circuit

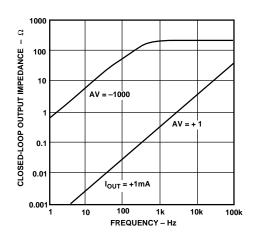


Figure 20. Magnitude of Closed-Loop Output Impedance vs. Frequency

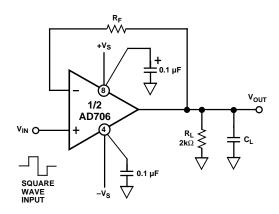


Figure 21a. Unity Gain Follower (For Large Signal Applications, Resistor  $R_F$  Limits the Current Through the Input Protection Diodes)

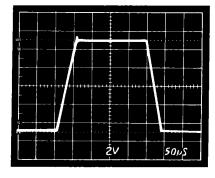


Figure 21b. Unity Gain Follower Large Signal Pulse Response,  $R_F = 10 \text{ k}\Omega$ ,  $C_L = 1,000 \text{ pF}$ 

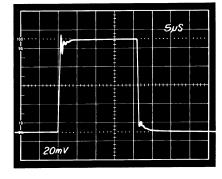


Figure 21c. Unity Gain Follower Small Signal Pulse Response,  $R_F = 0 \Omega$ ,  $C_L = 100 pF$ 

-6-

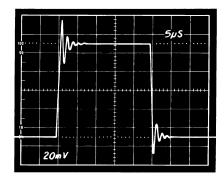


Figure 21d. Unity Gain Follower Small Signal Pulse Response,  $R_F = 0 \Omega$ ,  $C_L = 1000 pF$ 

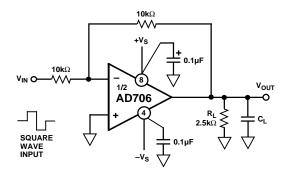
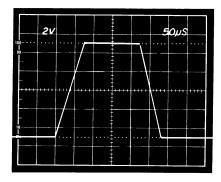


Figure 22a. Unity Gain Inverter Connection



20mV

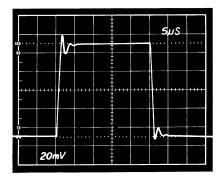


Figure 22b. Unity Gain Inverter Large Signal Pulse Response,  $C_L = 1,000 \text{ pF}$ 

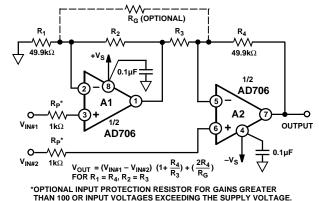
Figure 22c. Unity Gain Inverter Small Signal Pulse Response,  $C_L = 100 \text{ pF}$ 

Figure 22d. Unity Gain Inverter Small Signal Pulse Response,  $C_L = 1000 \text{ pF}$ 

Figure 23 shows an in-amp circuit that has the obvious advantage of requiring only one AD706 rather than three op amps, with subsequent savings in cost and power consumption. The transfer function of this circuit (without  $R_G$ ) is:

$$V_{OUT} = (V_{IN\#1} - V_{IN\#2}) \left( 1 + \frac{R_4}{R_3} \right)$$
  
for  $R_1 = R_4$  and  $R_2 = R_3$ 

Input resistance is high, thus permitting the signal source to have an unbalanced output impedance.



THAN 100 OR INPUT VOLTAGES EXCEEDING THE SUPPLY VOLTAGE

Figure 23. A Two Op-Amp Instrumentation Amplifier Furthermore, the circuit gain may be fine trimmed using an optional trim resistor, R<sub>G</sub>. Like the three op-amp circuit, CMR

increases with gain, once initial trimming is accomplished—but CMR is still dependent upon the ratio matching of Resistors R<sub>1</sub> through R<sub>4</sub>. Resistor values for this circuit using the optional gain resistor, R<sub>G</sub>, can be calculated using:

$$R_1 = R_4 = 49.9 \ k\Omega$$

$$R_2 = R_3 = \frac{49.9 \ k\Omega}{0.9 \ G - 1}$$

$$R_G = \frac{99.8 \ k\Omega}{0.06 \ G}$$

where G = Desired Circuit Gain

Table I provides practical 1% resistance values. (Note that without resistor  $R_G$ ,  $R_2$  and  $R_3$  = 49.9 k $\Omega$ /G-1.)

Table I. Operating Gains of Amplifiers A1 and A2 and Practical 1% Resistor Values for the Circuit of Figure 23

Circuit Gain	Gain of A1	Gain of A2	$R_2, R_3$	R <sub>1</sub> , R <sub>4</sub>
1.10	11.00	1.10	499 kΩ	49.9 kΩ
1.33	4.01	1.33	150 kΩ	49.9 kΩ
1.50	3.00	1.50	100 kΩ	49.9 kΩ
2.00	2.00	2.00	49.9 kΩ	49.9 kΩ
10.1	1.11	10.10	5.49 kΩ	49.9 kΩ
101.0	1.01	101.0	$499 \Omega$	49.9 kΩ
1001	1.001	1001	$49.9~\Omega$	49.9 kΩ

For a much more comprehensive discussion of in-amp applications, refer to the *Instrumentation Amplifier Applications Guide*—available free from Analog Devices, Inc.

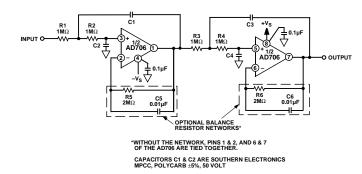


Figure 24. A 1 Hz, 4-Pole Active Filter

#### A 1 Hz, 4-Pole, Active Filter

**AD706** 

Figure 24 shows the AD706 in an active filter application. An important characteristic of the AD706 is that both the input bias current, input offset current and their drift remain low over most of the op amp's rated temperature range. Therefore, for most applications, there is no need to use the normal balancing resistor. Adding the balancing resistor enhances performance at high temperatures, as shown by Figure 25.

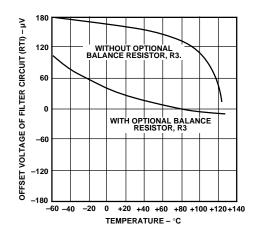


Figure 25.  $V_{OS}$  vs. Temperature Performance of the 1 Hz Filter

Table II. 1 Hz, 4-Pole, Low Pass Filter Recommended Component Values

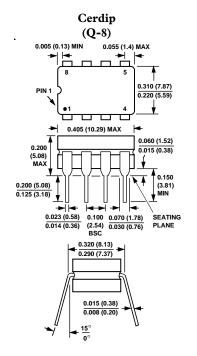
Desired Low Pass Response	Section 1 Frequency (Hz)	Q	Section 2 Frequency (Hz)	Q	C1 (μ <b>F</b> )	C2 (µF)	C3 (µF)	C4 (μ <b>F</b> )
Bessel	1.43	0.522	1.60	0.806	0.116	0.107	0.160	0.0616
Butterworth	1.00	0.541	1.00	1.31	0.172	0.147	0.416	0.0609
0.1 dB Chebychev	0.648	0.619	0.948	2.18	0.304	0.198	0.733	0.0385
0.2 dB Chebychev	0.603	0.646	0.941	2.44	0.341	0.204	0.823	0.0347
0.5 dB Chebychev	0.540	0.705	0.932	2.94	0.416	0.209	1.00	0.0290
1.0 dB Chebychev	0.492	0.785	0.925	3.56	0.508	0.206	1.23	0.0242

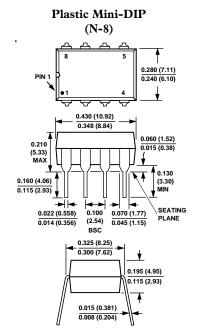
#### NOTE

Specified Values are for a -3 dB point of 1.0 Hz. For other frequencies simply scale capacitors C1 through C4 directly, i.e.: for 3 Hz Bessel response, C1 =  $0.0387 \mu F$ , C2 =  $0.0357 \mu F$ , C3 =  $0.0533 \mu F$ , C4 =  $0.0205 \mu F$ .

#### **OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).





-8-

