DATA SHEET

VES1993
Single Chip Satellite Channel Receiver

Product specification
File under Integrated Circuits, IC02

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Philips
Semiconductors

PHILIPS

Single Chip Satellite Channel Receiver VES1993

FEATURES

- DSS and DVB-S compatible single chip demodulator & forward error correction.
- Dual 6-bit ADC on chip.
- PLL for crystal frequency multiplication.
- Variable rate BPSK/QPSK coherent demodulator.
- Modulation rate from 1 to 45MBaud.
- Automatic Gain Control output.
- Digital symbol timing recovery :
  Acquisition range up to ±240ppm
- Digital carrier recovery :
  Acquisition range up to ±12% of symbol rate
- Half Nyquist baseband filters on chip
  roll-off = 0.35 for DVB and 0.2 for DSS
- Channel quality estimation.
- Viterbi decoder :
  Supported rates : from 1/2 to 8/9.
  Constraint length K = 7
  with G1 = 171_8 G2 = 133_8
  VBER measurement provided.
- Convolutional deinterleaver and Reed Solomon decoder according to DVB and DSS specifications.
- Automatic Frame Synchronization.
- Selectable DVB-S descrambling.
- I2C bus interface.
- 100-pin MQFP package.
- CMOS technology (0.35 µm 3.3V).

APPLICATIONS

- DSS receivers.
- DVB-S receivers (ETS 300-421).
- Direct Broadcast Satellite (DBS).

DESCRIPTION

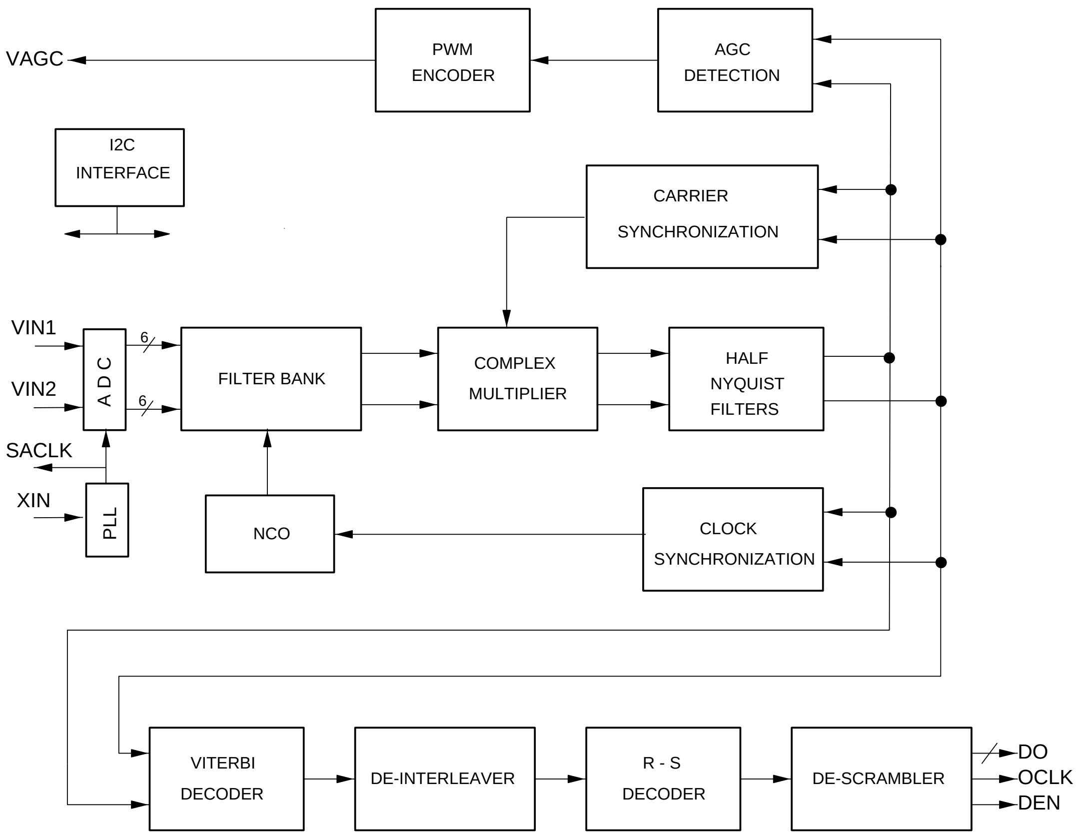
The VES 1993 is a single-chip channel receiver for satellite television reception which matches both DSS and DVB-S standards. The device contains a dual 6-bit flash analog to digital converter, variable rate BPSK/QPSK coherent demodulator and Forward Error Correction functions.The ADCs directly interface with I and Q analog baseband signals. After A to D conversion, the VES 1993 implements a bank of cascadable filters as well as antialias and half-Nyquist filters. Analog AGC signal is generated by an amplitude estimation function. The VES 1993 performs clock recovery at twice the Baud rate and achieves coherent demodulation without any feedback to the local oscillator. Forward Error Correction is built around two error correcting codes : a Reed-Solomon (outer code), and a Viterbi decoder (inner code). The Reed-Solomon decoder corrects up to 8 erroneous bytes among the N bytes of one data packet. Convolutional deinterleaver is located between the Viterbi output and the R.S. decoder input. De-interleaver and R.S. decoder are automatically synchronized thanks to the frame synchronisation algorithm which uses the sync pattern present in each packet. The VES 1993 is controlled via an I2C bus interface. The circuit operates up to 91MHz and can process variable modulation rates, up to 45Mbaud.

The VES 1993 provides an interrupt line which can be programmed on either events or timing information.

Designed in 0.35 CMOS technology and housed in a 100-MQFP package, the VES 1993 operates over the commercial temperature range.

FIGURE 1. BLOCK DIAGRAM

1.1 WITH COMPLEX MULTIPLIER AFTER ANTI-ALIASING FILTERS (POSMUL=0) :



1.2 WITH COMPLEX MULTIPLIER BEFORE ANTI-ALIASING FILTERS (POSMUL=1) :

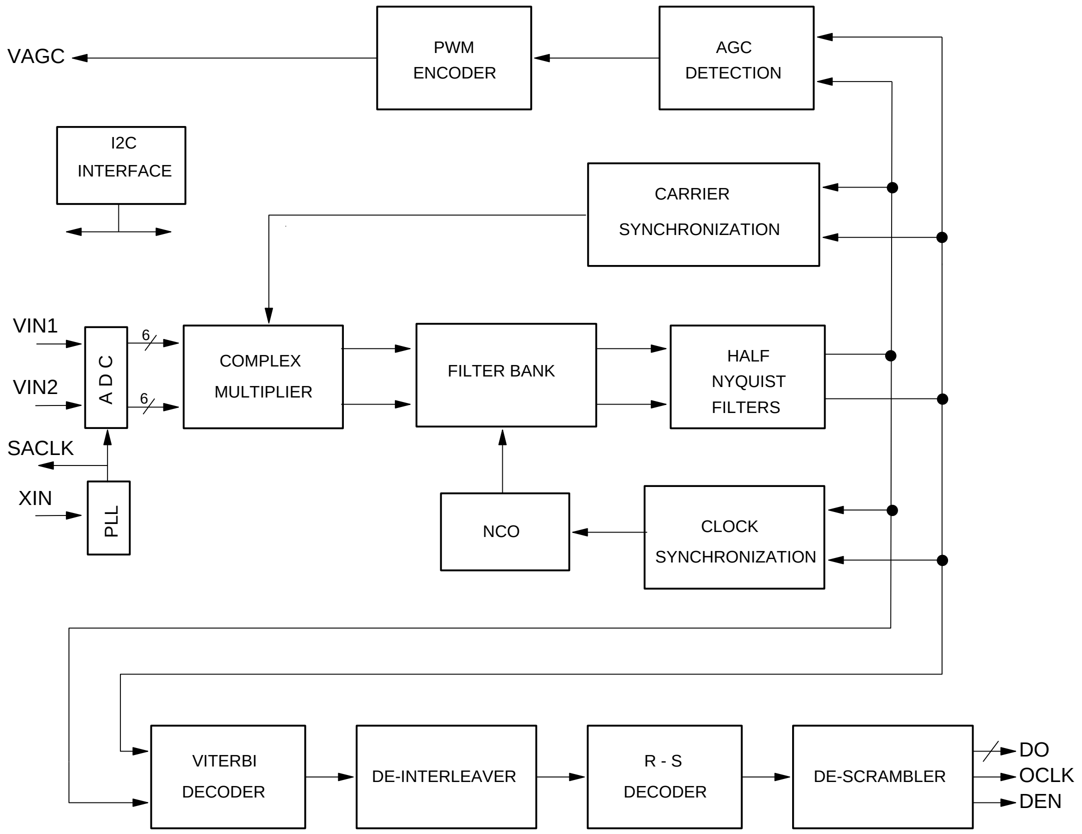


TABLE 1 : ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Unit
Ambient operating temperature (Ta)	0	70	°C
DC supply voltage	- 0.5	+4.1	V
DC input voltage	- 0.5	VDD + 0.5	V
DC input current		± 20	mA
Lead Temperature		+ 300	°C
Junction Temperature		+ 125	°C

Stresses above the absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

TABLE 2: RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VDD	Digital supply voltage	3.135	3.3	3.465	V	3.3V ±5%
VCC	5V supply voltage	4.75	5	5.25	V	pins 22 and 91
Ta	Operating temperature	0		70	° C	Ambient temperature
AVD	Analog supply voltage	3.135	3.3	3.465	V	pin 43
AVS	Analog ground		0		V	pin 44
VINDC	DC Analog Input	VREFN		VREFP	V	pins 41 and 45
VINAC	AC Analog Input		750		mVpp	pins 41 and 45
ZIN	Analog input impedance	10	100		Ohms	pins 41 and 45
VREFP	Top voltage reference		2.0		V	pin 46
VREFN	Bottom voltage reference		1.25		V	pin 42
XIN	Crystal frequency			93	MHz	
ZOE (1)	Zero Offset Error			10	mV	
DNL(2)	Differential Non Linearity		0.5	0.9	LSB	
INL(3)	Integral Non Linearity		0.8	1	LSB	
GE (4)	Gain Error			10	mV	
SINAD (5)	ADC signal to noise ratio		34		dB	@ 1MHz input signal and 92MHz sampling clock
THD(6)	Total Harmonic Distorsion		35		dB	
VIH(7)	High-level input voltage	2		VCC+0.3	V	TTL input
VIL	Low-level input voltage	-0.5		0.8	V	TTL input
VOH(8)	High-level output voltage	2.4			V	@IOH = -2mA to -4mA
VOL(8)	Low-level output voltage			0.4	V	@IOL = + 2 mA to +4mA
IDD	Supply current		8.5		mA/MBaud	@XIN = 91MHz
CIN	Input capacitance		15		pF	1MHz input to VSS
COUT	Output capacitance		15		pF	1MHz input to VSS

(1) Zero Offset Error : deviation of voltage input from ideal voltage to get the 00 code.
(2) Differential Non linearity : maximum deviation of the analog span of each output code from its ideal 1lsb value.
(3) Integral Non linearity : deviation of the ADC transfer curve from the ideal transfer curve, defined according to the best straight line fit method.
(4) Gain Error : Deviation of voltage input from ideal value to get the highest code.
(5) Signal-to-noise plus distortion ratio (SINAD) : ratio between the RMS magnitude of the fundamental input frequency to the RMS magnitude of all other A/D output signals.
(6) Total harmonic distortion (THD) : ratio of the RMS sum of all harmonics of the input signal (below one half of the sample rate) to the fundamental.
(7) All inputs are 5V tolerant.
(8) IOH, IOL = ±4mA only for pins : SACLK, OCLK, SDA, SCL_0, SDA_0.

FUNCTIONAL DESCRIPTION

- **PLL**
  The VES 1993 implements a PLL used as clock multiplier by 1, 2, 3, 4 or 6, so that the crystal can be low frequency.

- **DUAL 6-BIT ADC**
  The VES 1993 implements a dual 6-bit ADC. The architecture is a standard flash one based on 63 latched comparators determining simultaneously the precise analog signal level. No external voltage references are required to use the ADCs.

- **FILTER BANK**
  The filter bank contains 2 selectable Anti-Alias lowpath filters (AAF) which, combined with cascadable decimation filters, allows to perform variable rate demodulation capability over a ratio of up to 45.

- **COMPLEX MUTIPLIER**
  Coherent data demodulation (BPSK or QPSK) is performed by complex multiplication of the incoming symbol with the computed correction angle. This leads to a rotation and a stabilization of the PSK constellation when the algorithms of carrier and clock recovery have both converged.
  The position of this complex multiplier is programmable and can be either after antialiasing filters or before any filtering.

- **HALF NYQUIST FILTERS**
  Half-Nyquist filtering is performed in each arm of the constellation. 2 programmable roll-off are available depending on the selected standard. The digital filter has 19 (roll-off 0.35) or 25 (roll-off 0.2) taps to provide an outband attenuation of 40dB.

- **CARRIER SYNCHRONIZER**
  The carrier synchronizer block implements successively a phase/frequency comparator, a programmable digital second order loop filter, a phase accumulator (NCO) that accumulates the phase error and drives a sine/cosine table to determine the angle for correction, applied to the complex multiplier.

- **CLOCK SYNCHRONIZER**
  The clock phase detector block implements the algorithm for variable rate digital timing recovery. The digital second order loop filter is programmable, and provides an 8-bit command to the NCO block for clock recovery.

- **AGC**
  This block calculates the magnitude of the I and Q channels after Nyquist filtering. This value is then compared to a programmable threshold value, filtered and PWM encoded before being output on the VAGC pin.

- **VITERBI DECODER**
  The Viterbi decoder performs a maximum likelihood estimation over the received data on the basis of four-bit quantized samples of the demodulated signals. The average truncation length is 144. The rate R can be chosen between R = 1/2 and R = 8/9 (punctured codes). Automatic viterbi rate recovery can be selected, so as automatic spectral inversion ambiguity resolution. The rate search is performed among rates ½, 2/3, ¾, 5/6 and 7/8 In DVB-S standard and among rates 2/3 and 6/7 in DSS mode. Output Bit Error Rate (VBER) is provided by the decoder. Differential decoding is selectable. The Viterbi decoder provides decoded data and the corresponding clock.

FUNCTIONAL DESCRIPTION (Con't)

- **FRAME SYNCHRONIZATION AND DEINTERLEAVING**

  The Viterbi decoder provides errors which occur in bursts. The length of some error bursts may exceed that which can be reliably corrected by the Reed-Solomon decoder. The implemented de-interleaving is a convolutional one of depth 12 for DVB and 13 for DSS. The first operation consists in synchronizing the de-interleaver. This is accomplished by detecting α consecutive sync Words (or $\overline{\text{sync}}$) which are present as the first byte of each packet.

  Next, the RAM memory associated with the de-interleaver fills up and the first deinterleaved bytes are provided to the input of the Reed-Solomon decoder. The state machine of the de-interleaver goes to the control phase which counts β consecutive missed sync Words (or $\overline{\text{sync}}$) before declaring the system desynchronized and going back to the sync. phase. α and β are programmable through the I2C interface.

  When the inverted sync word is detected at the input of the de-interleaver (π ambiguity at the output of the Viterbi decoder), the bytes provided to the Reed-Solomon decoder are inverted at the output of the de-interleaver.

- **REED-SOLOMON DECODER**

  The Reed-Solomon decoder decodes the symbol stream from the de-interleaver according to the (N=204 for DVB and N=146 for DSS) shortened Reed-Solomon code. Synchronization to Reed-Solomon code is defined over the finite Galois field GF (2^8). The field generator polynomial is given by :

$$G(x) = \pi_{i=0}^{15} (x + \alpha^{i})$$

  This Reed-Solomon decoder corrects up to eight erroneous symbols in each block. When the correction capability of the decoder is exceeded, the block is not changed and is provided as it has been entered. In this case the flag UNCOR is set and the MSB of the second byte in the MPEG2 frame is forced to one (TEI : Transport Error Indicator in DVB-S).The correction capability of the RS decoder can be inhibited.

- **DESCRAMBLER (DVB-S)**

  In order to comply with energy dispersal requirements of radio transmission regulations and to ensure adequate binary transitions, the MPEG2 frames are scrambled at the encoder side. Dual operation is achieved at the output of the Reed-Solomon decoder using the same scrambler/descrambler. The polynomial for the pseudo random binary sequence (PRBS generator is $1 + x^{14} + x^{15}$). The PRBS registers are initialized at the start of every eight transport packets. To provide an initialization signal for the descrambler, the MPEG2 sync byte of the first transport packet is inverted from 47_{16} to $B8_{16}$. When detected, the descrambler is loaded with the initial sequence "100101010000000". The descrambler can be inhibited. Before being provided, the inverted sync pattern $B8_{16}$ is reinverted in order to get the original MPEG2 sync word 47_{16}.

- **INTERFACE**

  The VES 1993 integrates an I2C interface in slave mode. This I2C interface fulfills the Philips component I2C bus specification.

INPUT – OUTPUT SIGNAL DESCRIPTION

Symbol	Pin Number	Type	Description
CLB#	78	I	The CLB# input is asynchronous and active low, and clears the CAS 1993. When CLB# goes low, the circuit immediately enters its RESET mode and normal operation will resume 3 XIN rising edges later after CLB# returned high. The I2C register contents are all initialized to their default values. The minimum width of CLB# at low level is 3 XIN clock periods.
XIN	97	I	Crystal oscillator input pin. Typically a fundamental XTAL oscillator is connected between the XIN and XOUT pins. (See typical application **ERROR! REFERENCE SOURCE NOT FOUND.** page **Error! Bookmark not defined.**).
XOUT	96	O	Crystal oscillator output pin. Typically a fundamental XTAL oscillator is connected between the XIN and XOUT pins. (See typical application **ERROR! REFERENCE SOURCE NOT FOUND.** page **Error! Bookmark not defined.**.)
SACLK	3	O	SamplingCLocK output. SACLK is nominally a square wave clock with a maximum of 93 MHz depending on the XTAL connected between XIN and XOUT and the multiplying factor of the PLL. SACLK is provided in case an external A/D is used only. When the internal A/D is used, SACLK is set to 0.
PLLAVS	99	I	Analog ground for the PLL.
PLLAVD	100	I	Analog positive supply voltage for the PLL. PLLAVD is typically 3.3V.
I[5:0] And Q[5:0]	6,7,8,9,10,11 16,17,18,19,20, 21	I I	I[5:0] and Q[5:0] are the 6-bit in-phase and quadrature base-band symbol input signals respectively, coming from an external dual A/D converter. These signals are sampled on the rising edge of SACLK. The input data may be in either offset binary (default) or two's complement format.(See TABLE 3 page 11).When not used, these 12 pins must be grounded (use of the internal ADCs).
VAGC	5	O 5V	PWM encoded output signal for AGC. This signal is typically fed to the AGC amplifier through a single RC network (see typical application **Error! Reference source not found.** page **Error! Bookmark not defined.**). The maximum signal frequency on VAGC output is SACLK / 8. The refresh frequency of AGC information is the symbol rate divided by 2048.
CTRL1	4	O 5V	ConTRoL line output. This output is directly programmable through the I2C interface. Its default value is a logical "1". CTRL1 is an open drain output and therefore requires an external pull-up resistor to either VDD or VCC.
CTRL2	27	O 5V	ConTRoL line output. This output is directly programmable through the I2C interface. Its default value is a logical "0". CTRL2 is an open drain output and therefore requires an external pull-up resistor to either VDD or VCC.
CTRL3	92	O 5V	ConTRoL Line output. This output is directly programmable through the I2C interface. Its default value is a logical "0". CTRL3 is an open drain output and therefore requires an external pull-up resistor to either VDD or VCC.
CTRL4	87	I/O 5V	ConTRoL Line input/output. This pin is directly programmable through the I2C interface. Its default configuration is an input. A pull-up to VDD or VCC, or a pull-down resistor to VSS must be connected to CTRL4.
DO[7:0]	56,57,58, 60,64,65, 67,68	O 3.3V	Data Output bus . These 8-bit parallel data are the outputs of the VES 1993 after demodulation, Viterbi decoding, de-interleaving, RS decoding and de-scrambling. There are 3 possible output interfaces : two parallel and one serial (See **Error! Reference source not found.**,**Error!**

Symbol	Pin Number	Type	Description
			Reference source not found.,Error! Reference source not found.)
OCLK	72	O 3.3V	Output CLock. OCLK is the output clock for the parallel DO[7:0] outputs. OCLK is internally generated depending on which type of interface is selected.
DEN	73	O 3.3V	Data ENable : this output signal is high when there is valid data on bus DO[7:0].
UNCOR	74	O 3.3V	UNCORrectable packet. This output signal goes high on a rising edge of OCLK when the provided packet is uncorrectable.
PSYNC	76	O 3.3V	Pulse SYNChro. This output signal goes high on a rising edge of OCLK each time the first byte of a packet is provided.
FEL	80	O 5V	Front End Locked. This output signal goes high when the demodulator, the Viterbi decoder and the de-interleaver are all synchronized. FEL is an open drain output and therefore requires an external pull up resistor to either VDD or VCC.
TEST	84	I	TEST input. This input pin must be grounded for normal operation of the VES 1993.
TRST	85	I	Test ReSeT. This active low input signal is used to reset the TAP controller when in boundary scan mode. In normal mode of operation TRST must be set low.
TDO	86	O 5V	Test Data Out. This is the serial Test output pin used in boundary scan mode. Serial Data are provided on the falling edge of TCK.
TCK	88	I	Test ClocK : an independant clock used to drive the TAP controller when in boundary scan mode. In normal mode of operation, TCK must be grounded.
TDI	89	I	Test Data In. The serial input for Test data and instruction when in boundary scan mode. In normal mode of operation, TDI must be set to GND or VDD.
TMS	90	I	Test Mode Select. This input signal provides the logic levels needed to change the TAP controller from state to state. In normal mode of operation, TMS must be set to VDD.
SADDR[2:0]	31,32,33	I	SADDR[2:0] input signals are the 3 LSBs of the I2C address of the VES 1993.The MSBs are internally set to 0001. Therefore the complete I2C address of the VES 1993 is (MSB to LSB) : 0, 0, 0, 1, SADDR[2], SADDR[1], SADDR[0].
SDA	36	I/O 5V	SDA is a bidirectional signal. It is the serial input/output of the I2C internal block. A pull-up resistor (typically 2.2 k•) must be connected between SDA and VCC for proper operation (Open Drain output).
SCL	37	I	I2C clock input. SCL should nominally be a square wave with a maximum frequency of 400 KHz. SCL is generated by the system I2C master.
IICDIV[1:0]	12,15	I	These pins allow to select the frequency of the I2C system clock, depending on the crystal frequency. Internal I2C clock is a division of XIN by 2^{IICDIV} (IICDIV from 1 to 3) and must be between 6 and 20 MHz.
VIN1	41	I	Analog signal Input for channel I.
VIN2	45	I	Analog signal Input for channel Q.
VREFN	42	O	Analog negative voltage reference. A decoupling capacitor of typically 0.1mF must be placed as closed as possible between VREFP and VREFN. The typical voltage value at VREFN is 1.25V.
VREFP	46	O	Analog positive voltage reference. A decoupling capacitor of typically 0.1 µF must be placed as closed as possible between VREFP and VREFN. The typical voltage value at VREFP is 2V.
AVD	43	I	Analog positive supply voltage. AVD is typically 3.3V.
AVS	44	I	Analog ground voltage. A 0.1µF decoupling capacitor must be placed between AVD and AVS.

Symbol	Pin Number	Type	Description
SCL_0	28	O 5V	This output is equivalent to the SCL input, but can be tristated by I2C programmation. A pull-up resistor (typically 22KΩ) must be connected between this pin and VCC.
SDA_0	29	I/O 5V	This signal is equivalent to the SDA I/O of the VES 1993 but can be tristated by I2C programmation. SDA_0 is bidirectionnal. A pull-up resistor (typically 22KΩ) must be connected between this pin and VCC.
TO[7:0]	53,55,59,62, 66,69,75,77	O 3.3V	TO[7:0] is a dedicated Test output bus used to test the VES 1993. In normal mode of operation, these 8 outputs are set to 0.*
INT	79	O 5V	INTerrupt line output. This active low output interrupt line can be configured by the I2C interface. INT is an open drain output and therefore requires an external pull-up resistor to either VDD or VCC.
22K_0	82	O 5V	This output pin provides the 22KHz used to control the antena LNB. This output is controlled via the I2C interface.
XINDIV	26	O 5V	This clock output pin is a division of the crystal frequency by a factor programmable from 1 to 15 through the I2C interface (index 39).
PWMO	25	O 5V	This output pin is a programmable PWM signal. It can be used as an analog control signal, which value can be programmed through the I2C interface (index 38). The maximum frequency on VAGC output is SACLK / 8.
IDDQ	30	I	Test input pin. Must be grounded.
GND	1,13,24,34, 47,50,63,70, 83,93,95	I	Digital ground voltage.
VDD	2,14,23,35, 48,49,61,71, 81,94,98	I	Digital 3.3V supply voltage.
VCC	22, 91	I	Digital 5V supply voltage.

TABLE 3. I,Q INPUT FORMAT

This table is to be used with an external 6-bit ADC.

	Offset binary (IFS = 0)	2's complement (IFS = 1)
	1 1 1 1 1 1	0 1 1 1 1 1
	⋮	⋮
	1 1 0 0 0 0	0 1 0 0 0 0
+ 1 →		
	1 0 1 1 1 1	0 0 1 1 1 1
	1 0 1 1 1 0	0 0 1 1 1 0
	⋮	⋮
	1 0 0 0 0 1	0 0 0 0 0 1
	1 0 0 0 0 0	0 0 0 0 0 0
zero →		
	0 1 1 1 1 1	1 1 1 1 1 1
	0 1 1 1 1 0	1 1 1 1 1 0
	⋮	⋮
	0 1 0 0 0 1	1 1 0 0 0 1
	0 1 0 0 0 0	1 1 0 0 0 0
- 1 →		
	0 0 1 1 1 1	1 0 1 1 1 1
	⋮	⋮
	0 0 0 0 0 0	1 0 0 0 0 0

Note : (+1) and (-1) levels correspond to AGCR[4:0] set to B_{16}.

TABLE 5. PUNCTURING AND MAPPING

Rate	R	Inhibition Flags	Mapping
½	000	inh[0] = 1 inh[1] = 1	I = X1 Q = Y1
2/3	001	inh[0] = 10 10 inh[1] = 11 11	I = X1Y2Y3 Q = Y1X3Y4
¾	010	inh[0] = 101 inh[1] = 110	I = X1Y2 Q = Y1X3
4/5	011	inh[0] = 1000 1000 inh[1] = 1111 1111	I = X1Y2Y4Y5Y7 Q = Y1Y3X5Y6Y8
5/6	100	inh[0] = 10101 inh[1] = 11010	I = X1Y2Y4 Q = Y1X3X5
6/7	101	inh[0] = 100101 100101 inh[1] = 111010 111010	I = X1Y2X4X6Y7Y9Y11 Q = Y1Y3Y5X7Y8X10 X12
7/8	110	inh[0] = 1000101 inh[1] = 1111010	I = X1Y2X4Y6 Q = Y1Y3X5X7
8/9	111	inh[0] = 10001011 10001011 inh[1] = 11110100 11110100	I = X1Y2Y4Y6X8Y9Y11X13X15 Q = Y1Y3X5X7X9Y10Y12Y14X16

Notes :
1.Polynomial X is G1=171 inhibited with inh[0]
2.Polynomial Y is G2=133 inhibited with inh[1]
3.In DVB and RAUTO modes, the only Viterbi rates that the internal state machine will look for synchronization are : 1/2, 2/3, 3/4, 5/6 and 7/8.
4.In DSS and RAUTO modes, the only Viterbi rates that the internal state machine will look for synchronization are : 2/3 and 6/7.

FIGURE 2. BLOCK DIAGRAM

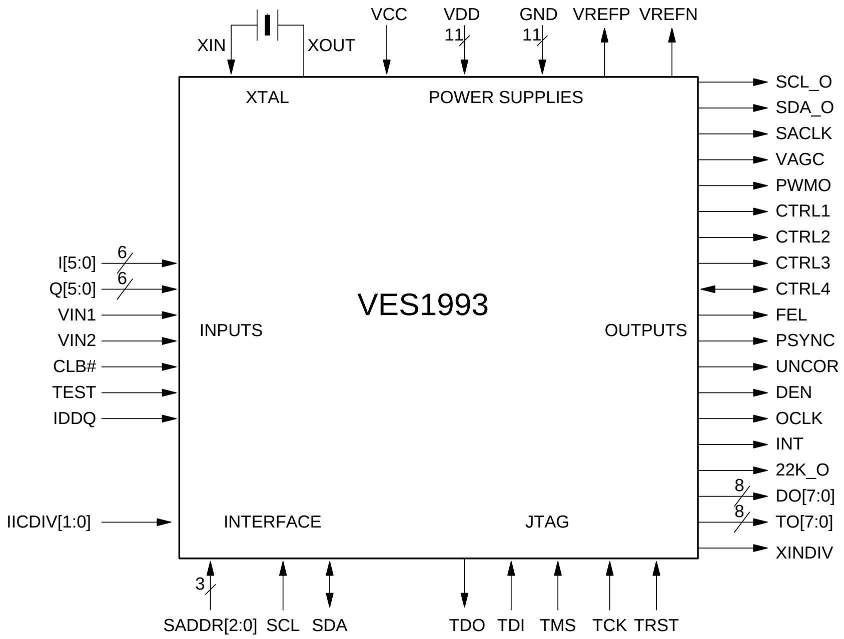


FIGURE 3. PIN DIAGRAM (100 MQFP)

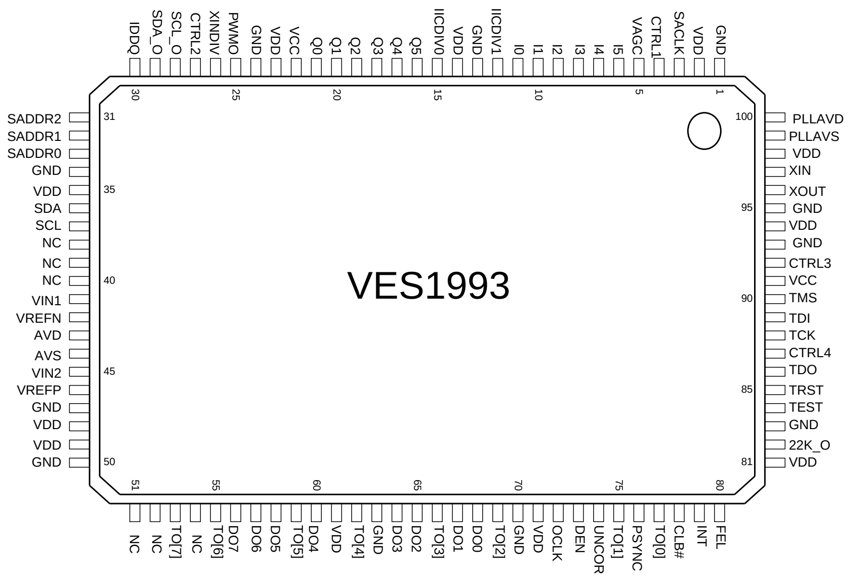


TABLE 6. PIN DESCRIPTION

Pin	Pin Name	Type	Pin	Pin Name	Type	Pin	Pin Name	Type
1	GND	-	34	GND	-	67	DO1	O
2	VDD	-	35	VDD	-	68	DO0	O
3	SACLK	O	36	SDA	I/O	69	TO[2]	O
4	CTRL1	OD	37	SCL	I	70	GND	-
5	VAGC	O	38	NC	-	71	VDD	-
6	I5	I	39	NC	-	72	OCLK	O
7	I4	I	40	NC	-	73	DEN	O
8	I3	I	41	VIN1	I	74	UNCOR	O
9	I2	I	42	VREFN	O	75	TO[1]	O
10	I1	I	43	AVD	-	76	PSYNC	O
11	I0	I	44	AVS	-	77	TO[0]	O
12	IICDIV1	I	45	VIN2	I	78	CLB#	I
13	GND	-	46	VREFP	O	79	INT	OD
14	VDD	-	47	GND	-	80	FEL	OD
15	IICDIV0	I	48	VDD	-	81	VDD	-
16	Q5	I	49	VDD	-	82	22K_0	O
17	Q4	I	50	GND	-	83	GND	-
18	Q3	I	51	NC	-	84	TEST	I
19	Q2	I	52	NC	-	85	TRST	I
20	Q1	I	53	TO[7]	O	86	TDO	O
21	Q0	I	54	NC	-	87	CTRL4	I/O
22	VCC	-	55	TO[6]	O	88	TCK	I
23	VDD	-	56	DO7	O	89	TDI	I
24	GND	-	57	DO6	O	90	TMS	I
25	PWMO	O	58	DO5	O	91	VCC	-
26	XINDIV	O	59	TO[5]	O	92	CTRL3	OD
27	CTRL2	OD	60	DO4	O	93	GND	-
28	SCL_0	O	61	VDD	-	94	VDD	-
29	SDA_0	I/O	62	TO[4]	O	95	GND	-
30	IDDQ	I	63	GND	-	96	XOUT	O
31	SADDR2	I	64	DO3	O	97	XIN	I
32	SADDR1	I	65	DO2	O	98	VDD	-
33	SADDR0	I	66	TO[3]	O	99	PLLAVS	O
						100	PLLAVD	O

Notes :
1.All inputs (I) are TTL, 5V tolerant inputs
2.OD are Open Drain 5V outputs, so they must be connected to a pull-up resistor to either VDD or VCC
3. NC pins are non connected pins. They can be grounded.

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS [(1)]
Objective specification	Development	**POSITIONThis data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.**
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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