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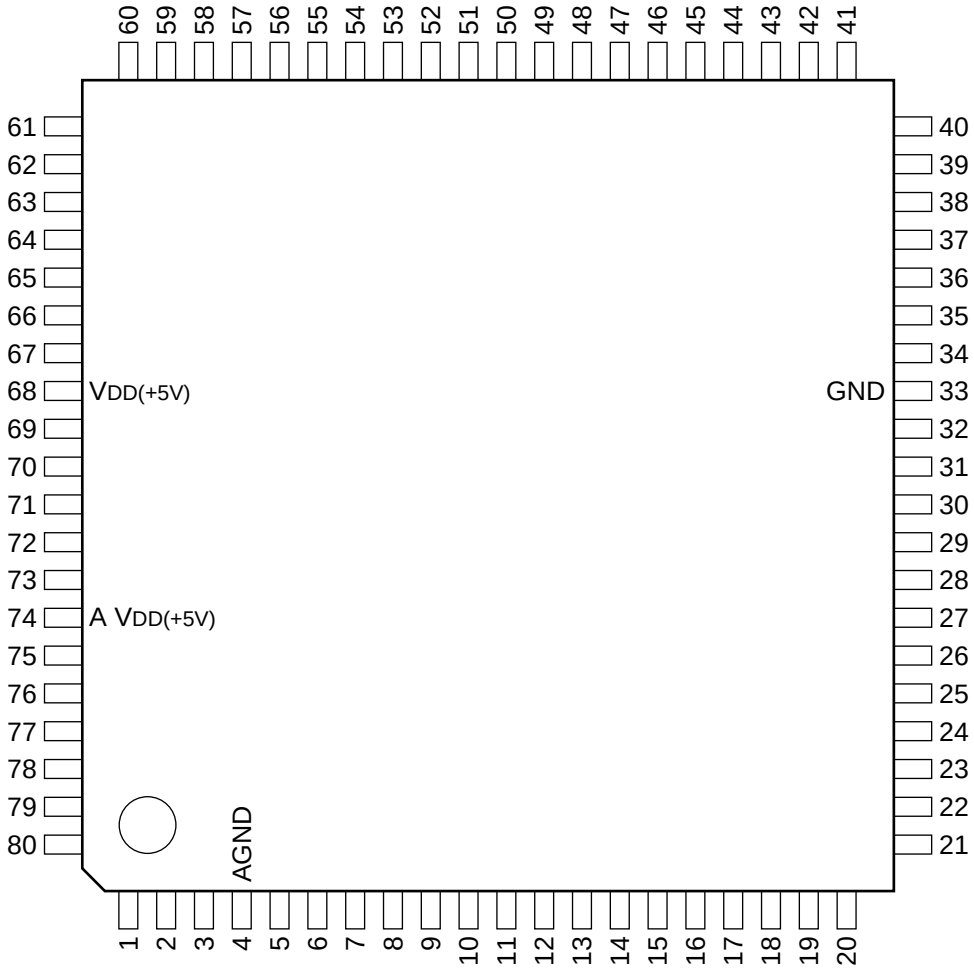
IL08

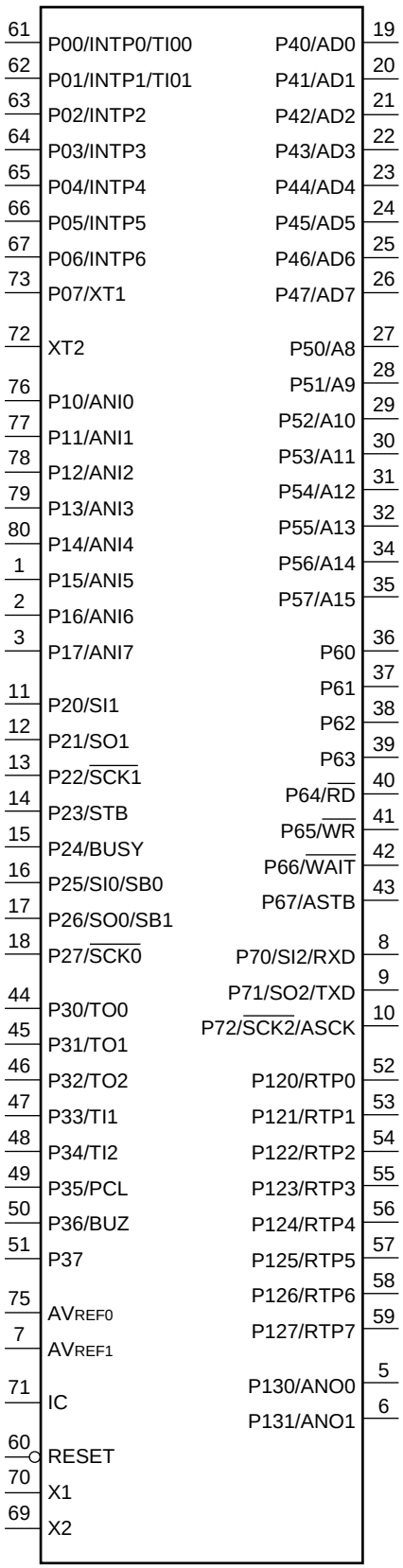
C-MOS 8-BIT MICROCOMPUTER

–TOP VIEW–



(A V_{DD}, V_{DD} = +5V)

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I/O	P15/ANI5	21	I/O	P42/AD2	41	I/O	P65/$\overline{WR}$	61	I	P00/INTP0/TI00
2	I/O	P16/ANI6	22	I/O	P43/AD3	42	I/O	P66/$\overline{WAIT}$	62	I/O	P01/INTP1/TI01
3	I/O	P17/ANI7	23	I/O	P44/AD4	43	I/O	P67/ASTB	63	I/O	P02/INTP2
4	—	AGND	24	I/O	P45/AD5	44	I/O	P30/TO0	64	I/O	P03/INTP3
5	I/O	P130/ANO0	25	I/O	P46/AD6	45	I/O	P31/TO1	65	I/O	P04/INTP4
6	I/O	P131/ANO1	26	I/O	P47/AD7	46	I/O	P32/TO2	66	I/O	P05/INTP5
7	I	AV_{REF1}	27	I/O	P50/A8	47	I/O	P33/TI1	67	I/O	P06/INTP6
8	I/O	P70/SI2/RXD	28	I/O	P51/A9	48	I/O	P34/TI2	68	—	V_{DD}
9	I/O	P71/SO2/TXD	29	I/O	P52/A10	49	I/O	P35/PCL	69	—	X2
10	I/O	P72/$\overline{SCK2}$/ASCK	30	I/O	P53/A11	50	I/O	P36/BUZ	70	I	X1
11	I/O	P20/SI1	31	I/O	P54/A12	51	I/O	P37	71	—	IC
12	I/O	P21/SO1	32	I/O	P55/A13	52	I/O	P120/RTP0	72	—	XT2
13	I/O	P22/$\overline{SCK1}$	33	—	GND	53	I/O	P121/RTP1	73	I	P07/XT1
14	I/O	P23/STB	34	I/O	P56/A14	54	I/O	P122/RTP2	74	—	AV_{DD}
15	I/O	P24/BUSY	35	I/O	P57/A15	55	I/O	P123/RTP3	75	I	AV_{REF0}
16	I/O	P25/SI0/SB0	36	I/O	P60	56	I/O	P124/RTP4	76	I/O	P10/ANI0
17	I/O	P26/SO0/SB1	37	I/O	P61	57	I/O	P125/RTP5	77	I/O	P11/ANI1
18	I/O	P27/$\overline{SCK0}$	38	I/O	P62	58	I/O	P126/RTP6	78	I/O	P12/ANI2
19	I/O	P40/AD0	39	I/O	P63	59	I/O	P127/RTP7	79	I/O	P13/ANI3
20	I/O	P41/AD1	40	I/O	P64/$\overline{RD}$	60	I	$\overline{RESET}$	80	I/O	P14/ANI4



INPUT

ANI0 - ANI7	;	ANALOG 0 - 7 (A/D CONVERTER)
ASCK	;	ASYNCHRONOUS SERIAL CLOCK
ASTB	;	ADDRESS STROBE
AVREF0	;	ANALOG REFERENCE VOLTAGE (A/D CONVERTER)
AVREF1	;	ANALOG REFERENCE VOLTAGE (D/A CONVERTER)
BUSY	;	BUSY
INTP0 - INTP6	;	INTERRUPT FROM PERIPHERALS 0 - 6
PO0, PO7	;	PORT 0
$\overline{\text{RESET}}$	;	RESET
RXD	;	RECEIVE DATA
SI0 - SI2	;	SERIAL DATA 0 - 2
TI00	;	EXTERNAL COUNT CLOCK 0
TI01	;	CAPTURE TRIGGER
TI1, TI2	;	EXTERNAL COUNT CLOCK 1, 2
$\overline{\text{WAIT}}$	;	WAIT
X1, X2	;	CRYSTAL1, 2 (MAIN SYSTEM CLOCK)
XT1, XT2	;	CRYSTAL1, 2 (SUB SYSTEM CLOCK)

OUTPUT

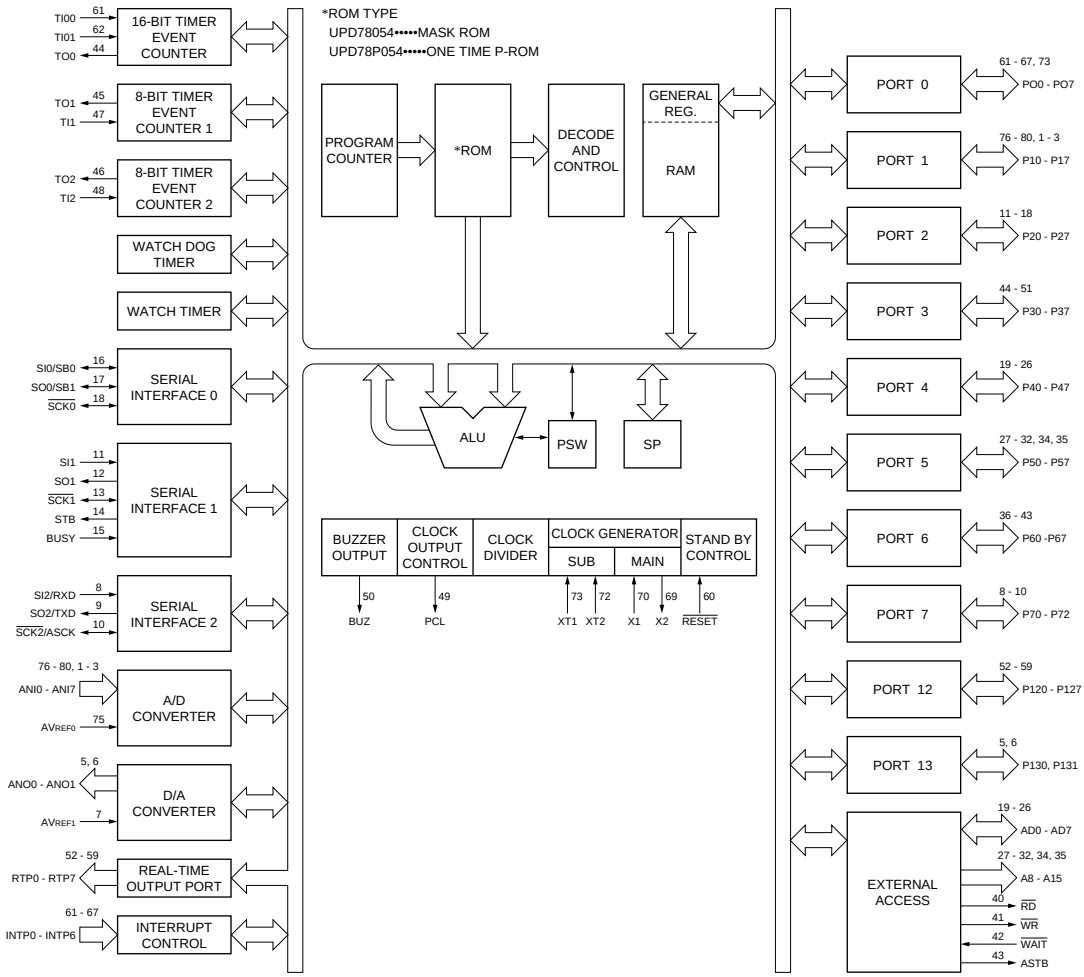
A8 - A15	;	ADDRESS BUS
ANO0, ANO1	;	ANALOG 0, 1 (D/A CONVERTER)
BUZ	;	BUZZER CLOCK
PCL	;	PROGRAMMABLE CLOCK
$\overline{\text{RD}}$	;	READ STROBE
RTP0 - RTP7	;	REAL-TIME PORT
SO0 - SO2	;	SERIAL DATA 0 - 2
STB	;	STROBE
TO0 - TO2	;	TIMER 0 - 2
TXD	;	TRANSMIT DATA
$\overline{\text{WR}}$	;	WRITE STROBE

INPUT/OUTPUT

AD0 - AD7	;	ADDRESS/DATA BUS 0 - 7
P01 - P06	;	PORT 0
P10 - P17	;	PORT 1
P20 - P27	;	PORT 2
P30 - P37	;	PORT 3
P40 - P47	;	PORT 4
P50 - P57	;	PORT 5
P60 - P67	;	PORT 6
P70 - P72	;	PORT 7
P120 - P127	;	PORT 12
P130, P131	;	PORT 13
SB0, SB1	;	SERIAL DATA BUS 0 , 1
$\overline{\text{SCK0}}$ - $\overline{\text{SCK2}}$	;	SERIAL CLOCK 0 - 2

OTHER

IC	;	INTERNALLY CONNECTED


*ROM TYPE
UPD78054•••••MASK ROM
UPD78P054•••••ONE TIME P-ROM
TI00
TI01
TO0
16-BIT TIMER EVENT COUNTER
TO1
TI1
8-BIT TIMER EVENT COUNTER 1
TO2
TI2
8-BIT TIMER EVENT COUNTER 2
WATCH DOG TIMER
WATCH TIMER
SI0/SB0
SO0/SB1
SCK0
SERIAL INTERFACE 0
SI1
SO1
SCK1
STB
BUSY
SERIAL INTERFACE 1
SI2/RXD
SO2/TXD
SCK2/ASCK
SERIAL INTERFACE 2
ANI0 - ANI7
AVREF0
A/D CONVERTER
ANO0 - ANO1
AVREF1
D/A CONVERTER
RTP0 - RTP7
REAL-TIME OUTPUT PORT
INTP0 - INTP6
INTERRUPT CONTROL
PROGRAM COUNTER
*ROM
DECODE AND CONTROL
GENERAL REG.
RAM
ALU
PSW
SP
BUZZER OUTPUT
CLOCK OUTPUT CONTROL
CLOCK DIVIDER
CLOCK GENERATOR
SUB
MAIN
STAND BY CONTROL
BUZ
PCL
XT1
XT2
X1
X2
RESET
PORT 0
PO0 - PO7
PORT 1
P10 - P17
PORT 2
P20 - P27
PORT 3
P30 - P37
PORT 4
P40 - P47
PORT 5
P50 - P57
PORT 6
P60 -P67
PORT 7
P70 - P72
PORT 12
P120 - P127
PORT 13
P130, P131
EXTERNAL ACCESS
AD0 - AD7
A8 - A15
RD
WR
WAIT
ASTB