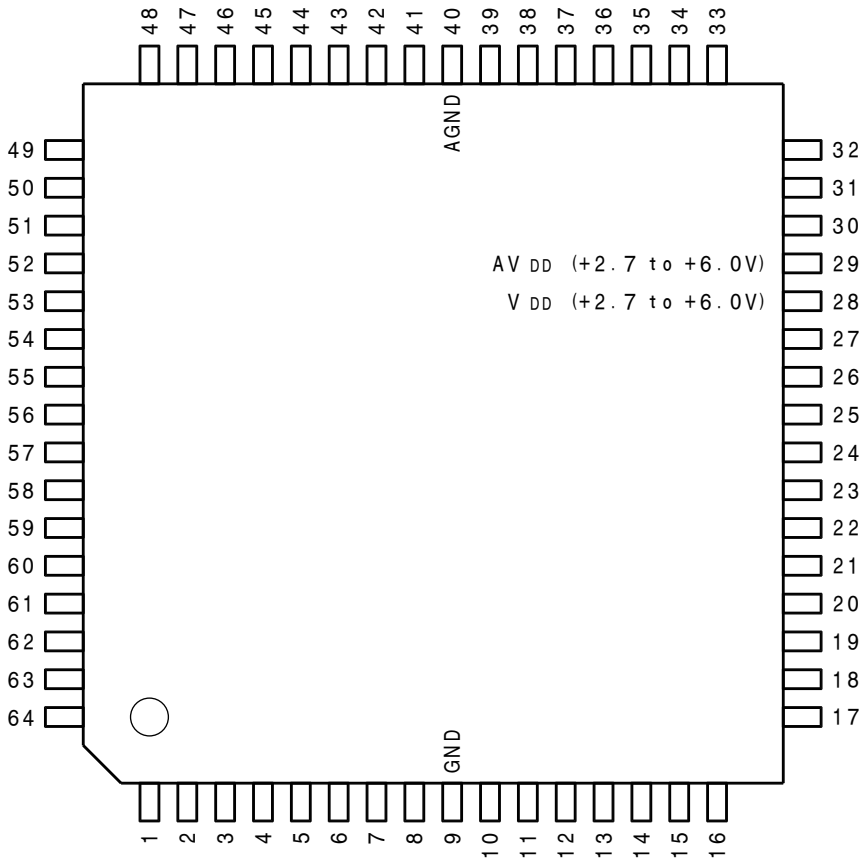
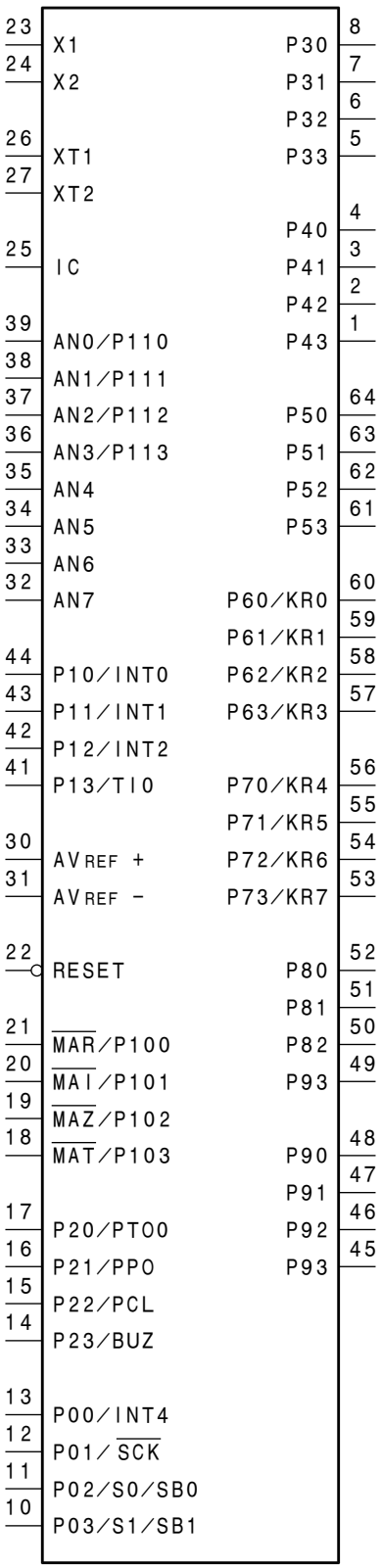
C-MOS 4-BIT SINGLE CHIP MICROCOMPUTER WITH MASK ROM AND EEPROM

-TOP VIEW-



(AVDD =VDD =+2.7 to +6.0V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I/O	P43	17	I/O	PTO0/P20	33	I	AN6	49	I/O	P83
2	I/O	P42	18	I/O	$\overline{MAT}$/P103	34	I	AN5	50	I/O	P82
3	I/O	P41	19	I/O	$\overline{MAZ}$/P102	35	I	AN4	51	I/O	P81
4	I/O	P40	20	O	$\overline{MAI}$/P101	36	I	AN3/P113	52	I/O	P80
5	I/O	P33	21	O	$\overline{MAR}$/P100	37	I	AN2/P112	53	I/O	P73/KR7
6	I/O	P32	22	I	$\overline{RESET}$	38	I	AN1/P111	54	I/O	P72/KR6
7	I/O	P31	23	I	X1	39	I	AN0/P110	55	I/O	P71/KR5
8	I/O	P30	24	-	X2	40	-	AGND	56	I/O	P70/KR4
9	-	GND	25	-	IC	41	I	TI0/P13	57	I/O	P63/KR3
10	I/O	SB1/SI/P03	26	I	XT1	42	I	P12/INT2	58	I/O	P62/KR2
11	I/O	SB0/SO/P02	27	-	XT2	43	I	P11/INT1	59	I/O	P61/KR1
12	I/O	$\overline{SCK}$/P01	28	-	VDD	44	I	P10/INT0	60	I/O	P60/KR0
13	I	INT4/P00	29	-	AVDD	45	I/O	P93	61	I/O	P53
14	I/O	BUZ/P23	30	I	AVREF+	46	I/O	P92	62	I/O	P52
15	I/O	PCL/P22	31	I	AVREF-	47	I/O	P91	63	I/O	P51
16	I/O	PPO/P21	32	I	AN7	48	I/O	P90	64	I/O	P50

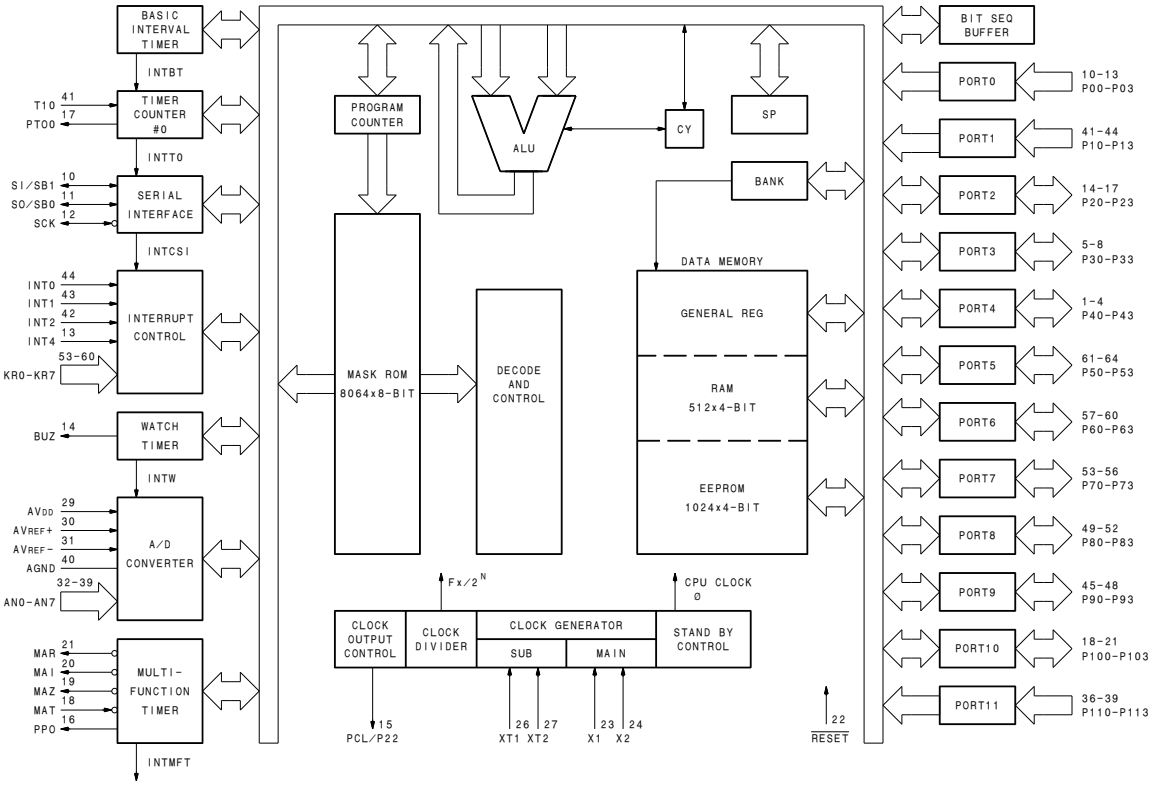


PORT

P00-P03	;PORT 0 IN/OUT
P10-P13	;PORT 1 IN
P20-P23	;PORT 2 IN/OUT
P30-P33	;PORT 3 IN/OUT
P40-P43	;PORT 4 IN/OUT
P50-P53	;PORT 5 IN/OUT
P60-P63	;PORT 6 IN/OUT
P70-P73	;PORT 7 IN/OUT
P80-P83	;PORT 8 IN/OUT
P90-P93	;PORT 9 IN/OUT
P100-P103	;PORT 10 IN/OUT
P110-P113	;PORT 11 IN

OTHERS

AN0-AN7	;ANALOG 0-7 IN
AVREF +	;ANALOG REFERENCE (+) IN
AVREF -	;ANALOG REFERENCE (-) IN
BUZ	;BUZZER CLOCK OUT
INT0, 1, 4	;EXTERNAL VECTORED INTERRUPT 0, 1, 4 IN
INT2	;EXTERNAL TEST 2 IN
KR0-KR7	;KEY RETURN 0-7 IN
MAI	;INTEGRATION CONTROL (MFT A/D MODE) OUT
MAR	;REFERENCE INTEGRATION CONTROL OUT (MFT A/D MODE)
MAT	;EXTERNAL COMPARATE TIMING IN/OUT (MFT A/D MODE)
MAZ	;AUTOZERO CONTROL (MFT A/D MODE) OUT
PCL	;PROGRAMMABLE CLOCK OUT
PPO	;PROGRAMMABLE PULSE (MFT TIMER MODE) OUT
PTO0	;PROGRAMMABLE TIMER 0 OUT
RESET	;RESET IN
SB0, 1	;SERIAL BUS 0, 1 IN/OUT
SCK	;SERIAL CLOCK IN/OUT
SO	;SERIAL OUT
SI	;SERIAL IN
TI0	;TIMER 0 IN
X1, 2	;MAIN SYSTEM CLOCK OSCILLATION 1, 2 IN
XT1, 2	;SUB SYSTEM CLOCK OSCILLATION 1, 2 IN


BASIC INTERVAL TIMER
INTBT
T10
PTO0
41
17
TIMER COUNTER #0
INTTO
SI/SB1
SO/SB0
SCK
10
11
12
SERIAL INTERFACE
INTCSI
INT0
INT1
INT2
INT4
KR0-KR7
44
43
42
13
53-60
INTERRUPT CONTROL
BUZ
14
WATCH TIMER
INTW
AVDD
AVREF+
AVREF-
AGND
AN0-AN7
29
30
31
40
32-39
A/D CONVERTER
MAR
MAI
MAZ
MAT
PPO
21
20
19
18
16
MULTI-FUNCTION TIMER
INTMFT
PROGRAM COUNTER
ALU
CY
SP
BANK
DATA MEMORY
GENERAL REG
RAM 512x4-BIT
EEPROM 1024x4-BIT
MASK ROM 8064x8-BIT
DECODE AND CONTROL
Fx/2N
CPU CLOCK Ø
CLOCK OUTPUT CONTROL
CLOCK DIVIDER
CLOCK GENERATOR
SUB
MAIN
STAND BY CONTROL
15
PCL/P22
26 27
XT1 XT2
23 24
X1 X2
22
RESET
BIT SEQ BUFFER
PORT0
PORT1
PORT2
PORT3
PORT4
PORT5
PORT6
PORT7
PORT8
PORT9
PORT10
PORT11
10-13 P00-P03
41-44 P10-P13
14-17 P20-P23
5-8 P30-P33
1-4 P40-P43
61-64 P50-P53
57-60 P60-P63
53-56 P70-P73
49-52 P80-P83
45-48 P90-P93
18-21 P100-P103
36-39 P110-P113