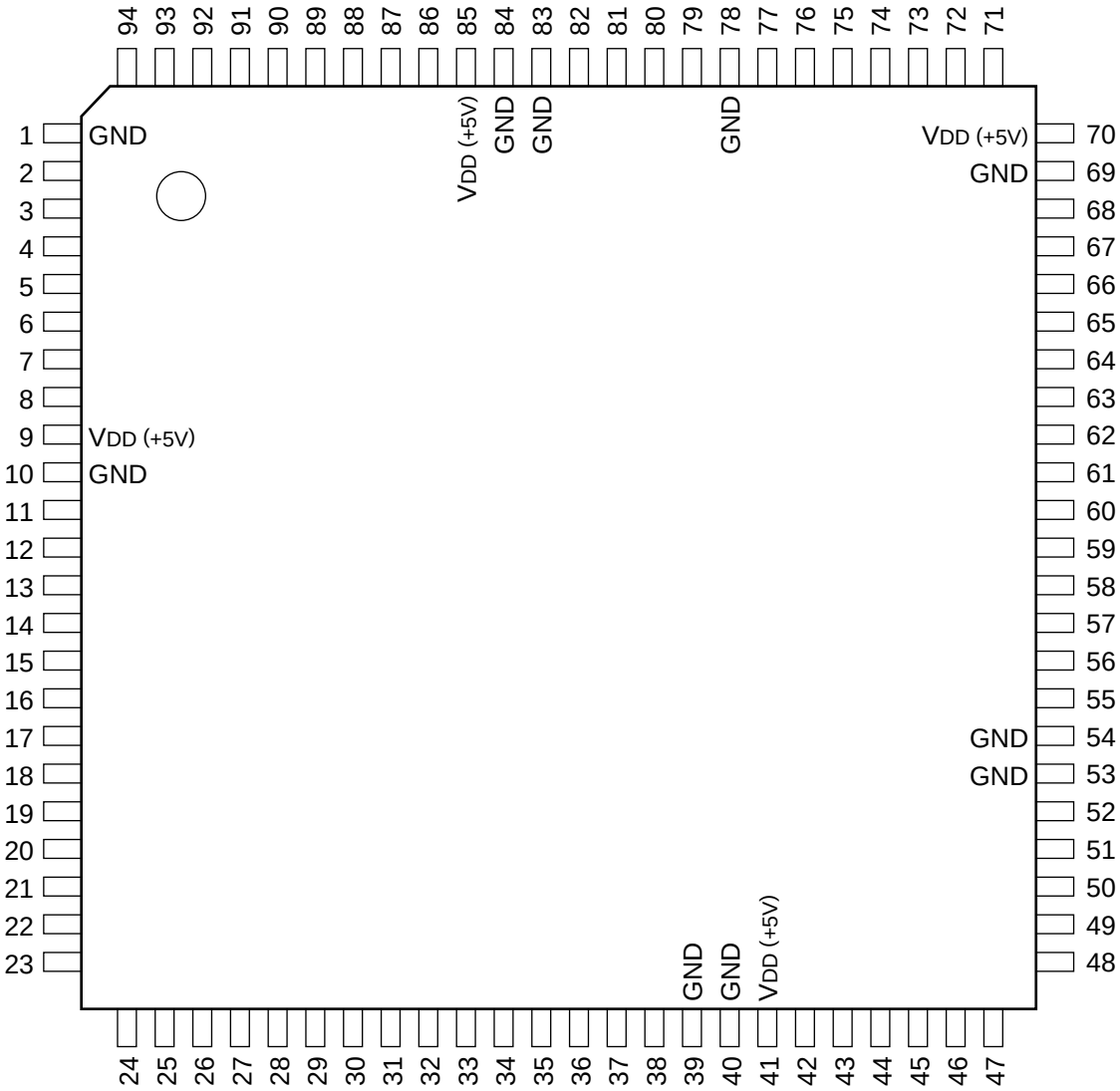
****

IL00

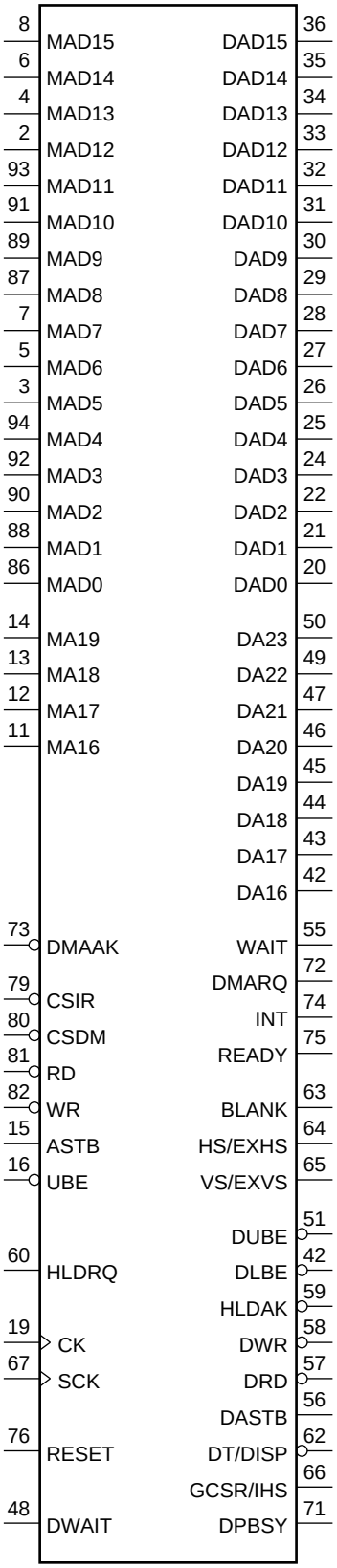
C-MOS ADVANCED GRAPHIC DISPLAY CONTROLLER

-TOP VIEW-



(V_{DD} = +5V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	—	GND	25	I/O	DAD4	49	O	DA22	73	I	DMAAK
2	I/O	MAD12	26	I/O	DAD5	50	O	DA23	74	O	INT
3	I/O	MAD5	27	I/O	DAD6	51	O	DUBE	75	O	READY
4	I/O	MAD13	28	I/O	DAD7	52	O	DLBE	76	I	RESET
5	I/O	MAD6	29	I/O	DAD8	53	—	GND	77	—	IC
6	I/O	MAD14	30	I/O	DAD9	54	—	GND	78	—	GND
7	I/O	MAD7	31	I/O	DAD10	55	O	WAIT	79	I	CSIR
8	I/O	MAD15	32	I/O	DAD11	56	O	DASTB	80	I	CSDM
9	—	V_{DD}	33	I/O	DAD12	57	O	DRD	81	I	RD
10	—	GND	34	I/O	DAD13	58	O	DWR	82	I	WR
11	I	MA16	35	I/O	DAD14	59	O	HLDAK	83	—	GND
12	I	MA17	36	I/O	DAD15	60	I	HLDRO	84	—	GND
13	I	MA18	37	—	IC	61	—	IC	85	—	V_{DD}
14	I	MA19	38	—	IC	62	O	DT/DISP	86	I/O	MAD0
15	I	ASTB	39	—	GND	63	O	BLANK	87	I/O	MAD8
16	I	UBE	40	—	GND	64	I/O	HS/EXHS	88	I/O	MAD1
17	—	IC	41	—	V_{DD}	65	I/O	VS/EXVS	89	I/O	MAD9
18	—	IC	42	O	DA16	66	O	GCSR/IHS	90	I/O	MAD2
19	I	CK	43	O	DA17	67	I	SCK	91	I/O	MAD10
20	I/O	DAD0	44	O	DA18	68	—	IC	92	I/O	MAD3
21	I/O	DAD1	45	O	DA19	69	—	GND	93	I/O	MAD11
22	I/O	DAD2	46	O	DA20	70	—	V_{DD}	94	I/O	MAD4
23	—	IC	47	O	DA21	71	O	DPBSY			
24	I/O	DAD3	48	I	DWAIT	72	O	DMARO			



INPUT

ASTB	;	ADDRESS STROBE
$\overline{CK}$	;	CLOCK
$\overline{CSDM}$	;	CHIP SELECT DISPLAY MEMORY
$\overline{CSIR}$	;	CHIP SELECT INTERNAL REGISTER
$\overline{DMAAK}$	;	DMA ACKNOWLEDGE
DWAIT	;	DRAWING WAIT
HLDRQ	;	HOLD REQUEST
MA19-16	;	MAIN ADDRESS
$\overline{RESET}$	;	RESET (PARAMETER REGISTER NO CLEAR)
$\overline{RD}$	;	READ
$\overline{SCK}$	;	SYNC CLOCK
$\overline{UBE}$	;	UPPER BYTE ENABLE
$\overline{WR}$	;	WRITE

OUTPUT

BLANK	;	DISPLAY ERASE CONTROL
DA23-16	;	DISPLAY ADDRESS
DASTB	;	DISPLAY ADDRESS STROBE
DLBE	;	DISPLAY LOWER BYTE ENABLE
DMARQ	;	DMA REQUEST
DPBSY	;	DRAWING PROCESSOR BUSY
DRD	;	DISPLAY READ
DT/DISP	;	DATA TRANSFER/DISPLAY
DUBE	;	DISPLAY UPPER BYTE ENABLE
DWR	;	DISPLAY WRITE
GCSR/IHS	;	GRAPHIC CURSOR/ INTERNAL HORIZONTAL SYNC
HLDAK	;	HOLD ACKNOWLEDGE
INT	;	INTERRUPT
READY	;	RD/WR ACCESS WITH LOW OUTPUT
WAIT	;	GDC WAIT CONTROL

INPUT/OUTPUT

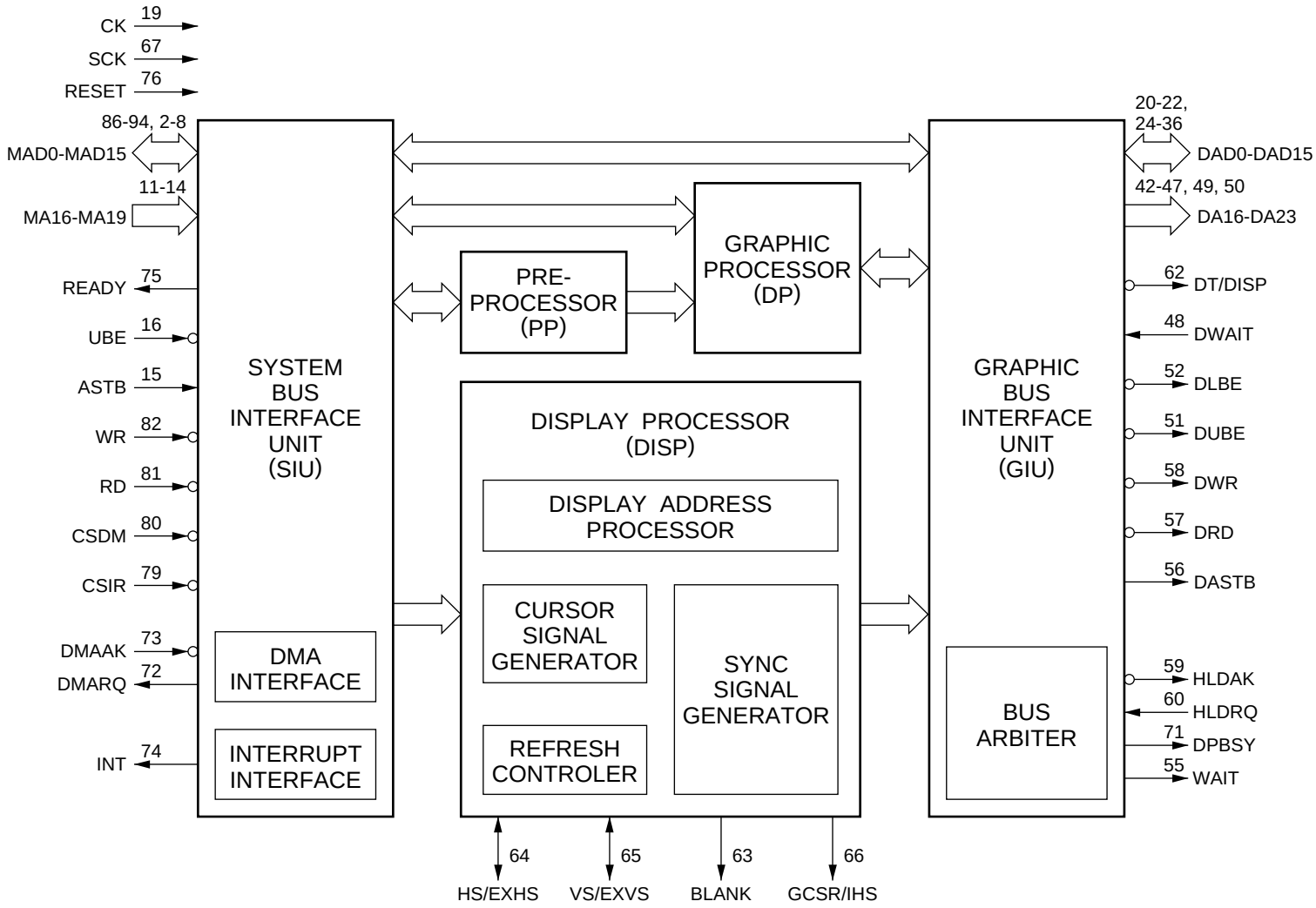
DAD15-0	;	DISPLAY/ADDRESS/DATA BUS
HS/EXHS	;	H SYNC/EXTERNAL H SYNC
MAD15-0	;	MAIN ADDRESS/DATA BUS
VS/EXVS	;	V SYNC/EXTERNAL V SYNC

• PREDFINE DATA ACCESS

DATA BUS OF DIMENSION MEMORY

DLBE	DUBE	DATA ACCESS FORMAT
0	0	EVEN ADDRESS WORD
0	1	EVEN ADDRESS BYTE
1	0	ODD ADDRESS BYTE

0 ; LOW LEVEL
1 ; HIGH LEVEL


CK
19
SCK
67
RESET
76
86-94, 2-8
MAD0-MAD15
11-14
MA16-MA19
READY
75
UBE
16
ASTB
15
WR
82
RD
81
CSDM
80
CSIR
79
DMAAK
73
DMARQ
72
INT
74
SYSTEM BUS INTERFACE UNIT (SIU)
DMA INTERFACE
INTERRUPT INTERFACE
PRE-PROCESSOR (PP)
GRAPHIC PROCESSOR (DP)
DISPLAY PROCESSOR (DISP)
DISPLAY ADDRESS PROCESSOR
CURSOR SIGNAL GENERATOR
SYNC SIGNAL GENERATOR
REFRESH CONTROLER
64
HS/EXHS
65
VS/EXVS
63
BLANK
66
GCSR/IHS
GRAPHIC BUS INTERFACE UNIT (GIU)
BUS ARBITER
20-22, 24-36
DAD0-DAD15
42-47, 49, 50
DA16-DA23
62
DT/DISP
48
DWAIT
52
DLBE
51
DUBE
58
DWR
57
DRD
56
DASTB
59
HLDAK
60
HLDRQ
71
DPBSY
55
WAIT