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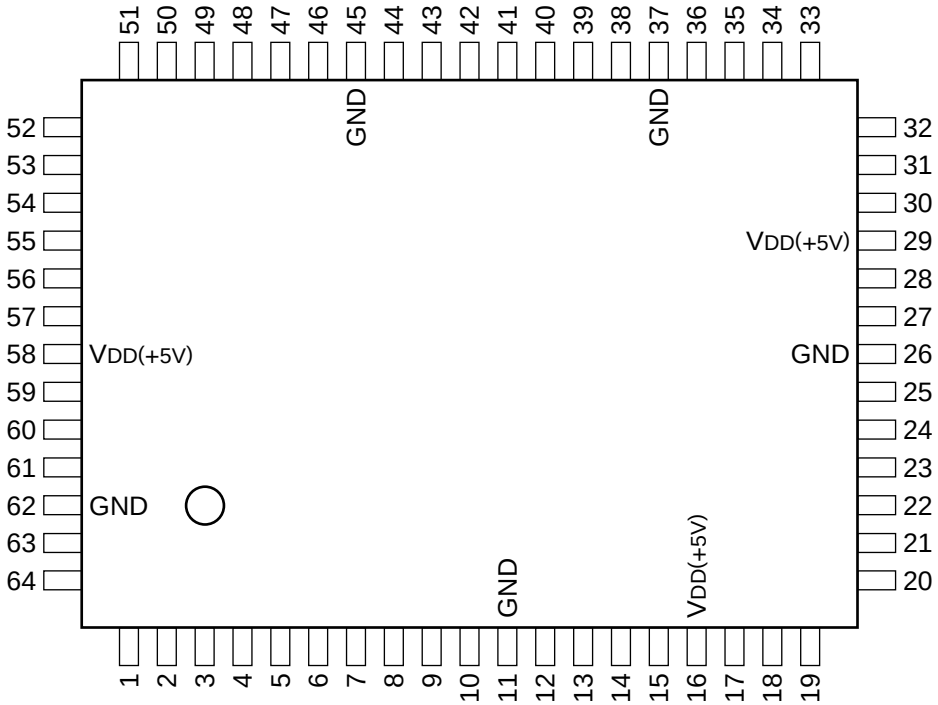
C-MOS FLOPPY DISK CONTROLLER

—TOP VIEW—



(VDD = +5V)

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	$\overline{RD}$	17	O	INT	33	I	$\overline{TRK0}$	49	I	$\overline{INDEX}$
2	I	$\overline{WR}$	18	O	DMARQ	34	O	$\overline{WGATE}$	50	O	$\overline{DS3}$
3	I	$\overline{CS}$	19	I	TC	35	O	$\overline{WDATA}$	51	O	$\overline{HDLD}$ (SEL)
4	I	A0	20	I	$\overline{ENDKCG}$	36	O	$\overline{ME3}$ ($\overline{ENBL1}$)	52	O	$\overline{DEN0}$
5	I	A1	21	I	$\overline{DRV2}$	37	—	GND	53	O	$\overline{DEN1}$
6	I	A2	22	I	PCTYP0	38	O	$\overline{ME2}$ ($\overline{ENBL0}$)	54	O	TDO
7	I/O	DB0	23	I	PCTYP1	39	O	NC (LSTRB)	55	I	TCK
8	I/O	DB1	24	O	CGP1	40	O	$\overline{SIDE}$ (CA2)	56	I	TMS
9	I/O	DB2	25	O	CGP2	41	O	$\overline{STEP}$ (CA1)	57	I	TDI
10	I/O	DB3	26	—	GND	42	O	$\overline{DIR}$ (CA0)	58	—	VDD
11	—	GND	27	O	LPF1	43	O	$\overline{ME1}$	59	I	XB
12	I/O	DB4	28	O	LPF2	44	O	$\overline{ME0}$	60	—	XA2
13	I/O	DB5	29	—	VDD	45	—	GND	61	I	XA1
14	I/O	DB6	30	I	$\overline{DKCG}$/$\overline{READY}$	46	O	$\overline{DS2}$	62	—	GND
15	I/O	DB7	31	I	$\overline{RDATA}$	47	O	$\overline{DS1}$	63	I	RESET
16	—	VDD	32	I	$\overline{WPRT}$	48	O	$\overline{DS0}$	64	I	$\overline{DMAAK}$

NOTE : ( ) APPLIES TO ONLY APPLE FDD MODE.

INPUT

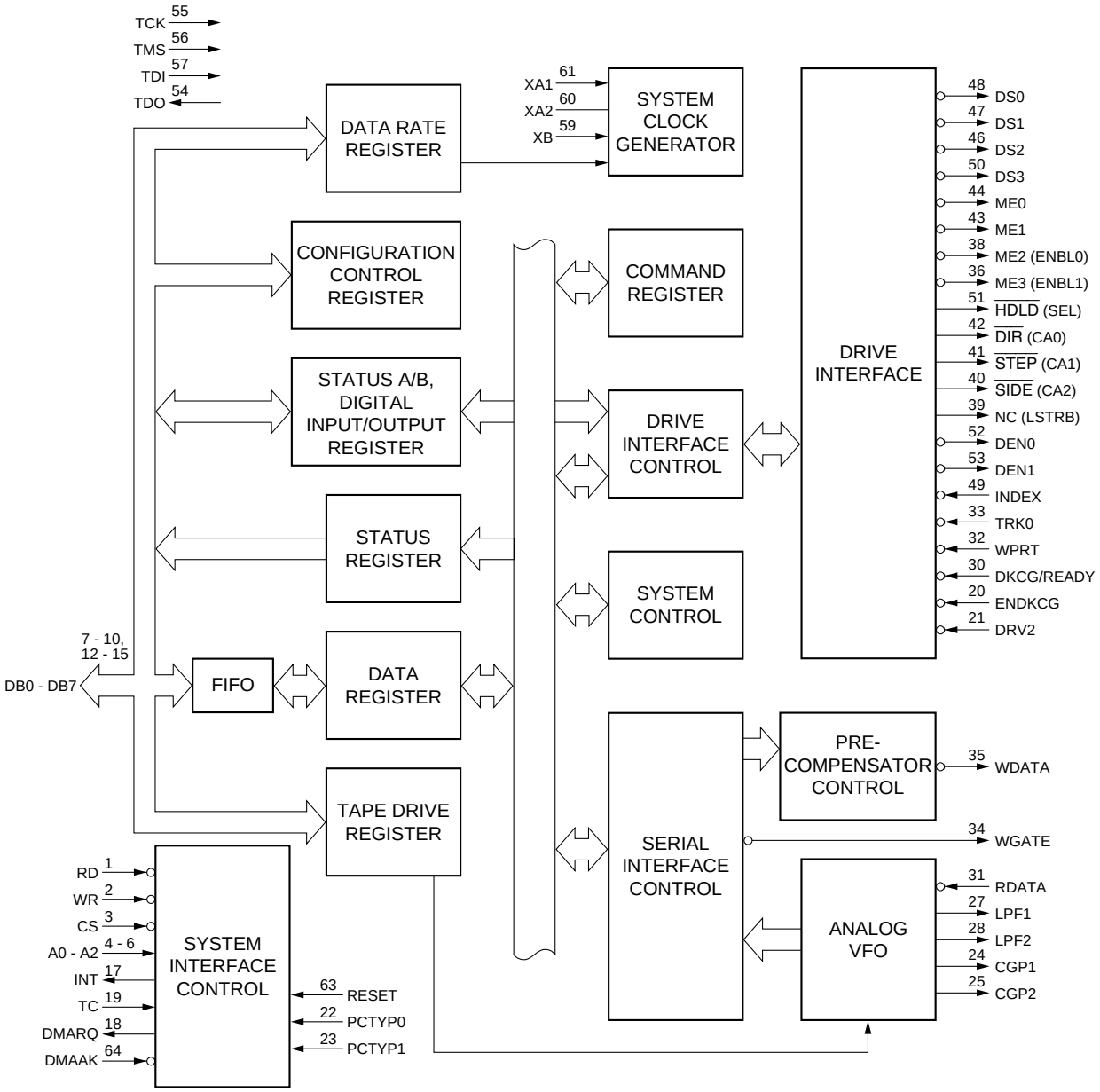
A0 - A2	;	ADDRESS
$\overline{CS}$	;	CHIP SELECT
$\overline{DKCG}$/$\overline{READY}$	;	DISK CHANGE/READY
$\overline{DMAAK}$	;	DMA ACKNOWLEDGE
$\overline{DRV2}$	;	DRIVE2
$\overline{ENDKCG}$	;	ENABLE DISK CHANGE
$\overline{INDEX}$	;	INDEX PULSE
PCTYP0, PCTYP1	;	PC TYPE
$\overline{RD}$	;	READ
$\overline{RDATA}$	;	READ DATA
RESET	;	RESET
TC	;	TERMINAL COUNT
TCK	;	TEST CLOCK
TDI	;	TEST DATA
TMS	;	TEST MODE SELECT
$\overline{TRK0}$	;	TRACK0
$\overline{WR}$	;	WRITE
$\overline{WPRT}$	;	WRITE PROTECT
XA1, XA2	;	CRYSTAL A
XB	;	CRYSTAL B

OUTPUT

CGP1, $\overline{CGP2}$	;	CHARGE PUMP
$\overline{DEN0}$, $\overline{DEN1}$	;	DENSITY
$\overline{DIR}$ (CA0)	;	DIRECTION (CA0)
DMARQ	;	DMA REQUEST
$\overline{DS0}$ - $\overline{DS3}$	;	DRIVE SELECT
$\overline{HDLD}$ (SEL)	;	HEAD LOAD (SEL)
INT	;	INTERRUPT REQUEST
LPF1, LPF2	;	LOW PASS FILTER
$\overline{ME0}$, $\overline{ME1}$	;	MOTOR ENABLE
$\overline{ME2}$ ($\overline{ENBL0}$)	;	MOTOR ENABLE2 (ENABLE0)
$\overline{ME3}$ ($\overline{ENBL1}$)	;	MOTOR ENABLE3 (ENABLE1)
NC (LSTRB)	;	NO CONNECTION (LINE STROBE)
$\overline{SIDE}$ (CA2)	;	SIDE (CA2)
$\overline{STEP}$ (CA1)	;	STEP (CA1)
TDO	;	TEST DATA
$\overline{WDATA}$	;	WRITE DATA
$\overline{WGATE}$	;	WRITE GATE

INPUT/OUTPUT

DB0 - DB7	;	DATA BUS


TCK 55
TMS 56
TDI 57
TDO 54
DATA RATE REGISTER
XA1 61
XA2 60
XB 59
SYSTEM CLOCK GENERATOR
CONFIGURATION CONTROL REGISTER
COMMAND REGISTER
STATUS A/B, DIGITAL INPUT/OUTPUT REGISTER
DRIVE INTERFACE CONTROL
STATUS REGISTER
SYSTEM CONTROL
7 - 10, 12 - 15
DB0 - DB7
FIFO
DATA REGISTER
TAPE DRIVE REGISTER
SERIAL INTERFACE CONTROL
PRE-COMPENSATOR CONTROL
ANALOG VFO
DRIVE INTERFACE
48 DS0
47 DS1
46 DS2
50 DS3
44 ME0
43 ME1
38 ME2 (ENBL0)
36 ME3 (ENBL1)
51 HDLD (SEL)
42 DIR (CA0)
41 STEP (CA1)
40 SIDE (CA2)
39 NC (LSTRB)
52 DEN0
53 DEN1
49 INDEX
33 TRK0
32 WPRT
30 DKCG/READY
20 ENDKCG
21 DRV2
35 WDATA
34 WGATE
31 RDATA
27 LPF1
28 LPF2
24 CGP1
25 CGP2
RD 1
WR 2
CS 3
A0 - A2 4 - 6
INT 17
TC 19
DMARQ 18
DMAAK 64
SYSTEM INTERFACE CONTROL
63 RESET
22 PCTYP0
23 PCTYP1