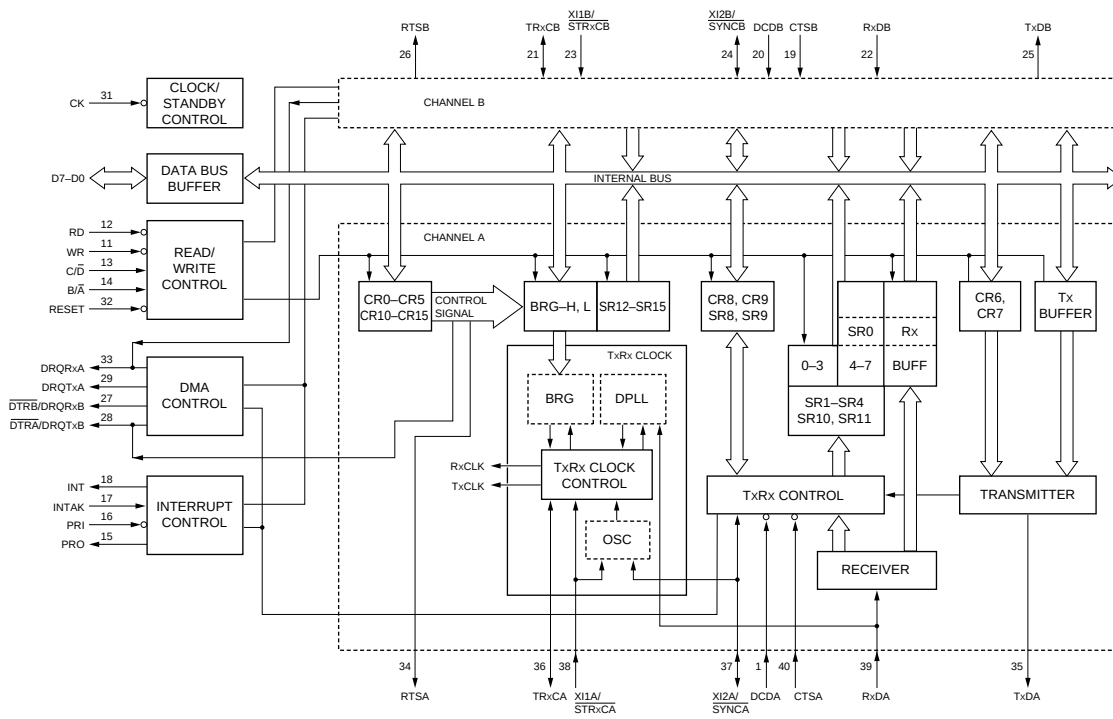




INPUTS				FUNCTION	
WR	RD	B/A	C/D		
0	1	0	0	CHANNEL A	WRITE (Tx/D)
		1		CHANNEL B	
1	0	0	0	CHANNEL A	READ (Rx/D)
		1		CHANNEL B	
0	1	0	1	CHANNEL A	WRITE (CONTROL REGISTER)
		1		CHANNEL B	
1	0	0	1	CHANNEL A	READ (STATUS REGISTER)
		1		CHANNEL B	
1	1	X	X		HIGH-IMPEDANCE
0	0	X	X		INHIBIT

0 ; LOW LEVEL
1 ; HIGH LEVEL
X ; DON'T CARE

CK ; SYSTEM CLOCK INPUT
WR ; WRITE ENABLE INPUT
RD ; READ ENABLE INPUT
B/A ; CHANNEL B/A SELECT INPUT
C/D ; CONTROL/DATA SELECT INPUT
D0-D7 ; DATA BUS INPUTS/OUTPUTS
INT ; INTERRUPT OUTPUT
INTAK ; INTERRUPT ACKNOWLEDGE INPUT
PRI ; PRIORITY INPUT
DRQTxA ; DMA REQUEST Tx/A OUTPUT
DRQRxA ; DMA REQUEST Rx/A OUTPUT
PRO ; PRIORITY OUTPUT

DTxR/DRQTxB ; DATA TERMINAL READY A/DMA REQUEST Tx/B OUTPUT
DTxR/DRQRxB ; DATA TERMINAL READY B/DMA REQUEST Rx/B OUTPUT
CTSA, CTxB ; CLEAR TO SEND A/B INPUT
DCDA, DCDB ; DATA CARRIER DETECT A/B INPUT
RTSA, RTSB ; REQUEST TO SEND A/B OUTPUT
RESET ; RESET INPUT