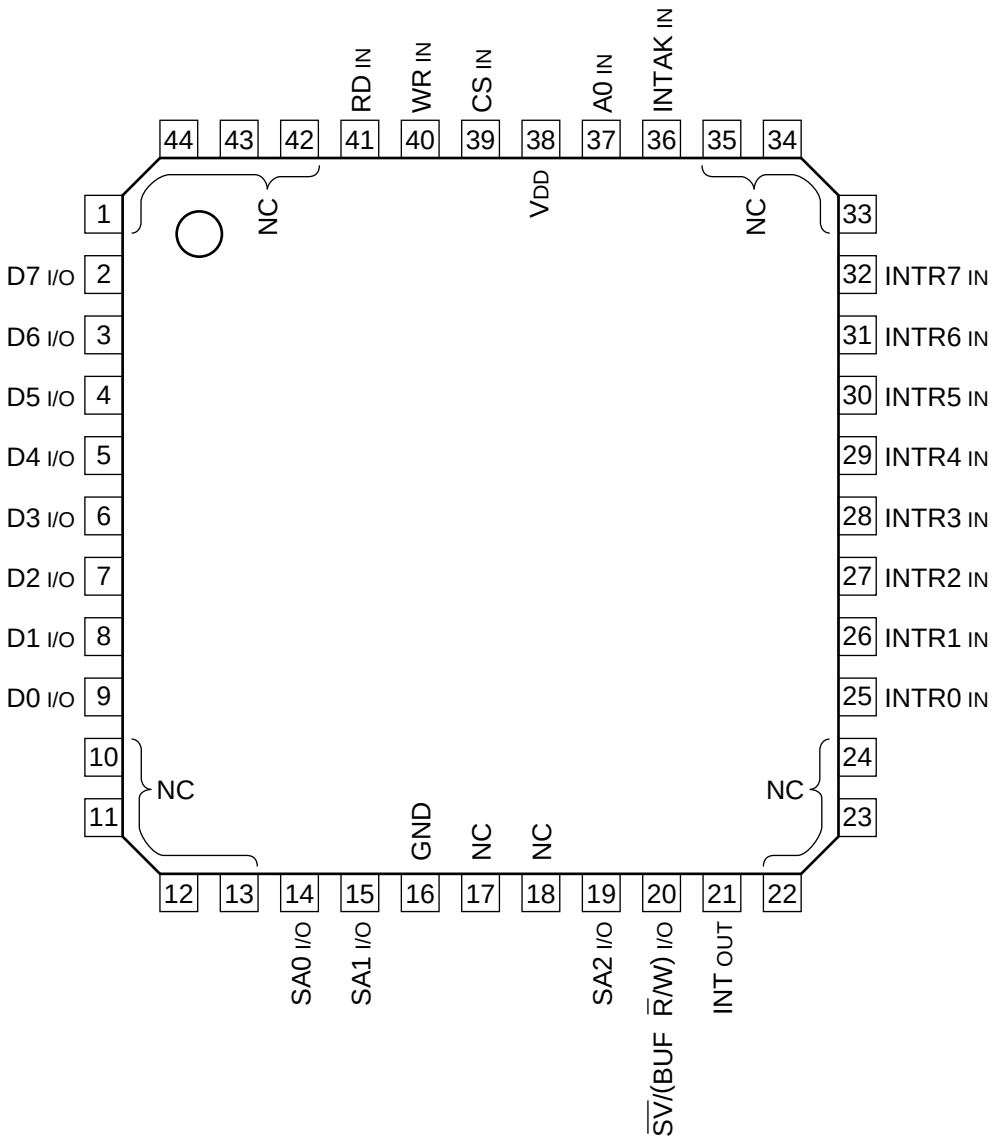
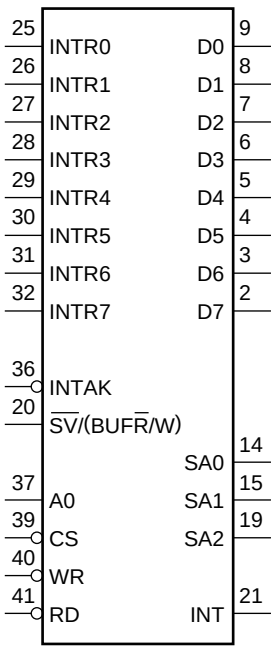
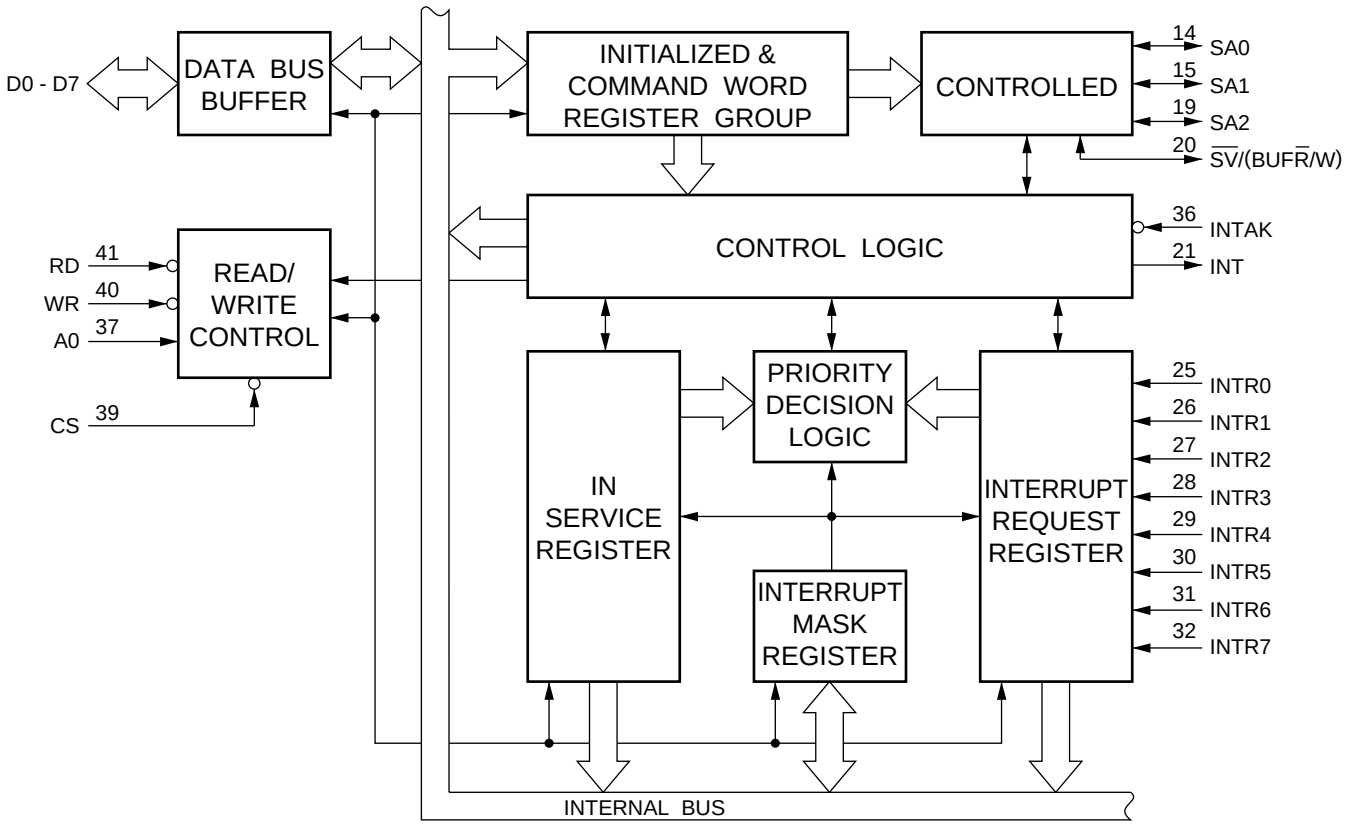
C-MOS INTERRUPT CONTROL UNIT

—TOP VIEW—





INTR0 - INTR7	:	INTERRUPT REQUEST INPUTS
D0 - D7	:	DATA BUS INPUTS/OUTPUTS
CS	:	CHIP SELECT INPUT
RD	:	READ STROBE INPUT
WR	:	WRITE STROBE INPUT
A0	:	ADDRESS INPUT
INT	:	INTERRUPT OUTPUT
INTAK	:	INTERRUPT ACKNOWLEDGE INPUT
$\overline{SV}$/(BUF$\overline{R}$/W)	:	CONTROLLED/BUFFER READ/WRITE INPUT/OUTPUT
SA0 - SA2	:	CONTROLLED ADDRESS INPUTS/OUTPUTS


D0 - D7
DATA BUS BUFFER
INITIALIZED & COMMAND WORD REGISTER GROUP
CONTROLLED
14 SA0
15 SA1
19 SA2
20 SV/(BUFR/W)
CONTROL LOGIC
36 INTAK
21 INT
RD 41
WR 40
A0 37
READ/ WRITE CONTROL
CS 39
PRIORITY DECISION LOGIC
IN SERVICE REGISTER
INTERRUPT REQUEST REGISTER
INTERRUPT MASK REGISTER
25 INTR0
26 INTR1
27 INTR2
28 INTR3
29 INTR4
30 INTR5
31 INTR6
32 INTR7
INTERNAL BUS