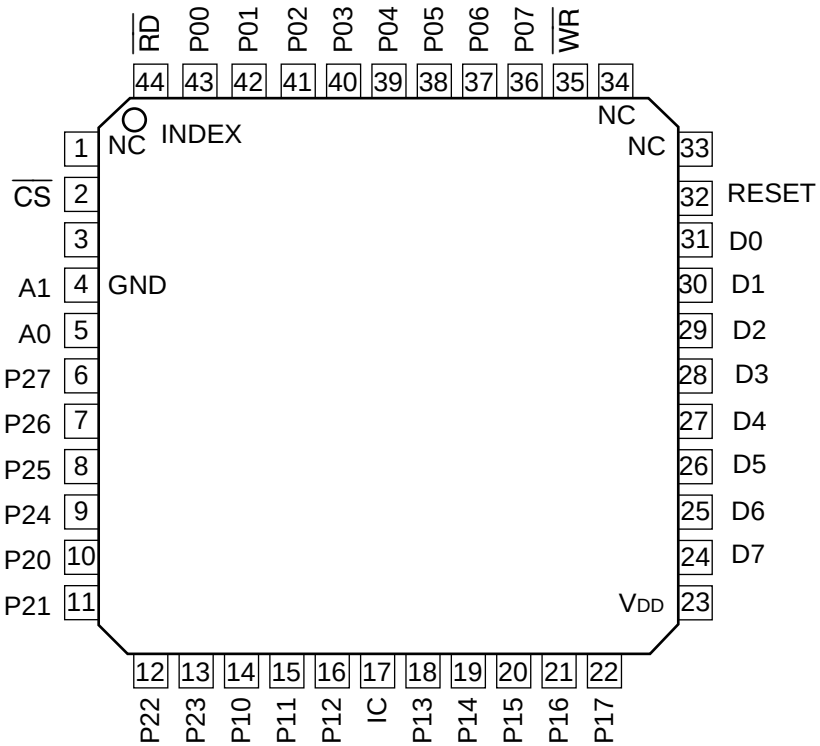
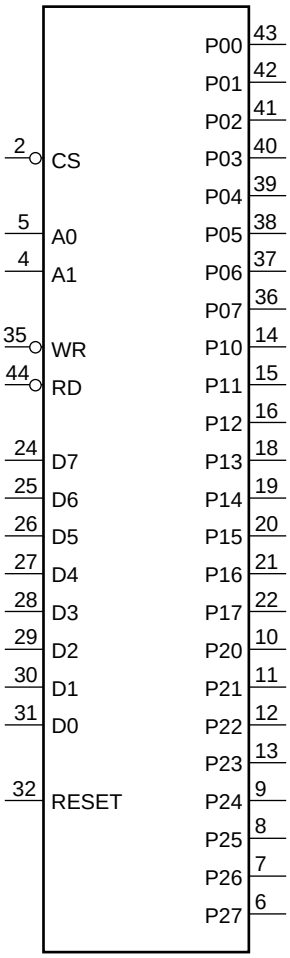
C-MOS PARALLEL INTERFACE UNIT

—TOP VIEW—





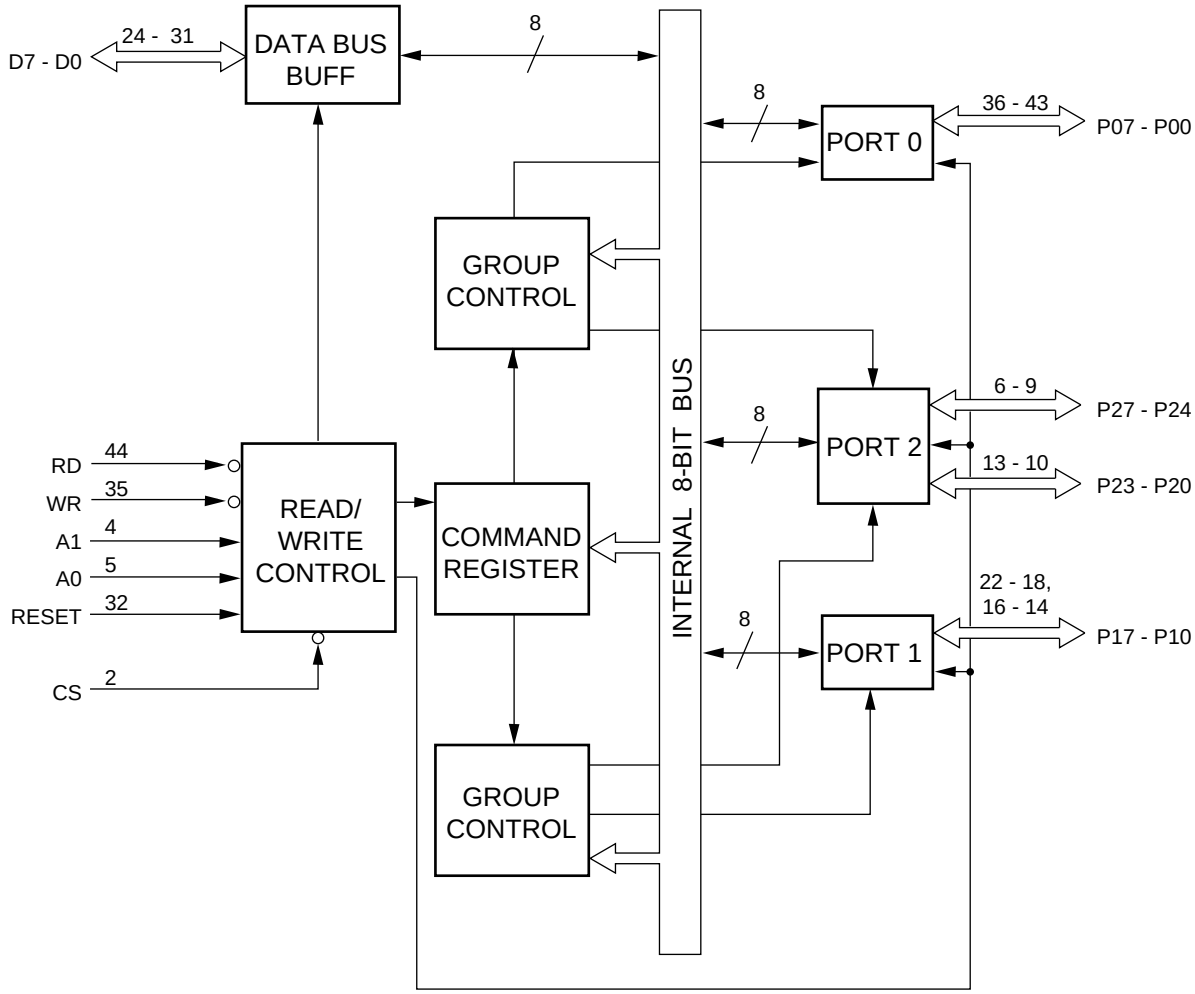
A1, A0 ; ADDRESS
$\overline{CS}$; CHIP SELECT
D7 - D0 ; DATA BUS
P07 - P00 ; PORT 0

P17 - P10 ; PORT 1
P27 - P20 ; PORT 2
$\overline{RD}$; READ STROBE
$\overline{WR}$; WRITE STROBE

IC ; INTERNALLY CONNECTED

CS	RD	WR	A1	A0	OPERATION	CPU ACTION
0	0	1	0	0	PORT0 → DATA • BUS	INPUT
0	0	1	0	1	PORT1 → DATA • BUS	INPUT
0	0	1	1	0	PORT2 → DATA • BUS	INPUT
0	0	1	1	1	DISABLE	
0	0	0	×	×		
0	1	0	0	0	DATA • BUS → PORT0	OUTPUT
0	1	0	0	1	DATA • BUS → PORT1	OUTPUT
0	1	0	1	0	DATA • BUS → PORT2	OUTPUT
0	1	0	1	1	DATA • BUS → COMMAND REGISTER	OUTPUT
0	1	1	×	×	HIGH IMPEDANCE	
1	×	×	×	×		

0 : LOW LEVEL
1 : HIGH LEVEL
× : DON'T CARE


D7 - D0
24 - 31
DATA BUS BUFF
8
INTERNAL 8-BIT BUS
8
PORT 0
36 - 43
P07 - P00
GROUP CONTROL
6 - 9
P27 - P24
8
PORT 2
13 - 10
P23 - P20
RD
44
WR
35
A1
4
A0
5
RESET
32
READ/ WRITE CONTROL
COMMAND REGISTER
22 - 18, 16 - 14
8
PORT 1
P17 - P10
CS
2
GROUP CONTROL