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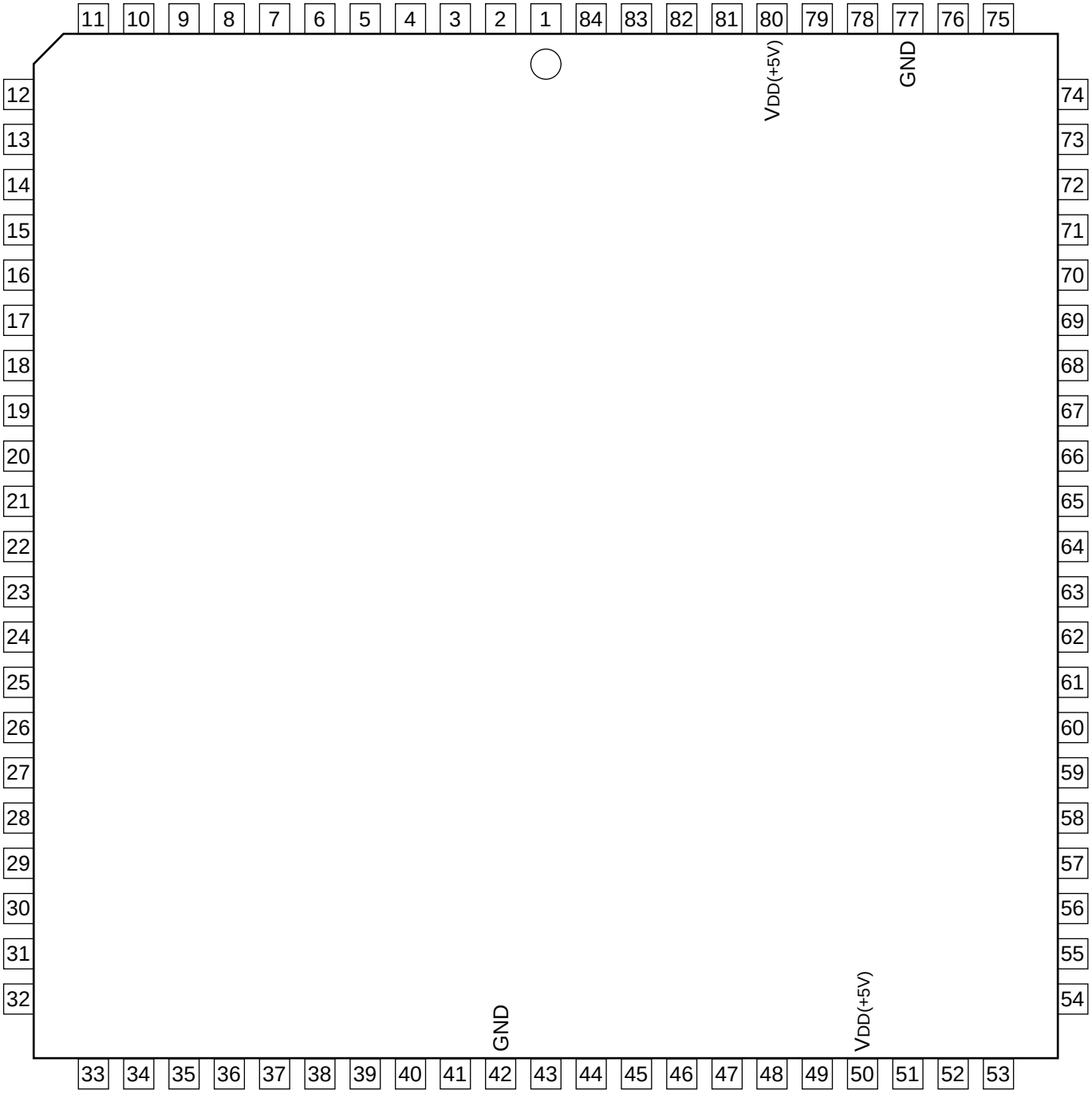
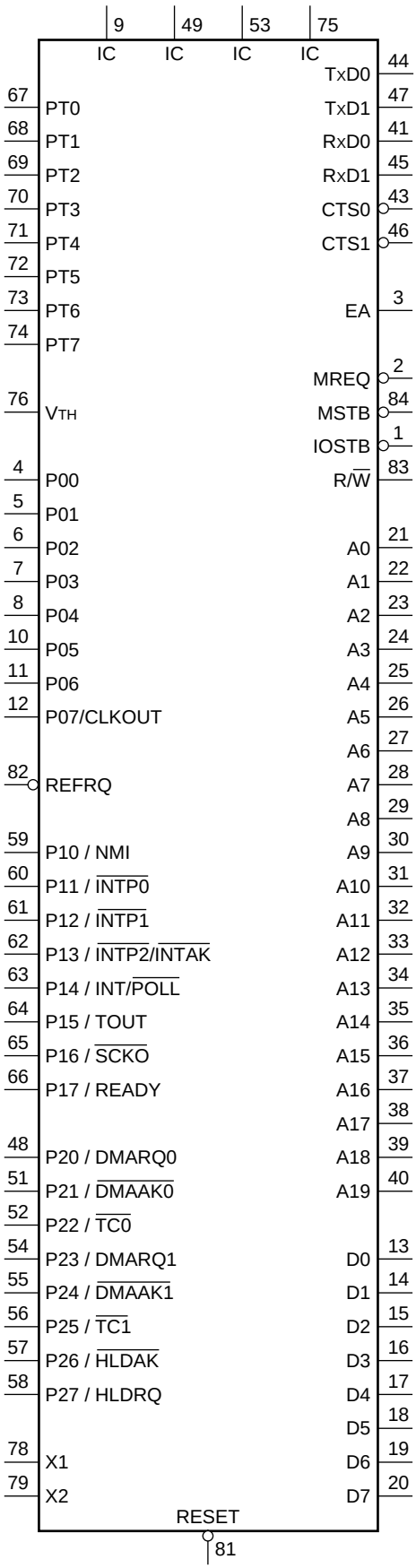
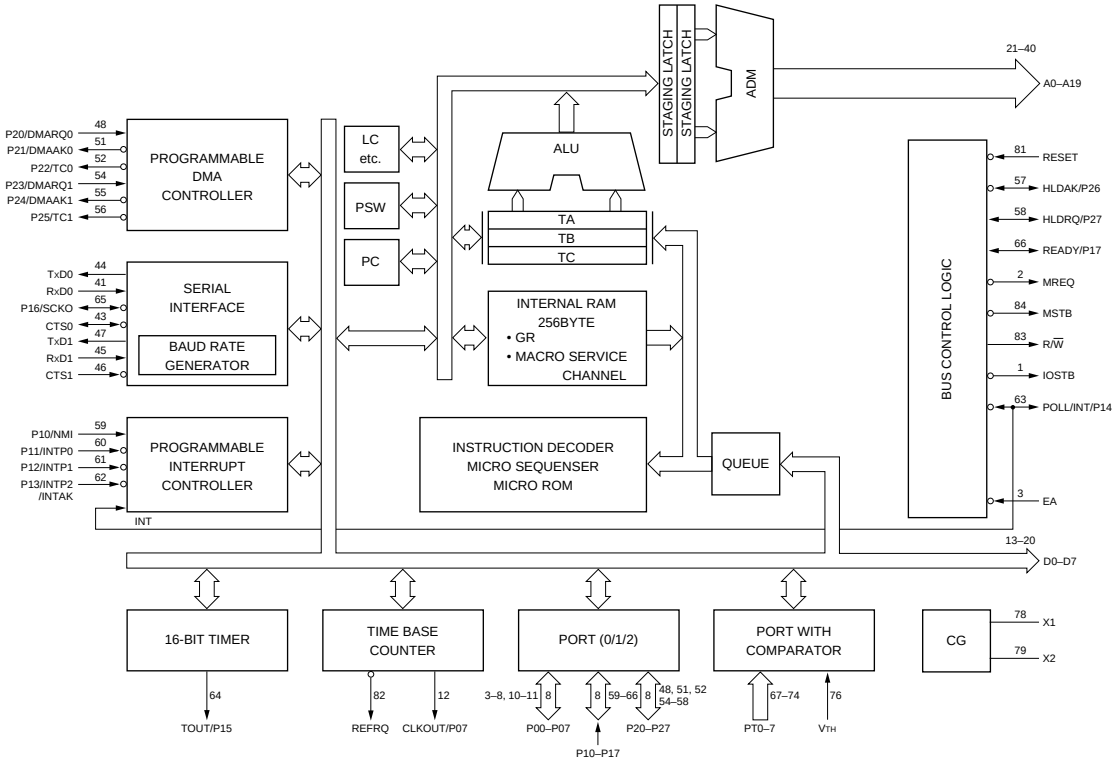
C-MOS 16-BIT MICROPROCESSOR

–TOP VIEW–





A0–A19	;	ADDRESS BUS OUTPUTS
CLKOUT	;	SYSTEM CLOCK OUTPUT
$\overline{CTS0}$, $\overline{CTS1}$	;	CLEAR TO SEND INPUT/OUTPUT
D0–D7	;	DATA BUS INPUTS/OUTPUTS
$\overline{DMAAK0}$, $\overline{DMAAK1}$	;	DMA ACKNOWLEDGE CH0, CH1 OUTPUTS
DMARQ0, DMARQ1	;	DMA REQUEST CH0, CH1 INPUTS
EA	;	ROM-LESS MODE SET INPUT
$\overline{HLDAK}$	;	HOLD ACKNOWLEDGE OUTPUT
HLDRQ	;	HOLD REQUEST INPUT
IC	;	INTERNAL CONNECT
$\overline{INTP0}$, $\overline{INTP1}$	;	INTERRUPT REQUEST INPUTS
$\overline{INTP2}$	;	INTERRUPT REQUEST INPUT
$\overline{INTAK}$	;	INTERRUPT ACKNOWLEDGE OUTPUT
$\overline{IOSTB}$	;	I/O READ/WRITE STROBE OUTPUT
$\overline{MREQ}$	;	MEMORY REQUEST OUTPUT
$\overline{MSTB}$	;	MEMORY READ/WRITE STROBE OUTPUT
NMI	;	NON-MASKABLE INTERRUPT INPUT
P00–P07	;	PORT 0 INPUTS/OUTPUTS
P10–P17	;	PORT 1 INPUTS/OUTPUTS
P20–P27	;	PORT 2 INPUTS/OUTPUTS
PT0–PT7	;	PORT 0 INPUTS
INT/$\overline{POLL}$	;	INTERRUPT REQUEST INPUT
READY	;	READY INPUT
$\overline{REFRQ}$	;	REFRESH REQUEST OUTPUT
$\overline{RESET}$	;	RESET INPUT
R/$\overline{W}$	;	READ AND WRITE CYCLE OUTPUT
RXD0, RXD1	;	SERIAL DATA INPUTS
$\overline{SCKO}$	;	SERIAL CLOCK OUTPUT
$\overline{TC0}$, $\overline{TC1}$	;	DMA (CH0/CH1) ENDING OUTPUTS
TOUT	;	TIMER OUTPUTS
TXD0, TXD1	;	SERIAL DATA OUTPUTS
VTH	;	REF. V FOR COMPARATOR INPUT
X1, X2	;	CRYSTAL 1, 2


STAGING LATCH
STAGING LATCH
ADM
21–40
A0–A19
ALU
TA
TB
TC
LC
etc.
PSW
PC
INTERNAL RAM
256BYTE
• GR
• MACRO SERVICE
CHANNEL
INSTRUCTION DECODER
MICRO SEQUENSER
MICRO ROM
QUEUE
BUS CONTROL LOGIC
81 RESET
57 HLDAK/P26
58 HLDRQ/P27
66 READY/P17
2 MREQ
84 MSTB
83 R/W
1 IOSTB
63 POLL/INT/P14
3 EA
13–20
D0–D7
P20/DMARQ0 48
P21/DMAAK0 51
P22/TC0 52
P23/DMARQ1 54
P24/DMAAK1 55
P25/TC1 56
PROGRAMMABLE
DMA
CONTROLLER
TxD0 44
RxD0 41
P16/SCKO 65
CTS0 43
TxD1 47
RxD1 45
CTS1 46
SERIAL
INTERFACE
BAUD RATE
GENERATOR
P10/NMI 59
P11/INTP0 60
P12/INTP1 61
P13/INTP2
/INTAK 62
INT
PROGRAMMABLE
INTERRUPT
CONTROLLER
16-BIT TIMER
64
TOUT/P15
TIME BASE
COUNTER
82
REFRQ
12
CLKOUT/P07
PORT (0/1/2)
3–8, 10–11 8
8
59–66 8
48, 51, 52
54–58
P00–P07
P20–P27
P10–P17
PORT WITH
COMPARATOR
67–74
PT0–7
76
VTH
CG
78 X1
79 X2

PIN NO.	I/O	SYMBOL	PIN NO.	I/O	SYMBOL	PIN NO.	I/O	SYMBOL
1	O	IOSTB	29	O	A8	57	I/O	P26/$\overline{\text{HLDAK}}$
2	O	MREQ	30	O	A9	58	I/O	P27/HLDRQ
3	I	EA	31	O	A10	59	I/O	P10/NMI
4	I/O	P00	32	O	A11	60	I/O	P11/$\overline{\text{INTP0}}$
5	I/O	P01	33	O	A12	61	I/O	P12/$\overline{\text{INTP1}}$
6	I/O	P02	34	O	A13	62	I/O	P13/$\overline{\text{INTP2}}$/$\overline{\text{INTAK}}$
7	I/O	P03	35	O	A14	63	I/O	P14/INT/$\overline{\text{POLL}}$
8	I/O	P04	36	O	A15	64	I/O	P15/TOUT
9	—	IC	37	O	A16	65	I/O	P16/$\overline{\text{SCKO}}$
10	I/O	P05	38	O	A17	66	I/O	P17/READY
11	I/O	P06	39	O	A18	67	I	PT0
12	I/O	P07/CLKOUT	40	O	A19	68	I	PT1
13	I/O	D0	41	I	RXD0	69	I	PT2
14	I/O	D1	42	—	GND	70	I	PT3
15	I/O	D2	43	I/O	CTS0	71	I	PT4
16	I/O	D3	44	O	TXD0	72	I	PT5
17	I/O	D4	45	I	RXD1	73	I	PT6
18	I/O	D5	46	I	CTS1	74	I	PT7
19	I/O	D6	47	O	TXD1	75	—	IC
20	I/O	D7	48	I/O	P20/DMARQ0	76	I	V_{TH}
21	O	A0	49	—	IC	77	—	GND
22	O	A1	50	I	V_{DD}(+5V)	78	—	X1
23	O	A2	51	I/O	P21/$\overline{\text{DMAAK0}}$	79	—	X2
24	O	A3	52	I/O	P22/$\overline{\text{TC0}}$	80	I	V_{DD}(+5V)
25	O	A4	53	—	IC	81	I	$\overline{\text{RESET}}$
26	O	A5	54	I/O	P23/DMARQ1	82	O	REFRQ
27	O	A6	55	I/O	P24/$\overline{\text{DMAAK1}}$	83	O	R/$\overline{\text{W}}$
28	O	A7	56	I/O	P25/$\overline{\text{TC1}}$	84	O	MSTB