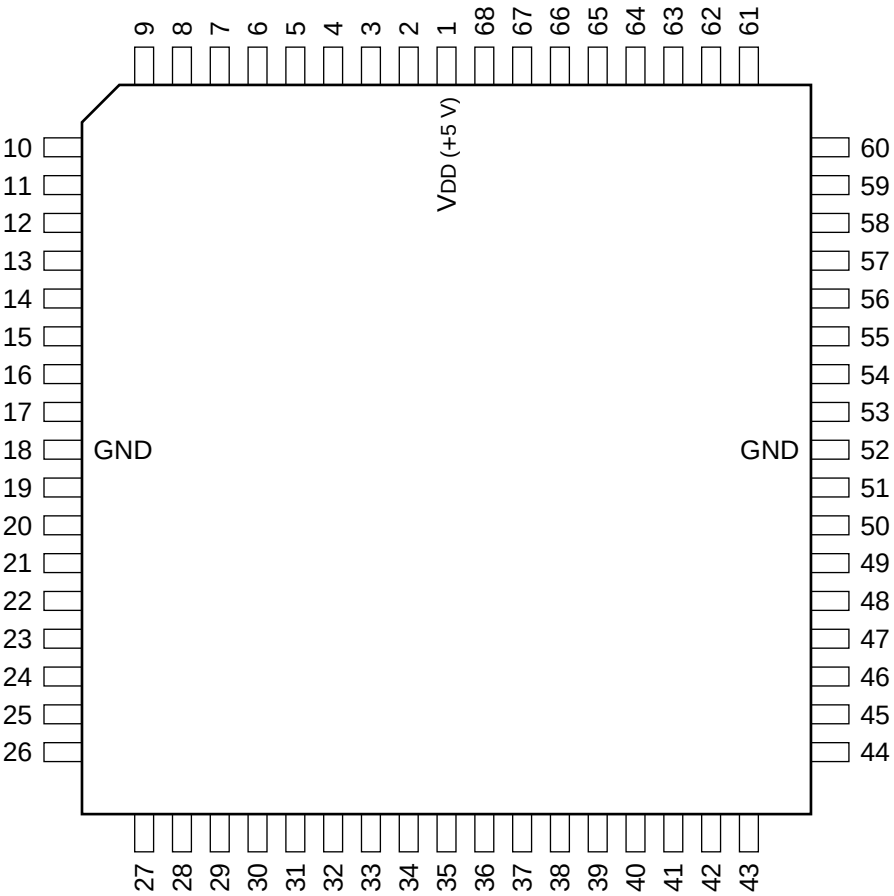
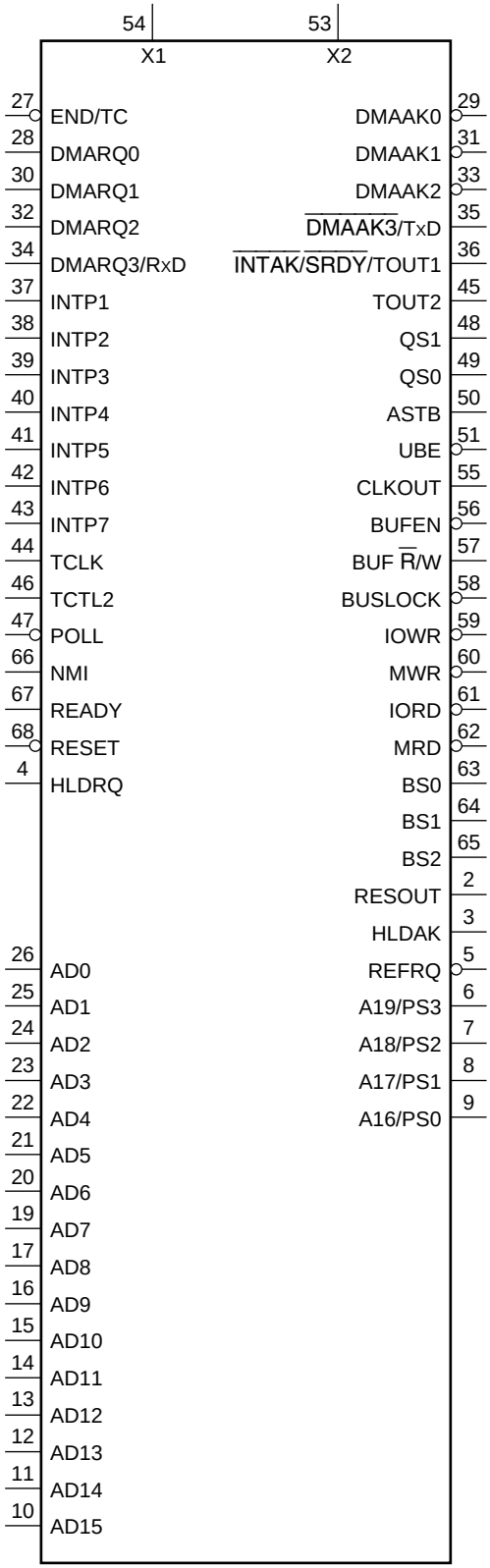
C-MOS 16-BIT MICROPROCESSOR

—TOP VIEW—



PIN No.	FUNCTION	PIN No.	FUNCTION	PIN No.	FUNCTION	PIN No.	FUNCTION
1	VDD	18	GND	35	$\overline{\text{DMAAK3}}$/TxD	52	GND
2	RESOUT	19	AD7	36	$\overline{\text{INTAK}}$/$\overline{\text{SRDY}}$/TOUT1	53	X2
3	HLDAK	20	AD6	37	INTP1	54	X1
4	HLDRQ	21	AD5	38	INTP2	55	CLKOUT
5	$\overline{\text{REFRQ}}$	22	AD4	39	INTP3	56	$\overline{\text{BUFEN}}$
6	A19/PS3	23	AD3	40	INTP4	57	BUF $\overline{\text{R}}$/W
7	A18/PS2	24	AD2	41	INTP5	58	$\overline{\text{BUSLOCK}}$
8	A17/PS1	25	AD1	42	INTP6	59	$\overline{\text{IOWR}}$
9	A16/PS0	26	AD0	43	INTP7	60	$\overline{\text{MWR}}$
10	AD15	27	$\overline{\text{END}}$/$\overline{\text{TC}}$	44	TCLK	61	$\overline{\text{IORD}}$
11	AD14	28	DMARQ0	45	TOUT2	62	$\overline{\text{MRD}}$
12	AD13	29	$\overline{\text{DMAAK0}}$	46	TCTL2	63	BS0
13	AD12	30	DMARQ1	47	$\overline{\text{POLL}}$	64	BS1
14	AD11	31	$\overline{\text{DMAAK1}}$	48	QS1	65	BS2
15	AD10	32	DMARQ2	49	QS0	66	NMI
16	AD9	33	$\overline{\text{DMAAK2}}$	50	ASTB	67	READY
17	AD8	34	DMARQ3/RxD	51	$\overline{\text{UBE}}$	68	$\overline{\text{RESET}}$


54
X1
53
X2
27 END/TC
28 DMARQ0
30 DMARQ1
32 DMARQ2
34 DMARQ3/RxD
37 INTP1
38 INTP2
39 INTP3
40 INTP4
41 INTP5
42 INTP6
43 INTP7
44 TCLK
46 TCTL2
47 POLL
66 NMI
67 READY
68 RESET
4 HLDRQ
26 AD0
25 AD1
24 AD2
23 AD3
22 AD4
21 AD5
20 AD6
19 AD7
17 AD8
16 AD9
15 AD10
14 AD11
13 AD12
12 AD13
11 AD14
10 AD15
29 DMAAK0
31 DMAAK1
33 DMAAK2
35 DMAAK3/TxD
36 INTAK/SRDY/TOUT1
45 TOUT2
48 QS1
49 QS0
50 ASTB
51 UBE
55 CLKOUT
56 BUFEN
57 BUF R/W
58 BUSLOCK
59 IOWR
60 MWR
61 IORD
62 MRD
63 BS0
64 BS1
65 BS2
2 RESOUT
3 HLDAK
5 REFRQ
6 A19/PS3
7 A18/PS2
8 A17/PS1
9 A16/PS0

INPUT

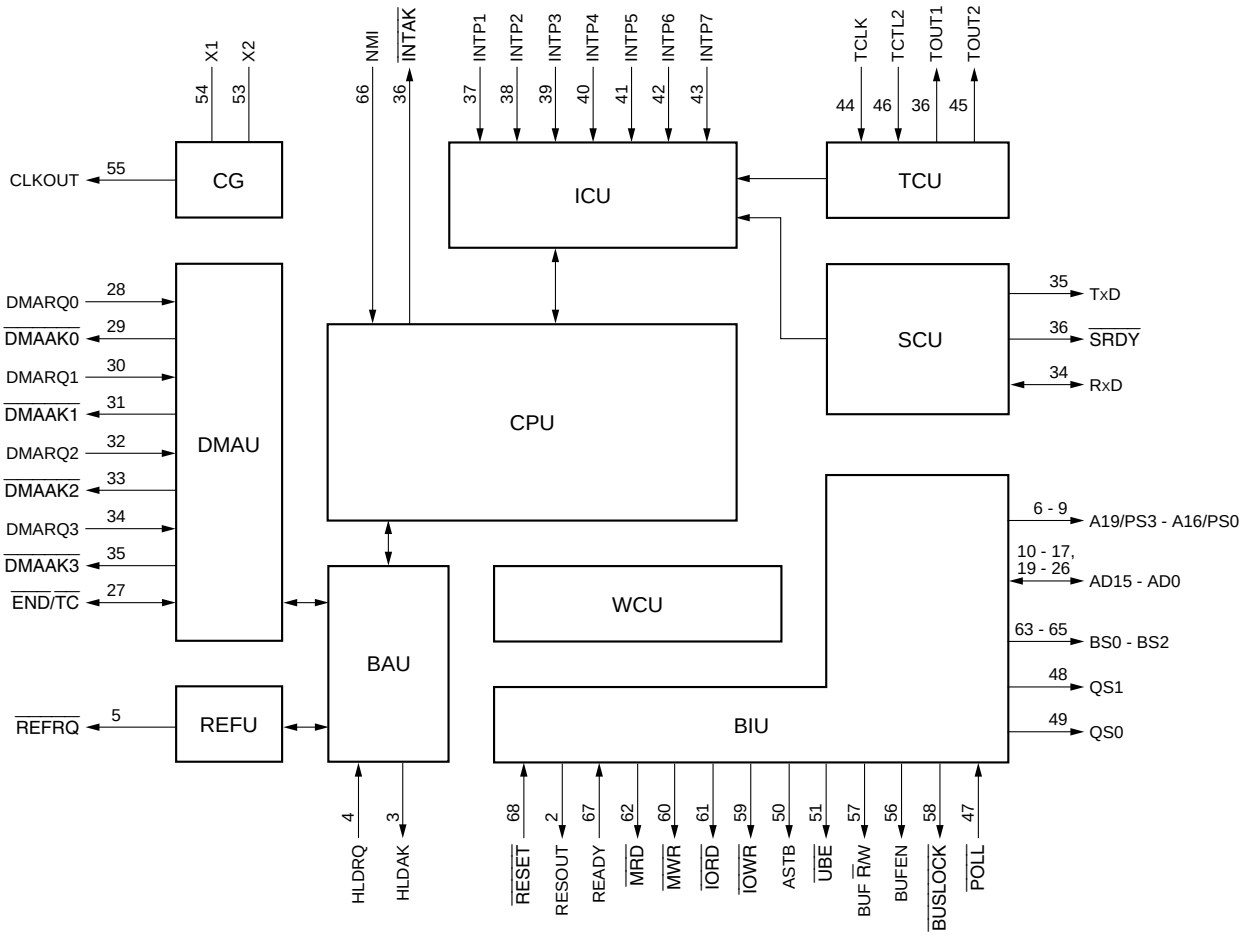
DMARQ0 - DMARQ2	:	DMA REQUEST 0 - 2
DMARQ3/RxD	:	DMA REQUEST/RECEIVE DATA
HLDRQ	:	BUS HOLD REQUEST
INTP0 - INTP7	:	INTERRUPT REQUEST FROM PERIPHERAL 0 - 7
NMI	:	NON MASKABLE INTERRUPT
POLL	:	POLL
READY	:	READY
RESET	:	RESET
TCLK	:	TIMER CLOCK
TCTL2	:	TIMER CONTROL 2
X1, X2	:	CRYSTAL 1, 2

OUTPUT

A16/PS0 - A19/PS3	:	ADDRESS/PROCESSOR STATUS
ASTB	:	ADDRESS STROBE
BS0 - BS2	:	BUS STATUS
BUFEN	:	BUFFER ENABLE
BUF $\overline{R}$/W	:	BUFFER READ/WRITE
BUSLOCK	:	BUS LOCK
CLKOUT	:	CLOCK
$\overline{DMAAK0}$ - $\overline{DMAAK2}$	:	DMA ACKNOWLEDGE 0 - 2
$\overline{DMAAK3}$/TxD	:	DMA ACKNOWLEDGE 3/TRANSMIT DATA
$\overline{HLDAK}$	:	BUS HOLD ACKNOWLEDGE
$\overline{INTAK}$/$\overline{SRDY}$/TOUT1	:	INTERRUPT ACKNOWLEDGE/SERIAL READY/TIMER OUT 1
IORD	:	I/O READ STROBE
IOWR	:	I/O WRITE STROBE
MRD	:	MEMORY READ STROBE
MWR	:	MEMORY WRITE STROBE
QS0, QS1	:	QUEUE STATUS
REFRQ	:	REFRESH REQUEST
RESOUT	:	SYSTEM RESET
TOUT2	:	TIMER OUT 2
UBE	:	UPPER BYTE ENABLE

INPUT/OUTPUT

AD0 - AD15	:	ADDRESS BUS/DATA BUS
END/TC	:	END/TERMINAL COUNT


X1
X2
54
53
NMI
INTAK
66
36
INTP1
INTP2
INTP3
INTP4
INTP5
INTP6
INTP7
37
38
39
40
41
42
43
TCLK
TCTL2
TOUT1
TOUT2
44
46
36
45
CLKOUT
55
CG
ICU
TCU
DMARQ0
28
DMAAK0
29
DMARQ1
30
DMAAK1
31
DMARQ2
32
DMAAK2
33
DMARQ3
34
DMAAK3
35
END/TC
27
DMAU
CPU
SCU
35
TxD
36
SRDY
34
RxD
6 - 9
A19/PS3 - A16/PS0
10 - 17,
19 - 26
AD15 - AD0
63 - 65
BS0 - BS2
48
QS1
49
QS0
WCU
BAU
REFRQ
5
REFU
BIU
4
3
HLDRQ
HLDAK
68
2
67
62
60
61
59
50
51
57
56
58
47
RESET
RESOUT
READY
MRD
MWR
IORD
IOWR
ASTB
UBE
BUF R/W
BUFEN
BUSLOCK
POLL