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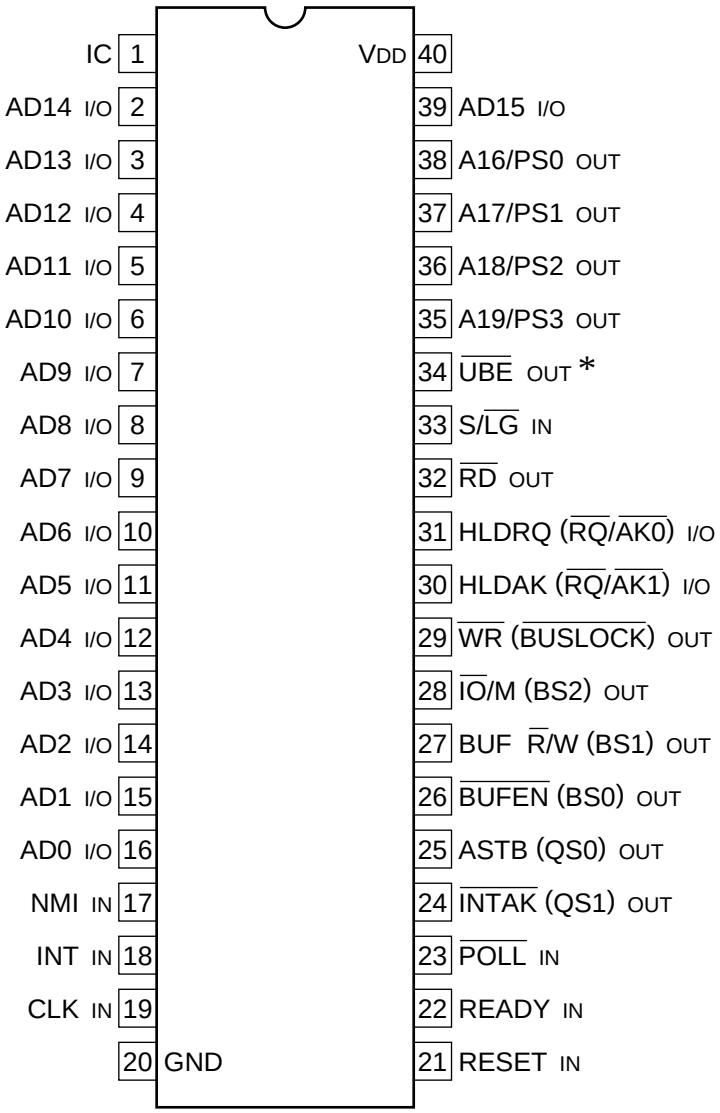
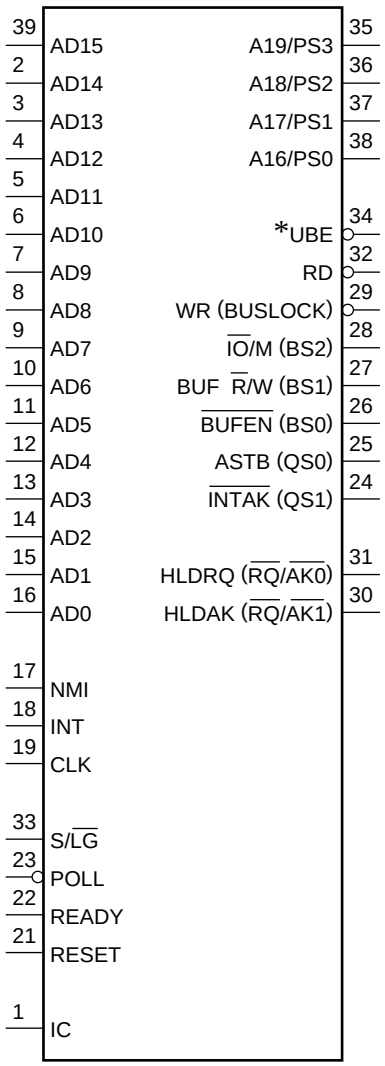
# C-MOS 16-BIT MICROPROCESSOR

—TOP VIEW—




| TYPE | VDD |
|---|---|
| UPD70108, 70116 | +5V |
| UPD70108H, 70116H | +5 or +3V |

* UPD70108, 70108H ; LBS0 (HIGH) OUT
UPD70116, 70116H ; UBE OUT

| PIN NO. | FUNCTION | |
|---|---|---|
| | S/LG=HIGH LEVEL | S/LG=LOW LEVEL |
| 24 | INTAK | QS1 |
| 25 | ASTB | QS0 |
| 26 | BUFEN | BS0 |
| 27 | BUF R/W | BS1 |
| 28 | IO/M | BS2 |
| 29 | WR | BUSLOCK |
| 30 | HLDAK | RQ/AK1 |
| 31 | HLDRQ | RQ/AK0 |
| 34 | LBS0 (UPD70108/H) | HIGH LEVEL |

**INPUT**

| | | |
|---|---|---|
| CLK | ; | CLOCK |
| HLDRQ | ; | HOLD REQUEST |
| INT | ; | MASKABLE INTERRUPT |
| NMI | ; | NON-MASKABLE INTERRUPT |
| $\overline{\text{POLL}}$ | ; | POLL CHECK |
| READY | ; | READ/WRITE CYCLE EXPANDER |
| RESET | ; | CPU RESET |
| S/$\overline{\text{LG}}$ | ; | SMALL/LARGE |

**OUTPUT**

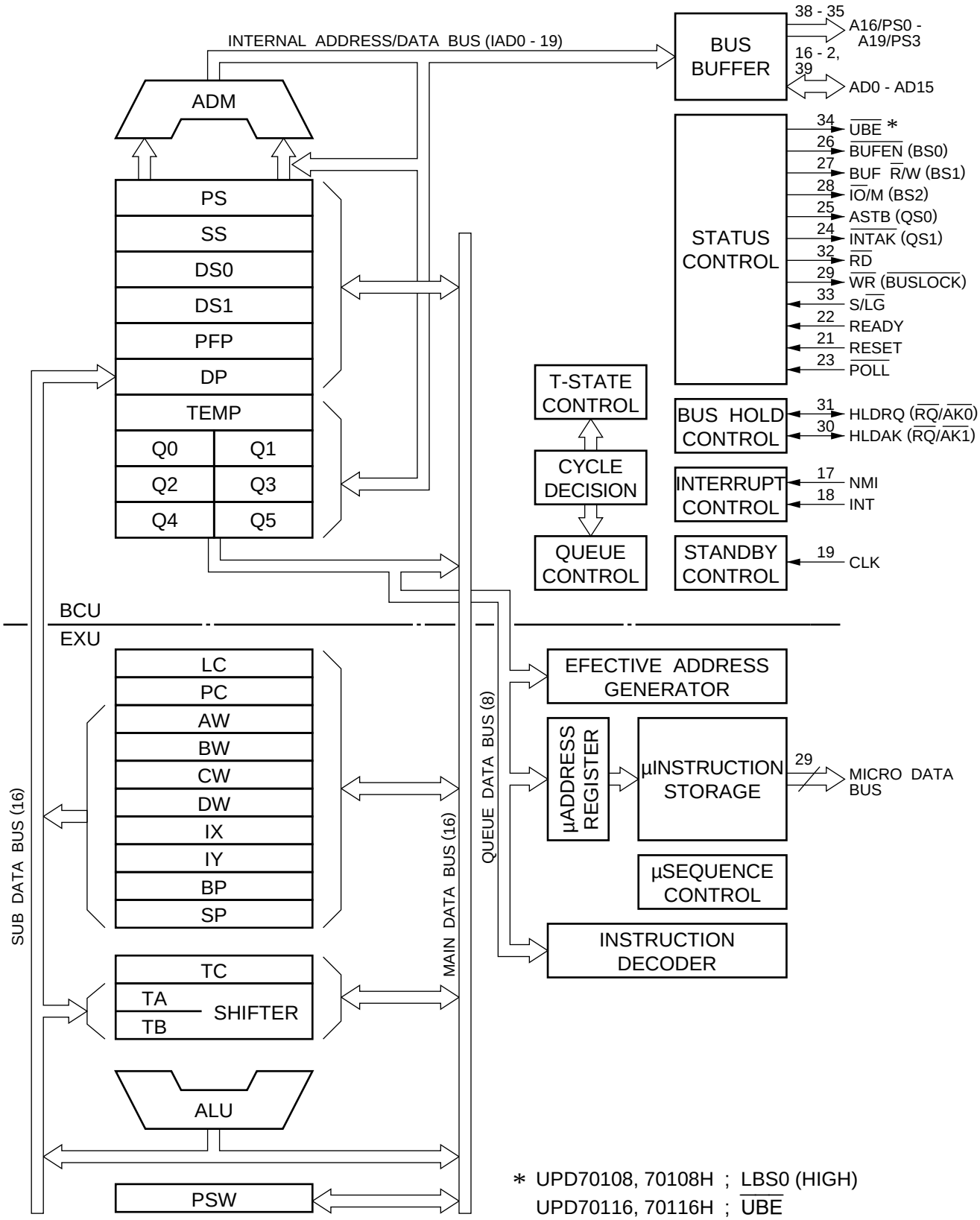
| | | |
|---|---|---|
| A16/PS0 - A19/PS3 | ; | ADDRESS BUS/PROCESSOR STATUS |
| ASTB | ; | ADDRESS STROBE |
| BS0 - BS2 | ; | BUS STATUS |
| $\overline{\text{BUFEN}}$ | ; | BUFFER ENABLE |
| BUF $\overline{\text{R}}$/W | ; | BUFFER READ/WRITE |
| $\overline{\text{BUSLOCK}}$ | ; | BUS LOCK |
| HLDAK | ; | HOLD ACKNOWLEDGE |
| $\overline{\text{INTAK}}$ | ; | INTERRUPT ACKNOWLEDGE |
| $\overline{\text{IO}}$/M | ; | IO/MEMORY |
| LBS0 | ; | LATCHED BUS STATUS 0 (UPD70108/H) |
| QS0, QS1 | ; | QUEUE STATUS |
| $\overline{\text{RD}}$ | ; | READ STROBE |
| $\overline{\text{UBE}}$ | ; | UPPER BYTE ENABLE (UPD70116/H) |
| $\overline{\text{WR}}$ | ; | WRITE STROBE |

**INPUT/OUTPUT**

| | | |
|---|---|---|
| AD0 - AD15 | ; | ADDRESS/DATA BUS |
| $\overline{\text{RQ}}$/AK0, $\overline{\text{RQ}}$/AK1 | ; | HOLD REQUEST IN/ACKNOWLEDGE OUT |

**OTHER**

| | | |
|---|---|---|
| IC | ; | INTERNALLY CONNECTED |




* UPD70108, 70108H ; LBS0 (HIGH)
UPD70116, 70116H ; $\overline{\text{UBE}}$