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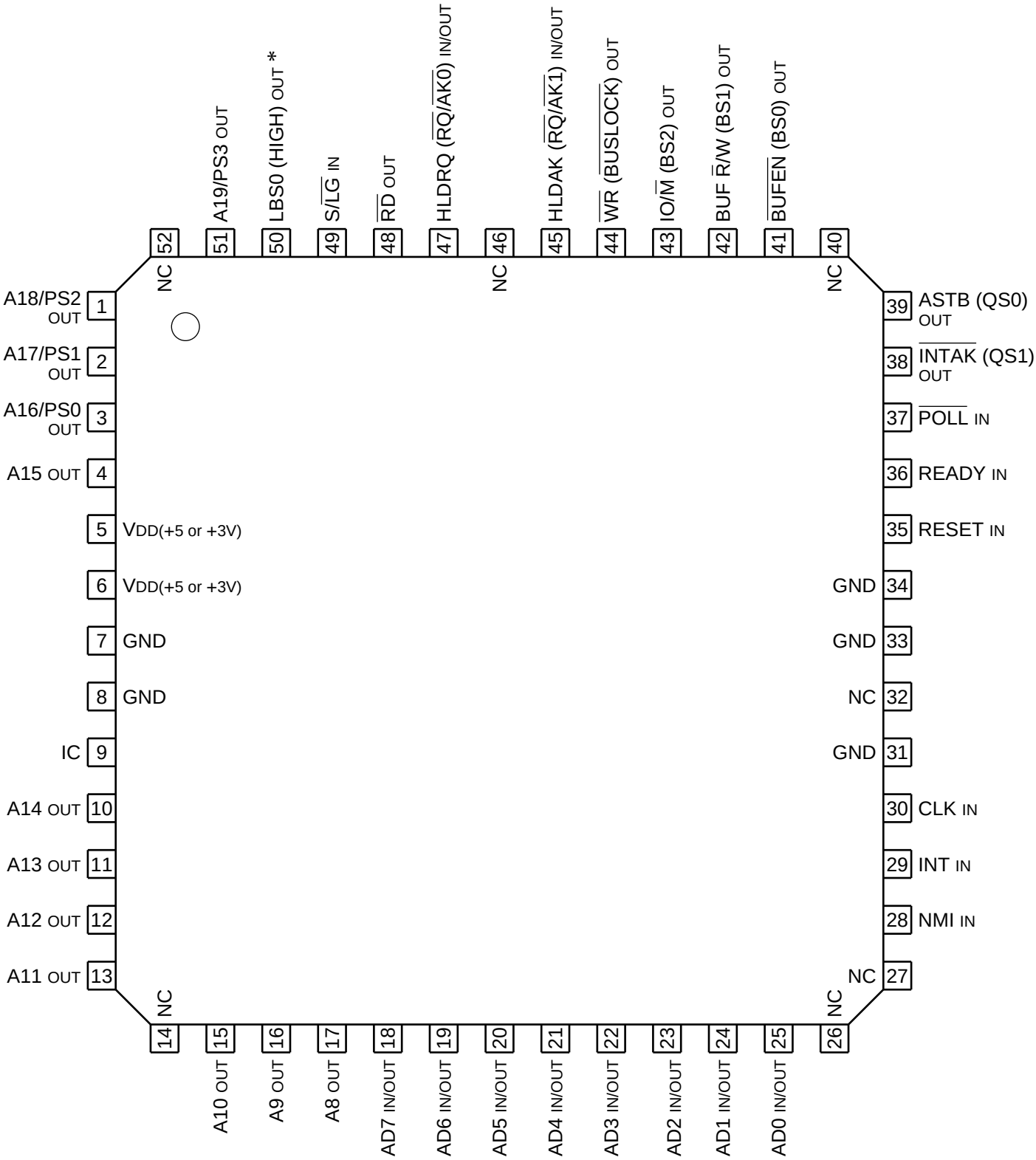
C-MOS 8-BIT MICROPROCESSOR

—TOP VIEW—



TYPE	VDD
UPD70108, 70116	+5V
UPD70108H, 70116H	+5 or +3V

* UPD70108, 70108H ; LBS0 (HIGH) OUT
UPD70116, 70116H ; UBE OUT

PIN NO.	FUNCTION	
	S/$\overline{LG}$=HIGH LEVEL	S/$\overline{LG}$=LOW LEVEL
38	$\overline{INTAK}$	QS1
39	ASTB	QS0
41	$\overline{BUFEN}$	BS0
42	BUF $\overline{R}$/W	BS1
43	IO/$\overline{M}$	BS2
44	$\overline{WR}$	$\overline{BUSLOCK}$
45	HLDAK	$\overline{RQ}$/$\overline{AK1}$
47	HLDRQ	$\overline{RQ}$/$\overline{AK0}$
50	LBS0 (UPD70108/H)	HIGH LEVEL

INPUT

CLK ; CLOCK
HLDRQ ; HOLD REQUEST
INT ; MASKABLE INTERRUPT
NMI ; NON-MASKABLE INTERRUPT
$\overline{POLL}$; POLL CHECK
READY ; READ/WRITE CYCLE EXPANDER
RESET ; CPU RESET
S/$\overline{LG}$; SMALL/LARGE

OUTPUT

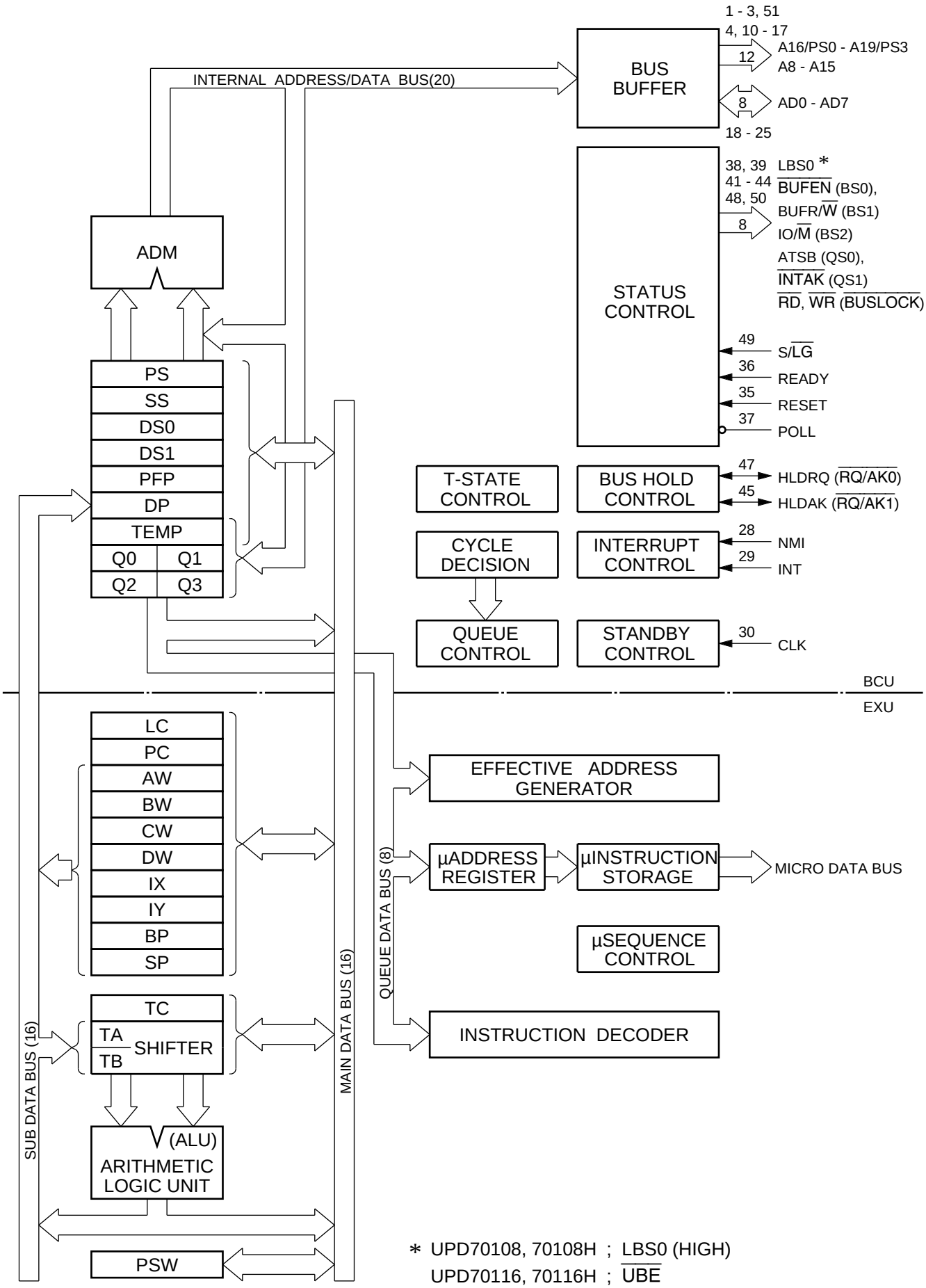
A16/PS0 - A19/PS3 ; ADDRESS BUS/PROCESSOR STATUS
ASTB ; ADDRESS STROBE
BS0 - BS2 ; BUS STATUS
$\overline{BUFEN}$; BUFFER ENABLE
BUF $\overline{R}$/W ; BUFFER READ/WRITE
$\overline{BUSLOCK}$; BUS LOCK
HLDAK ; HOLD ACKNOWLEDGE
$\overline{INTAK}$; INTERRUPT ACKNOWLEDGE
$\overline{IO}$/M ; IO/MEMORY
LBS0 ; LATCHED BUS STATUS 0 (UPD70108/H)
QS0, QS1 ; QUEUE STATUS
$\overline{RD}$; READ STROBE
$\overline{UBE}$; UPPER BYTE ENABLE (UPD70116/H)
$\overline{WR}$; WRITE STROBE

INPUT/OUTPUT

AD0 - AD15 ; ADDRESS/DATA BUS
$\overline{RQ}$/AK0, $\overline{RQ}$/AK1 ; HOLD REQUEST IN/ACKNOWLEDGE OUT

OTHER

IC ; INTERNALLY CONNECTED



* UPD70108, 70108H ; LBS0 (HIGH)
UPD70116, 70116H ; $\overline{UBE}$