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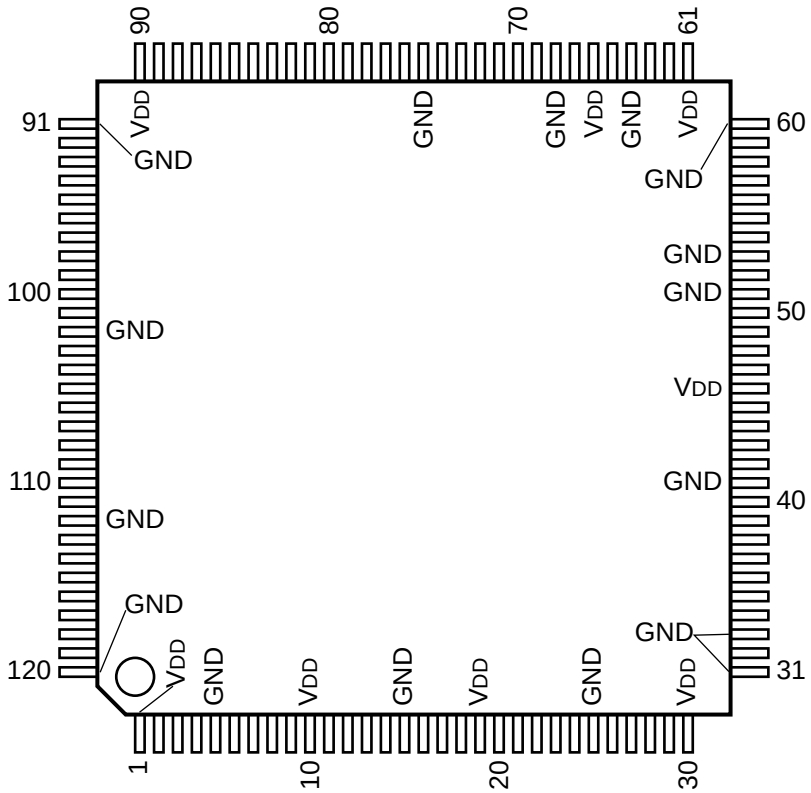
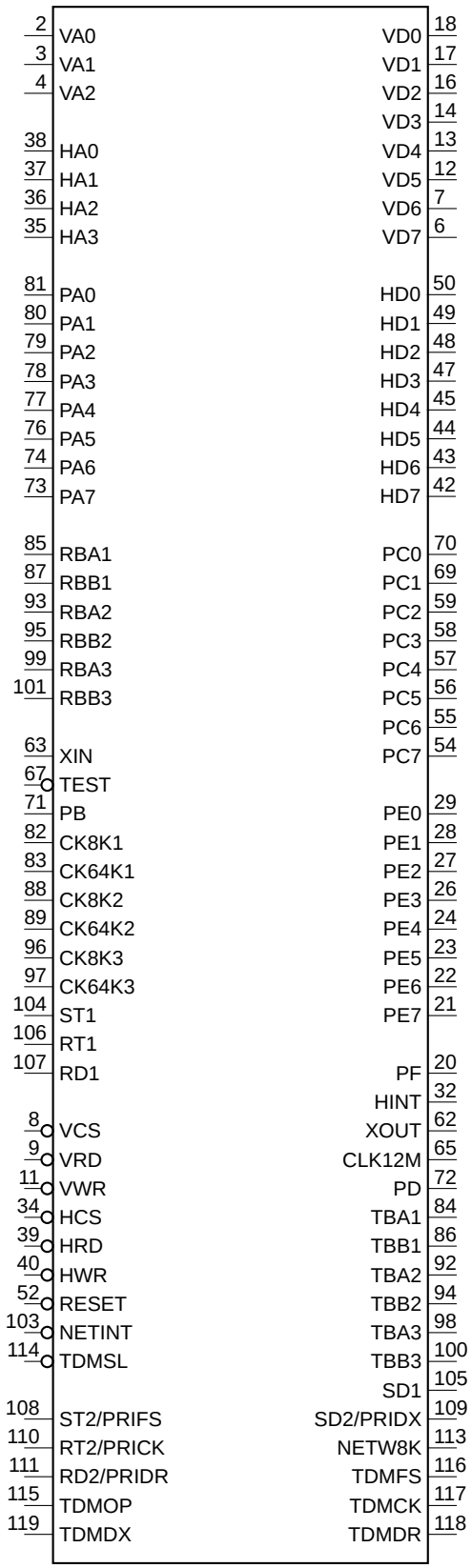
NETW-VCP INTERFACE

–TOP VIEW–




2 VA0
3 VA1
4 VA2
38 HA0
37 HA1
36 HA2
35 HA3
81 PA0
80 PA1
79 PA2
78 PA3
77 PA4
76 PA5
74 PA6
73 PA7
85 RBA1
87 RBB1
93 RBA2
95 RBB2
99 RBA3
101 RBB3
63 XIN
67 TEST
71 PB
82 CK8K1
83 CK64K1
88 CK8K2
89 CK64K2
96 CK8K3
97 CK64K3
104 ST1
106 RT1
107 RD1
8 VCS
9 VRD
11 VWR
34 HCS
39 HRD
40 HWR
52 RESET
103 NETINT
114 TDMSL
108 ST2/PRIFS
110 RT2/PRICK
111 RD2/PRIDR
115 TDMOP
119 TDMDX
18 VD0
17 VD1
16 VD2
14 VD3
13 VD4
12 VD5
7 VD6
6 VD7
50 HD0
49 HD1
48 HD2
47 HD3
45 HD4
44 HD5
43 HD6
42 HD7
70 PC0
69 PC1
59 PC2
58 PC3
57 PC4
56 PC5
55 PC6
54 PC7
29 PE0
28 PE1
27 PE2
26 PE3
24 PE4
23 PE5
22 PE6
21 PE7
20 PF
32 HINT
62 XOUT
65 CLK12M
72 PD
84 TBA1
86 TBB1
92 TBA2
94 TBB2
98 TBA3
100 TBB3
105 SD1
109 SD2/PRIDX
113 NETW8K
116 TDMFS
117 TDMCK
118 TDMDR

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	V_{DD}	31	—	GND	61	—	V_{DD}	91	—	GND
2	I	VA0	32	O	HINT	62	O	X_{OUT}	92	O	TBA2
3	I	VA1	33	—	GND	63	I	X_{IN}	93	I	RBA2
4	I	VA2	34	I	$\overline{HCS}$	64	—	GND	94	O	TBB2
5	—	GND	35	I	HA3	65	O	CLK12M	95	I	RBB2
6	I/O	VD7	36	I	HA2	66	—	V_{DD}	96	I	CK8K3
7	I/O	VD6	37	I	HA1	67	I	$\overline{TEST}$	97	I	CK64K3
8	I	$\overline{VCS}$	38	I	HA0	68	—	GND	98	O	TBA3
9	I	$\overline{VRD}$	39	I	$\overline{HRD}$	69	O	PC1	99	I	RBA3
10	—	V_{DD}	40	I	$\overline{HWR}$	70	O	PC0	100	O	TBB3
11	I	$\overline{VWR}$	41	—	GND	71	I	PB	101	I	RBB3
12	I/O	VD5	42	I/O	HD7	72	O	PD	102	—	GND
13	I/O	VD4	43	I/O	HD6	73	I	PA7	103	I	$\overline{NETINT}$
14	I/O	VD3	44	I/O	HD5	74	I	PA6	104	I	ST1
15	—	GND	45	I/O	HD4	75	—	GND	105	O	SD1
16	I/O	VD2	46	—	V_{DD}	76	I	PA5	106	I	RT1
17	I/O	VD1	47	I/O	HD3	77	I	PA4	107	I	RD1
18	I/O	VD0	48	I/O	HD2	78	I	PA3	108	I	ST2/PRIFS
19	—	V_{DD}	49	I/O	HD1	79	I	PA2	109	O	SD2/PRIDX
20	O	PF	50	I/O	HD0	80	I	PA1	110	I	RT2/PRICK
21	O	PE7	51	—	GND	81	I	PA0	111	I	RD2/PRIDR
22	O	PE6	52	I	$\overline{RESET}$	82	I	CK8K1	112	—	GND
23	O	PE5	53	—	GND	83	I	CK64K1	113	O	NETW8K
24	O	PE4	54	O	PC7	84	O	TBA1	114	I	$\overline{TDMSL}$
25	—	GND	55	O	PC6	85	I	RBA1	115	I	TDMOP
26	O	PE3	56	O	PC5	86	O	TBB1	116	O	TDMFS
27	O	PE2	57	O	PC4	87	I	RBB1	117	O	TDMCK
28	O	PE1	58	O	PC3	88	I	CK8K2	118	O	TDMDR
29	O	PE0	59	O	PC2	89	I	CK64K2	119	I	TDMDX
30	—	V_{DD}	60	—	GND	90	—	V_{DD}	120	—	GND

INPUT

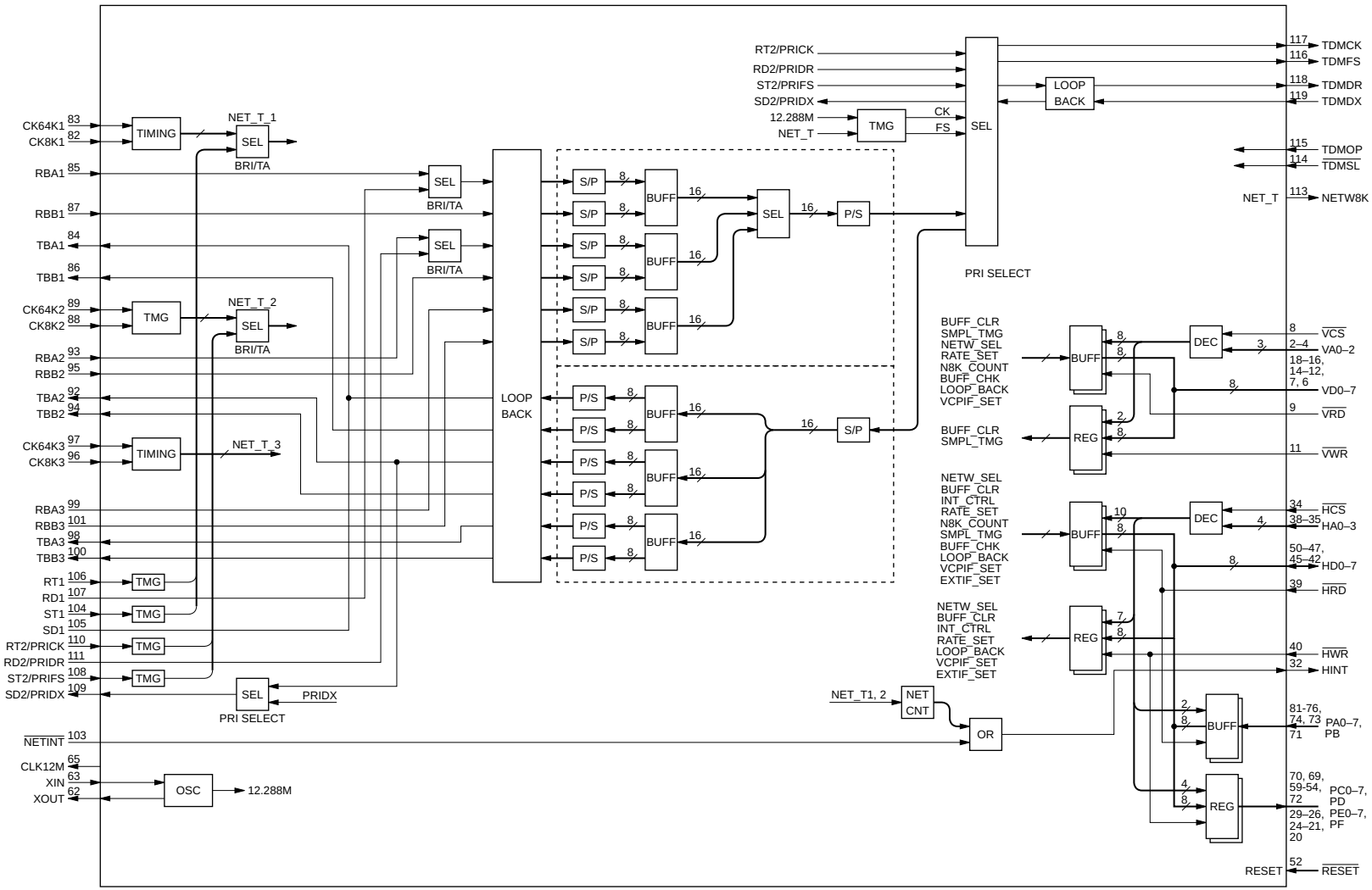
CK64K1–3 ; EACH 64kHz CLOCK FOR ISDN BRI
CK8K1–3 ; EACH 8kHz (OCTET TIMING) CLOCK FOR ISDN BRI
HA0–3 ; ADDRESS FROM THE HOST CPU
$\overline{\text{HCS}}$; CHIP SELECT FROM THE HOST CPU
$\overline{\text{HRD}}$; READ ENABLE FROM THE HOST CPU
$\overline{\text{HWR}}$; WRITE PULSE FROM THE HOST CPU
$\overline{\text{NETINT}}$; INTERRUPT
PA0–7, PB ; INPUT PORTS
RBA1–3, RBB1–3 ; EACH RECEIVING DATA FOR ISDN BRI
RD1 ; RECEIVING DATA FOR EXCLUSIVE USE LINE (TA) I/F
RD2/PRIDR ; RECEIVING DATA FOR EXCLUSIVE USE LINE (TA) I/F
$\overline{\text{RESET}}$; RESET
RT1 ; RECEIVING TIMING FOR EXCLUSIVE USE LINE (TA) I/F
RT2/PRICK ; RECEIVING TIMING FOR EXCLUSIVE USE LINE (TA) I/F
ST1 ; TRANSMITTING TIMING FOR EXCLUSIVE USE LINE (TA) I/F
ST2/PRIFS ; TRANSMITTING TIMING FOR EXCLUSIVE USE LINE (TA) I/F
TDMDX ; SERIAL DATA FOR TDM BUS
$\overline{\text{TEST}}$; TEST MODE SETTING TERMINAL
TDMOP ; SERIAL DATA FROM THE SECOND VCP
$\overline{\text{TDMSL}}$; IN PRI MODE, DURING THIS TERMINAL IS ACTIVE, TREATS DATA FROM TDMDR AS INPUT SIGNAL FROM TDMOP
VA0–2 ; ADDRESS FROM VCP
$\overline{\text{VCS}}$; CHIP SELECT FROM VCP
$\overline{\text{VRD}}$; READ ENABLE FROM VCP
$\overline{\text{VWR}}$; WRITE PULSE FROM VCP
XIN ; CRYSTAL OSCILLATOR (12.288MHz)

OUTPUT

CLK12M ; 12.288MHz CLOCK
HINT ; INTERRUPT TO THE HOST CPU
NETW8K ; 8kHz PULSE SIGNAL DIVIDE CIRCUIT CLOCK
PC0–7, PD, PE0–7, PF ; OUTPUT PORTS
SD1 ; TRANSMITTING DATA FOR EXCLUSIVE USE LINE (TA) I/F
SD2/PRIDX ; TRANSMITTING DATA FOR EXCLUSIVE USE LINE (TA) I/F
TBA1–3, TBB1–3 ; EACH TRANSMITTING DATA FOR ISDN BRI
TDMCK ; CLOCK (3.072MHz) FOR TDM BUS
TDMDR ; SERIAL DATA FOR TDM BUS
TDMFS ; FRAME SYNC (8kHz) FOR TDM BUS
XOUT ; CRYSTAL OSCILLATOR (12.288MHz)

INPUT/OUTPUT

HD0–7 ; DATA BUS FROM THE HOST CPU
VD0–7 ; DATA BUS FROM VCP


CK64K1 83
CK8K1 82
TIMING
NET_T_1
SEL
BRI/TA
RBA1 85
RBB1 87
TBA1 84
TBB1 86
SEL
BRI/TA
SEL
BRI/TA
CK64K2 89
CK8K2 88
TMG
NET_T_2
SEL
BRI/TA
RBA2 93
RBB2 95
TBA2 92
TBB2 94
CK64K3 97
CK8K3 96
TIMING
NET_T_3
RBA3 99
RBB3 101
TBA3 98
TBB3 100
RT1 106
RD1 107
ST1 104
SD1 105
RT2/PRICK 110
RD2/PRIDR 111
ST2/PRIFS 108
SD2/PRIDX 109
TMG
TMG
TMG
TMG
SEL
PRIDX
PRI SELECT
NETINT 103
CLK12M 65
XIN 63
XOUT 62
OSC
12.288M
LOOP BACK
S/P
BUFF
SEL
P/S
RT2/PRICK
RD2/PRIDR
ST2/PRIFS
SD2/PRIDX
12.288M
NET_T
TMG
CK
FS
SEL
PRI SELECT
LOOP BACK
117 TDMCK
116 TDMFS
118 TDMDR
119 TDMDX
115 TDMOP
114 TDMSL
NET_T 113 NETW8K
BUFF_CLR
SMPL_TMG
NETW_SEL
RATE_SET
N8K_COUNT
BUFF_CHK
LOOP_BACK
VCPIF_SET
BUFF
DEC
8 VCS
2–4 VA0–2
18–16, 14–12, 7, 6 VD0–7
9 VRD
11 VWR
BUFF_CLR
SMPL_TMG
REG
NETW_SEL
BUFF_CLR
INT_CTRL
RATE_SET
N8K_COUNT
SMPL_TMG
BUFF_CHK
LOOP_BACK
VCPIF_SET
EXTIF_SET
BUFF
DEC
34 HCS
38–35 HA0–3
50–47, 45–42 HD0–7
39 HRD
NETW_SEL
BUFF_CLR
INT_CTRL
RATE_SET
LOOP_BACK
VCPIF_SET
EXTIF_SET
REG
40 HWR
32 HINT
NET_T1, 2
NET CNT
OR
BUFF
81-76, 74, 73, 71 PA0–7, PB
REG
70, 69, 59-54, 72 PC0–7, PD
29–26, 24–21, 20 PE0–7, PF
RESET 52 RESET