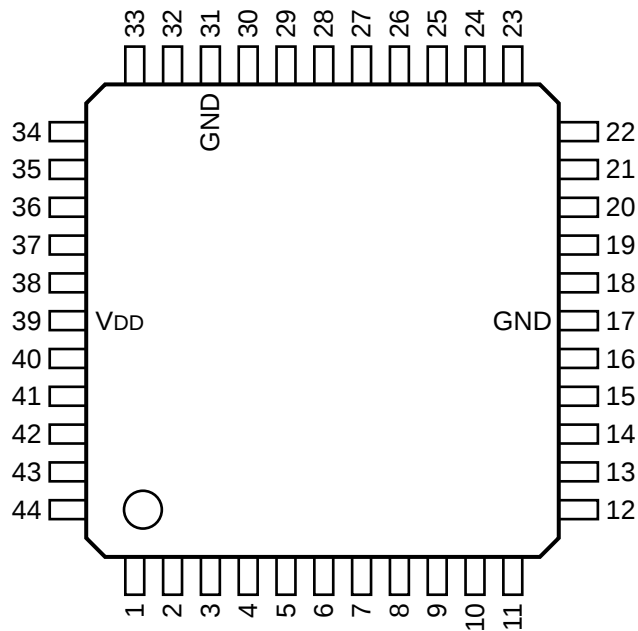


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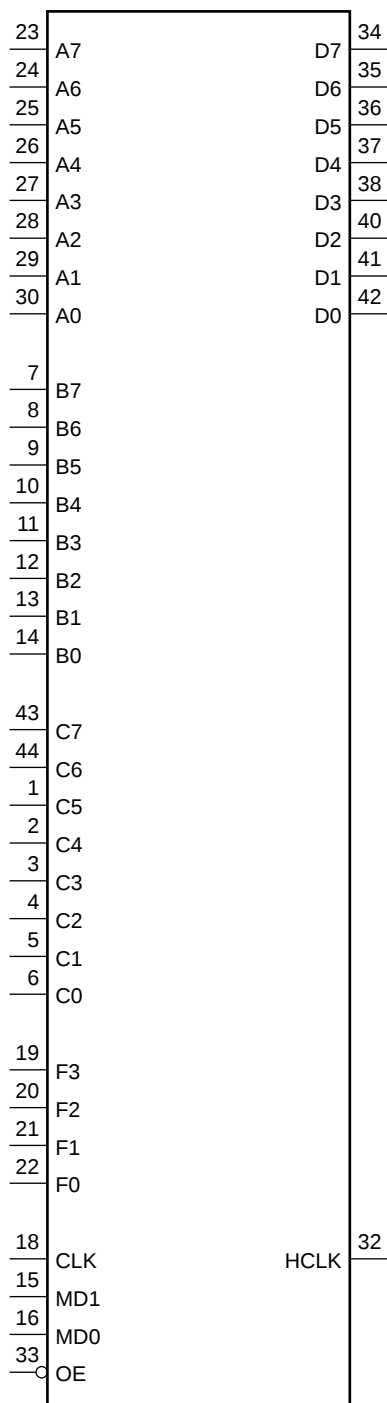
C-MOS MULTI FUNCTION GATE

—TOP VIEW—



(VDD = +5V)

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	C5	12	I	B2	23	I	A7	34	O	D7
2	I	C4	13	I	B1	24	I	A6	35	O	D6
3	I	C3	14	I	B0	25	I	A5	36	O	D5
4	I	C2	15	I	MD1	26	I	A4	37	O	D4
5	I	C1	16	I	MD0	27	I	A3	38	O	D3
6	I	C0	17	—	GND	28	I	A2	39	—	VDD
7	I	B7	18	I	CLK	29	I	A1	40	O	D2
8	I	B6	19	I	F3	30	I	A0	41	O	D1
9	I	B5	20	I	F2	31	—	GND	42	O	D0
10	I	B4	21	I	F1	32	O	HCLK	43	I	C7
11	I	B3	22	I	F0	33	I	OE	44	I	C6



MD1	MD0	MODE
L	L	VARIABLE LENGTH SHIFT REGISTER
L	H	SORTING REGISTER
H	L	TIMING GENERATOR
H	H	3 to 1 MULTIPLEXER WITH D-FF

••••• MODE-0

••••• MODE-1

••••• MODE-2

••••• MODE-3

LOW LEVEL : GND

HIGH LEVEL: +5V

MODE-0**INPUT**

A0–A7 : SHIFT REGISTER

F0–F3 : DELAY CONTROL

MODE-1**INPUT**

A0–A7 : LOWER 8 BITS

B0–B7 : UPPER 8 BITS

F0 : SYNC

F1 : GRAPH/MOTION SELECT

F2 : INVERT 2SB–LSB (D6–D0) WHEN H

F3 : INVERT MSB (D7) WHEN H

MODE-2**INPUT**

A0–A7 : INTERVAL ROM DATA

F0 : COUNTER ENABLE

F1 : LOAD

OUTPUT

HCLK : HALF CLOCK OUTPUT

MODE-3**INPUT**

A0–A7 : GROUP A

B0–B7 : GROUP B

C0–C7 : GROUP C

F0, F1 : SELECT FOR GROUP A TO C

F2 : INVERT 2SB to LSB (D6 to D0) WHEN H

F3 : INVERT MSB (D7) WHEN H

ALL MODE**INPUT**

CLK : SYSTEM CLOCK

MD0,MD1 : MODE CONTROL

OE : OUTPUT ENABLE

OUTPUT

D0–D7 : DATA