Low-voltage frequency synthesizer for radio telephones

UMA1021M

FEATURES

- Low phase noise
- Low current from 3 V supply
- Fully programmable main divider
- 3-line serial interface bus
- Independent fully programmable reference divider, driven from external crystal oscillator
- Dual charge pump outputs
- Hard and soft power-down control.

APPLICATIONS

- 900 MHz and 2 GHz mobile telephones
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The UMA1021M BICMOS device integrates a prescaler, programmable dividers, and a phase comparator to implement a phase-locked loop.

The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 5 V supplies.

The synthesizer operates at RF input frequencies up to 2.2 GHz, with a fully programmable reference divider. All divider ratios are supplied via a 3-wire serial programming bus.

Separate power and ground pins are provided to the analog (charge-pump) and digital circuits. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. V_{DD1} and V_{DD2} must also be at the same potential (V_{DD}). V_{CC} must be equal to or greater than V_{DD} (e.g. V_{DD} = 3 V and V_{CC} = 5 V for wider VCO control voltage range).

The phase detector has two charge-pump outputs, CP and CPF, the latter of which is enabled directly at pin FAST. This permits the design of adaptive loops. The charge pump currents (phase detector gain) are fixed by an external resistance at pin I_{SET} and via the serial interface. Only a passive loop filter is necessary; the charge pumps function within a wide voltage compliance range to improve the overall system performance.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	digital supply voltage	$V_{DD1} = V_{DD2}$; $V_{CC} \geq V_{DD}$	2.7	–	5.5	V
V_{CC}	charge-pump supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
$I_{DD} + I_{CC}$	supply current		–	9	–	mA
$I_{CC(pd)} + I_{DD(pd)}$	total supply current in power-down mode		–	5	–	µA
f_{RF}	RF input frequency		300	–	2200	MHz
f_{xtal}	crystal reference input frequency		3	–	35	MHz
f_{PC}	phase comparator frequency		–	200	–	kHz
T_{amb}	operating ambient temperature		–30	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1021M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

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BLOCK DIAGRAM

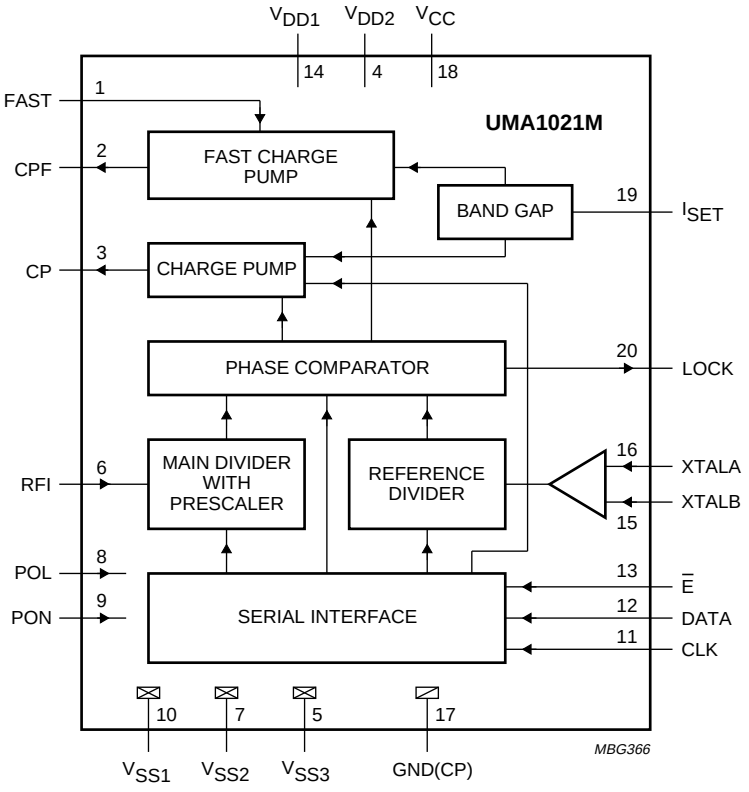


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
FAST	1	enable input for fast charge-pump output CPF
CPF	2	fast charge-pump output
CP	3	normal charge-pump output
V_{DD2}	4	power supply 2
V_{SS3}	5	ground 3
RFI	6	2 GHz main divider input
V_{SS2}	7	ground 2
POL	8	digital input to select polarity of power-on inputs (PON and sPON): POL = 0 for active low and POL = 1 for active HIGH
PON	9	power-on input
V_{SS1}	10	ground 1
CLK	11	programming bus clock input
DATA	12	programming bus data input
$\overline{E}$	13	programming bus enable input
V_{DD1}	14	power supply 1
XTALB	15	complementary crystal frequency input from TCXO; if not used should be decoupled to ground
XTALA	16	crystal frequency input from TCXO; if not used should be decoupled to ground
GND(CP)	17	ground for charge-pump
V_{CC}	18	supply for charge-pump
I_{SET}	19	external resistor from this pin to ground sets the charge-pump currents
LOCK	20	out-of-lock detector output

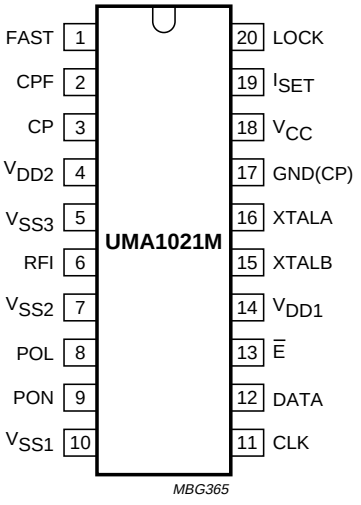


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Main divider

The main divider is clocked at pin RFI by the RF signal which is AC-coupled from an external VCO. The divider operates with signal levels from 50 to 225 mV (RMS), and at frequencies from 300 MHz to 2.2 GHz. It consists of a fully programmable bipolar prescaler followed by a CMOS counter. Any divide ratios from 512 to 131071 inclusive can be programmed.

Reference divider

The reference divider is clocked by the differential signal between pins XTALA and XTALB. If only one of these inputs is used, the other should be decoupled to ground. The applied input signal(s) should be AC-coupled. The circuit operates with levels from 50 up to 500 mV (RMS) and at frequencies from 3 to 35 MHz. Any divide ratios from 8 to 2047 inclusive can be programmed.

Phase detector

The phase detector is driven by the output edges of the main and reference dividers. It produces current pulses at pins CP and CPF whose amplitudes are programmed. The pulse duration is equal to the difference in time of arrival of the edges from the two dividers. If the main divider edge arrives first, CP and CPF sink current. If the reference divider edge arrives first, CP and CPF source current.

The currents at CP and CPF are programmed via the serial bus as multiples of a reference current set by an external resistor connected between pin I_{SET} and V_{SS} (see Table 3). CP remains active except in power-down. CPF is enabled via input pin FAST which is synchronized with respect to the phase detector to prevent output current pulses being interrupted. By appropriate connection to the loop filter, dual bandwidth loops can be designed; short time constant during frequency switching (FAST mode) to speed-up channel changes, and low bandwidth in the settled state to improve noise and breakthrough levels.

Additional circuitry is included to ensure that the gain of the phase detector remains linear even for small phase errors.

Out-of-lock detector

The out-of-lock detector is enabled (disabled) via the serial interface by setting bit OOL HIGH (LOW). Pin LOCK is a digital output with CMOS levels corresponding to the supply voltage. When the out-of-lock detector is enabled, LOCK is HIGH if the error at the phase detector input is less than approximately 25 ns, otherwise LOCK is LOW. If the out-of-lock detector is disabled, LOCK remains HIGH.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, clock (CLK) and enable ($\overline{E}$). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges and their appropriate data bits are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed latch when $\overline{E}$ returns HIGH. During normal operation, $\overline{E}$ should be kept HIGH. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programmed data even during power-down.

When the synthesizer is powered-on, the presence of a signal at the reference divider input is required for correct programming.

Data format

The leading bits (dt16 to dt0) make up the data field, while the trailing four bits (ad3 to ad0) are the address field. The UMA1021M uses 4 of the 16 available addresses. These are chosen for compatibility with other Philips Semiconductors radio telephone ICs. The data format is shown in Table 1. The first bit entered is dt16, the last bit is ad0. For the divider ratios, the first bits entered (PM16 and PR10) are the most significant (MSB).

The trailing address bits are decoded on the rising edge of $\overline{E}$. This produces an internal load pulse to store the data in the addressed latch. To avoid erroneous divider ratios, the load pulse is not allowed during data reads by the frequency dividers. This condition is guaranteed by respecting a minimum $\overline{E}$ pulse width after data transfer.

The test register (address 0000) does not normally need to be programmed. However if it is programmed, all bits in the data field should be set to logic 0.

Power-down mode

The synthesizer is on when both the input signals PON and the programmed bit sPON are active. The ‘active’ level for these two signals is chosen at pin POL (see Table 2). When turned on, the dividers and phase detector are synchronized to avoid random phase errors. When turned off, the phase detector is synchronized to avoid interrupting charge-pump pulses. The UMA1021M has a very low current consumption in the power-down mode.

Table 1 Bit allocation

First in	REGISTER BIT ALLOCATION																			Last in
DATA FIELD																	ADDRESS			
dt16	dt15	dt14	dt13	dt12	dt11	dt10	dt9	dt8	dt7	dt6	dt5	dt4	dt3	dt2	dt1	dt0	ad3	ad2	ad1	ad0
TEST BITS; note 1																	0	0	0	0
X	X	X	X	OOL[2]	X	CR1	CR0	X	X	sPON[2]	X	X	X	X	X	X	0	0	0	1
PM16[3]	MAIN DIVIDER COEFFICIENT															PM0	0	1	0	0
X	X	X	X	X	X	PR10[3]	REFERENCE DIVIDER COEFFICIENT									PR0	0	1	0	1

Notes

1. The test register (address 0000) should not be programmed with any other values except all zeros for normal operation.
2. Bit sPON = software power-up for synthesizer (see Table 2); OOL = Out-Of-Lock (1 = enabled).
3. PM16 is the MSB of the main divider coefficient; PR10 is the MSB of the reference divider coefficient.

Table 2 Power-on programming

POL	PON	sPON	SYNTHESIZER STATE	COMPATIBILITY
0	0	0	on	UMA1019M/UMA1019AM
0	1	X	off	UMA1019M/UMA1019AM
0	X	1	off	UMA1019M/UMA1019AM
1	0	X	off	UMA1017M
1	X	0	off	UMA1017M
1	1	1	on	UMA1017M

Table 3 Fast and normal charge pumps current ratio (note 1)

CR1	CR0	I_{CP}	I_{CPF}	$I_{CPF} : I_{CP}$
0	0	$2 \times I_{SET}$	$8 \times I_{SET}$	4 : 1
0	1	$2 \times I_{SET}$	$16 \times I_{SET}$	8 : 1
1	0	$1 \times I_{SET}$	$12 \times I_{SET}$	12 : 1
1	1	$1 \times I_{SET}$	$16 \times I_{SET}$	16 : 1

Note

1. $I_{SET} = \frac{V_{SET}}{R_{SET}}$; reference current for charge pumps.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	digital supply voltage	–0.3	+5.5	V
V_{CC}	charge-pump supply voltage	–0.3	+5.5	V
$V_{CC} - V_{DD}$	difference in voltage between V_{CC} and V_{DD}	–0.3	+5.5	V
V_n	voltage at pins 1, 6, 8, 9, 11 to 13 and 20	–0.3	V_{DD} + 0.3	V
	voltage at pins 2, 3, 15, 16, 19	–0.3	V_{CC} + 0.3	V
ΔV_{GND}	difference in voltage between any of GND(CP), V_{SS1}, V_{SS2}, and V_{SS3} (these pins should be connected together)	–0.3	+0.3	V
P_{tot}	total power dissipation	–	150	mW
T_{stg}	storage temperature	–55	+125	°C
T_{amb}	operating ambient temperature	–30	+85	°C
$T_{j(max)}$	maximum junction temperature	–	150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

CHARACTERISTICS

All values refer to the typical measurement circuit of Fig.5; $V_{DD1} = V_{DD2} = 2.7$ to 5.5 V; $V_{CC} = 2.7$ to 5.5 V; $T_{amb} = 25\ ^{\circ}C$; unless otherwise specified. Characteristics for which only a typical value is given are not tested.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply; pins 4, 14 and 18						
V_{DD}	digital supply voltage	$V_{DD1} = V_{DD2}$; $V_{CC} \geq V_{DD}$	2.7	–	5.5	V
V_{CC}	charge pump supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
$I_{DD1} + I_{DD2}$	synthesizer digital supply current	$V_{DD} = 5.5$ V	–	6.5	9.0	mA
I_{CC}	charge pump supply current	$V_{CC} = 5.5$ V; $R_{SET} = 5.6$ kΩ	–	2.5	3.5	mA
$I_{CC(pd)} + I_{DD(pd)}$	total supply current in power-down mode	logic levels 0 V or V_{DD}	–	5	50	µA
RF main divider input; pin 6						
f_{RF}	RF input frequency		300	–	2200	MHz
$V_{RF(rms)}$	AC-coupled input signal level (RMS value)	$R_s = 50\ \Omega$	50	–	225	mV
R_m	main divider ratio		512	–	131071	
Z_i	input impedance (real part)	$f_{RF} = 2$ GHz	–	tbf	–	kΩ
C_i	typical pin input capacitance		–	tbf	–	pF
Synthesizer reference divider input; pins 15 and 16						
f_{xtal}	crystal reference input frequency		3	–	35	MHz
$V_{xtal(rms)}$	sinusoidal input signal level between pins 15 and 16 (RMS value)		50	–	500	mV
R_{ref}	reference division ratio		8		2047	
Z_i	input impedance (real part)	$f_{xtal} = 30$ MHz	–	tbf	–	kΩ
C_i	typical pin input capacitance		–	tbf	–	pF
Phase detector						
f_{PCmax}	maximum loop comparison frequency		–	2000	–	kHz
Charge pump current setting resistor input; pin 19						
R_{SET}	external resistor connected between pin 19 and ground		5.6	–	12	kΩ
V_{SET}	regulated voltage at pin 19	$R_{SET} = 5.6$ kΩ	–	1.15	–	V
Charge pump outputs; pins 2 and 3; $R_{SET} = 5.6$ kΩ						
$I_{ocp(err)}$	charge pump output current error	note 1	–25	–	+25	%
I_{match}	sink-to-source current matching		–	±5	–	%
I_{LIcp}	charge pump off leakage current	$V_{CP/CPF} = \frac{1}{2}V_{CC}$	–5	±1	+5	nA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Phase noise						
N_{900}	synthesizer's contribution to close-in phase noise of 900 MHz RF signal at 1 kHz offset	f_{xtal} = 13 MHz; V_{xtal} = 0 dBm; f_{PC} = 200 kHz	–	–83	–	dBc/Hz
N_{1800}	synthesizer's contribution to close-in phase noise of 1.8 GHz RF signal at 1 kHz offset	f_{xtal} = 13 MHz; V_{xtal} = 0 dBm; f_{PC} = 200 kHz	–	–77	–	dBc/Hz
Interface logic input signal levels; pins 1, 8, 9, 11, 12 and 13						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.3	V
V_{IL}	LOW level input voltage		–0.3	–	$0.3V_{DD}$	V
I_{bias}	input bias current	logic 1 or logic 0	–5	–	+5	µA
C_i	input capacitance		–	2	–	pF
Lock detect output signal; pin 20						
V_{OH}	High level output voltage		$0.7V_{DD}$	–	–	V
V_{OL}	Low level output voltage		–	–	$0.3V_{DD}$	V
t_{OOL}	phase error threshold for out-of-lock detector		–	25	–	ns

Note

1. Condition: $0.4 < V_{CP/CPF} < (V_{CC} - 0.4)$.

SERIAL BUS TIMING CHARACTERISTICS

$V_{DD} = V_{CC} = 3$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r	input rise time	–	10	40	ns
t_f	input fall time	–	10	40	ns
T_{cy}	clock period	100	–	–	ns
Enable programming; $\overline{E}$					
t_{START}	delay to rising clock edge	40	–	–	ns
t_{END}	delay from last falling clock edge	–20	–	–	ns
t_W	minimum inactive pulse width	4000[1]	–	–	ns
$t_{SU;\overline{E}}$	enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time	20	–	–	ns

Note

1. The minimum pulse width (t_W) can be smaller than 4 µs provided all the following conditions are satisfied:

   a) Main divider input frequency $f_{RF} > \frac{447}{t_W}$

   b) Reference divider input frequency $f_{XTAL} > \frac{3}{t_W}$

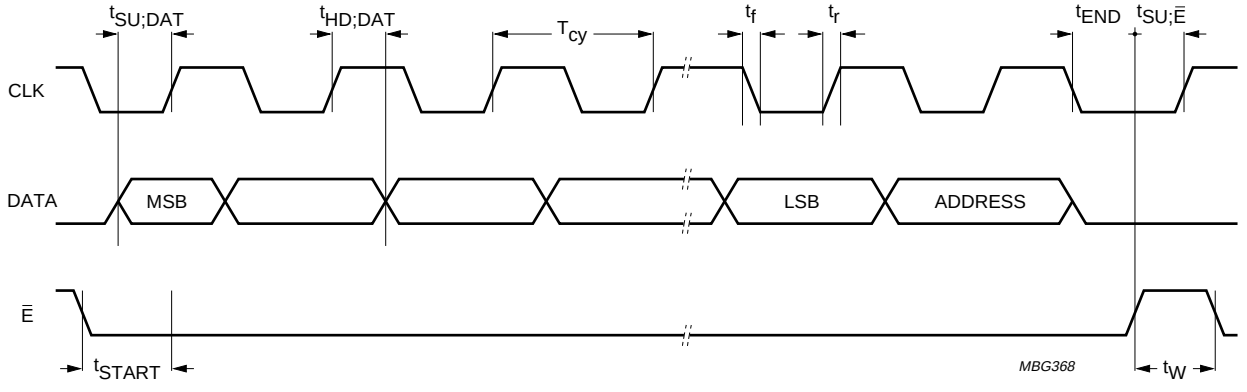


Fig.3 Serial bus timing diagram.

APPLICATION INFORMATION

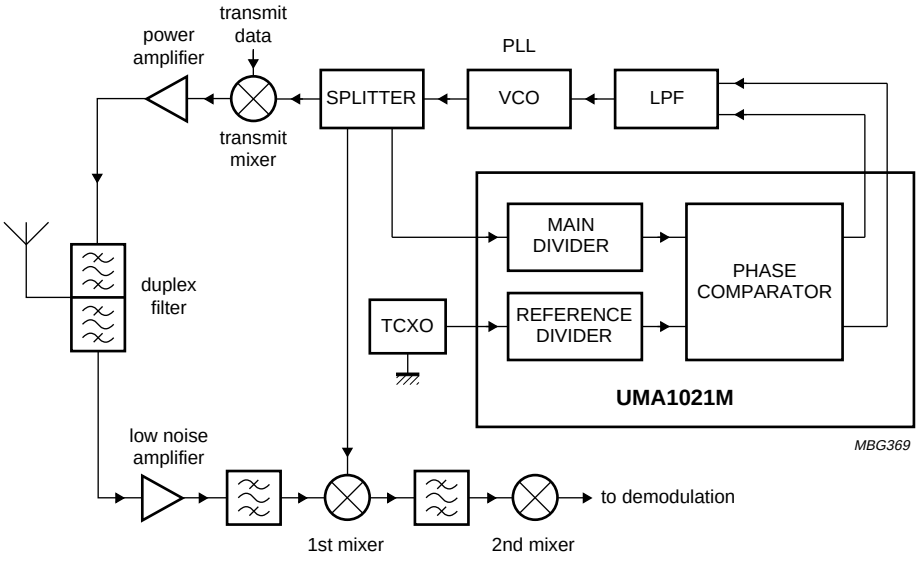
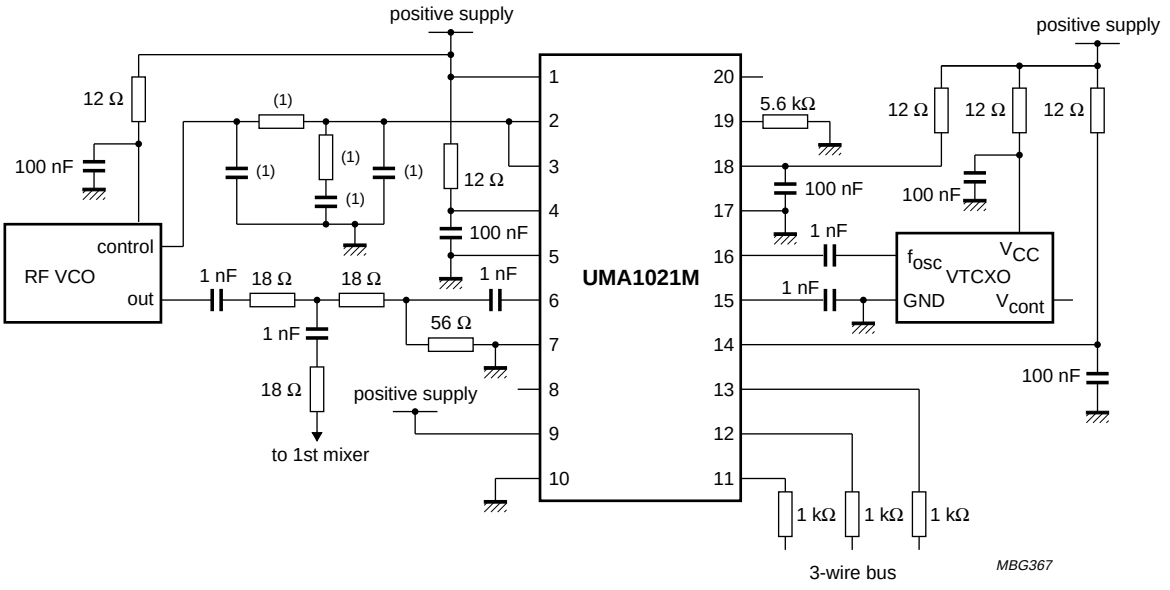


Fig.4 Typical application block diagram.



(1) Values depend on application.

Fig.5 Typical test and application diagram.