Dual low-power frequency synthesizer UMA1005T

FEATURES

- Fast locking by ‘Fractional-N’ divider
- Auxiliary synthesizer
- Digital phase comparator with proportional and integral charge pump output
- High-speed serial input
- Low-power consumption
- Programmable charge pump currents
- Supply voltage range 2.9 to 5.5 V.

APPLICATIONS

- Mobile telephony
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The UMA1005T is a low-power, high-performance dual frequency synthesizer fabricated in CMOS technology. Fractional-N division with selectable modulo 5 or 8 is implemented in the main synthesizer.

The detectors and charge pumps are designated to achieve 10 to 5000 kHz channel spacing using fractional-N decreases the channel spacing by a factor 5 or 8. Together with an external standard 2, 3 or 4 ratio prescaler the main synthesizer can operate in the GHz frequency range.

Channel selection and programming is realized by a high-speed 3-wire serial interface.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1005T	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

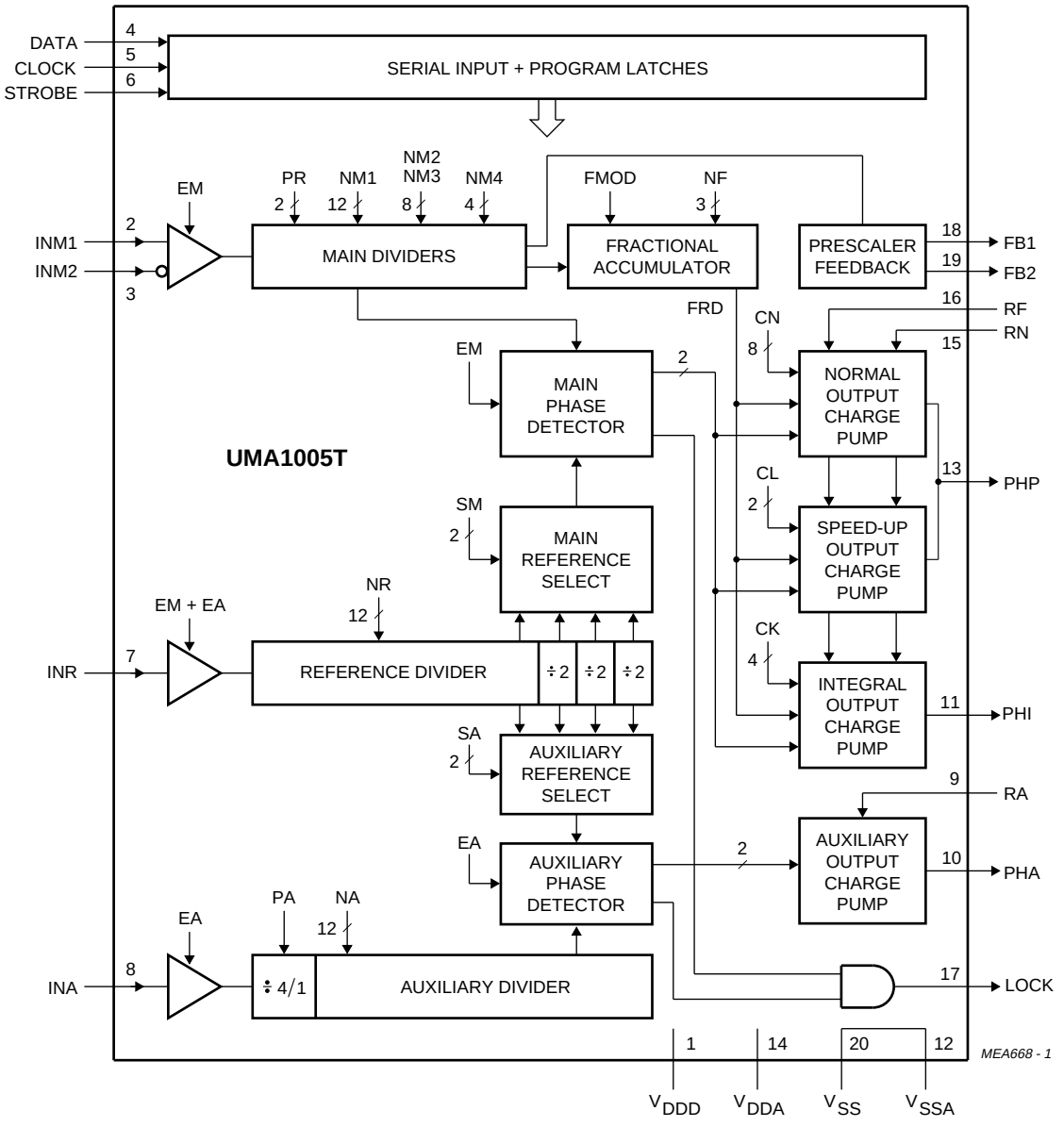

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{DDD}	1	digital supply voltage
INM1	2	main divider positive input; rising edge active
INM2	3	main divider negative input; falling edge active
DATA	4	serial data input line
CLOCK	5	serial clock input line
STROBE	6	serial strobe input line
INR	7	reference divider input line; rising edge active
INA	8	auxiliary divider input line; rising edge active
RA	9	auxiliary current setting; resistor to V_{SS}
PHA	10	auxiliary phase detector output
PHI	11	integral phase detector output
V_{SSA}	12	analog ground; internally connected to V_{SS}
PHP	13	proportional phase detector output
V_{DDA}	14	analog supply voltage
RN	15	main current setting input; resistor to V_{SS}
RF	16	fractional compensation current setting input; resistor to V_{SS}
LOCK	17	lock detector output
FB1	18	feedback output 1 for prescaler modulus control
FB2	19	feedback output 2 for prescaler modulus control
V_{SS}	20	common ground connection

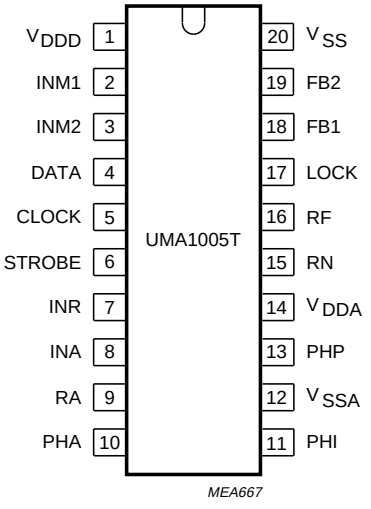

Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Serial programming input

The serial input is a 3-wire input (CLOCK, STROBE and DATA) to program all counter ratios, DACs, selection and enable bits. The programming data is structured into 24 or 32-bit words. Each word includes 1 or 4 address bits. Figure 3 shows the timing diagram of the serial input. When the STROBE = LOW, the clock driver is enabled and on the positive edges of the CLOCK the signal on the DATA input is clocked into a shift register. When the STROBE = HIGH, the clock is disabled and the data in the shift register remains stable. Depending on the 1 or 4 address bits the data is latched into different working registers or temporary registers. In order to fully program the synthesizer, 4 words must be sent:

1. D word.
2. C word.
3. B word.
4. A word.

Figure 4 shows the format and the contents of each word. The E word is for testing purposes only. The E (test) word is reset when programming the D word. The data for NM4, CN and PR is stored by the B word temporary registers. When the A word is loaded, the data of these temporary registers is loaded together with the A word into the work registers which avoids false temporary main divider input. CN is only loaded from the temporary registers when a short 24-bit A0 word is used. CN will be directly loaded by programming a long 32-bit A1 word. The flag LONG in the D word determines whether A0 (LONG = 0) or A1 (LONG = 1) format is applicable.

The A word contains new data for the main divider. The A word is loaded only when a main divider synchronization signal is also active, to avoid phase jumps when reprogramming the main divider. The synchronization signal is generated by the main divider. It disables the loading of the A word each main divider cycle during maximum 300 main divider input cycles. To make sure that the A word will be correctly loaded the STROBE signal must be HIGH for at least 300 main divider input cycles. Programming the A word also means that the main charge pumps on outputs PHP and PHI are set into the speed-up mode as long as the STROBE remains HIGH.

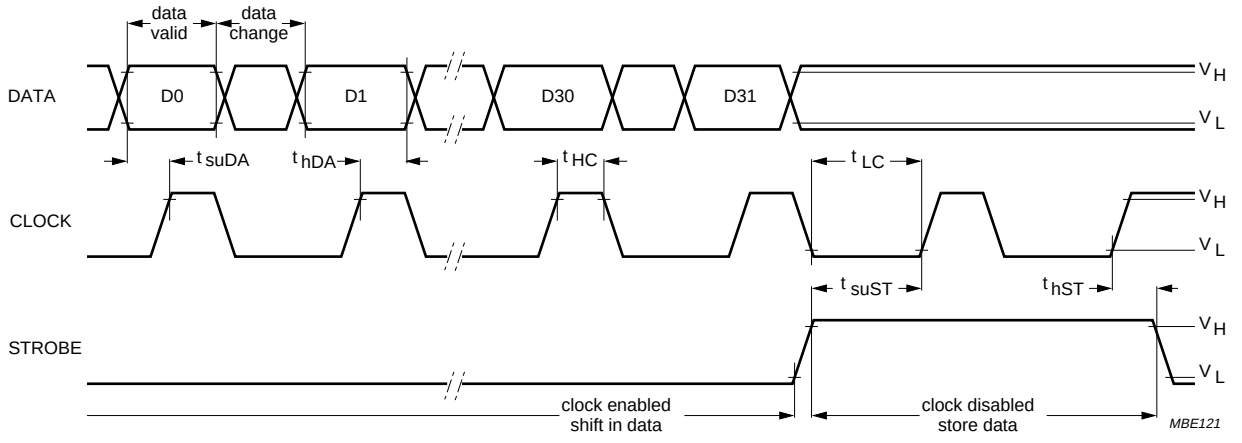

Fig.3 Serial input timing sequence.

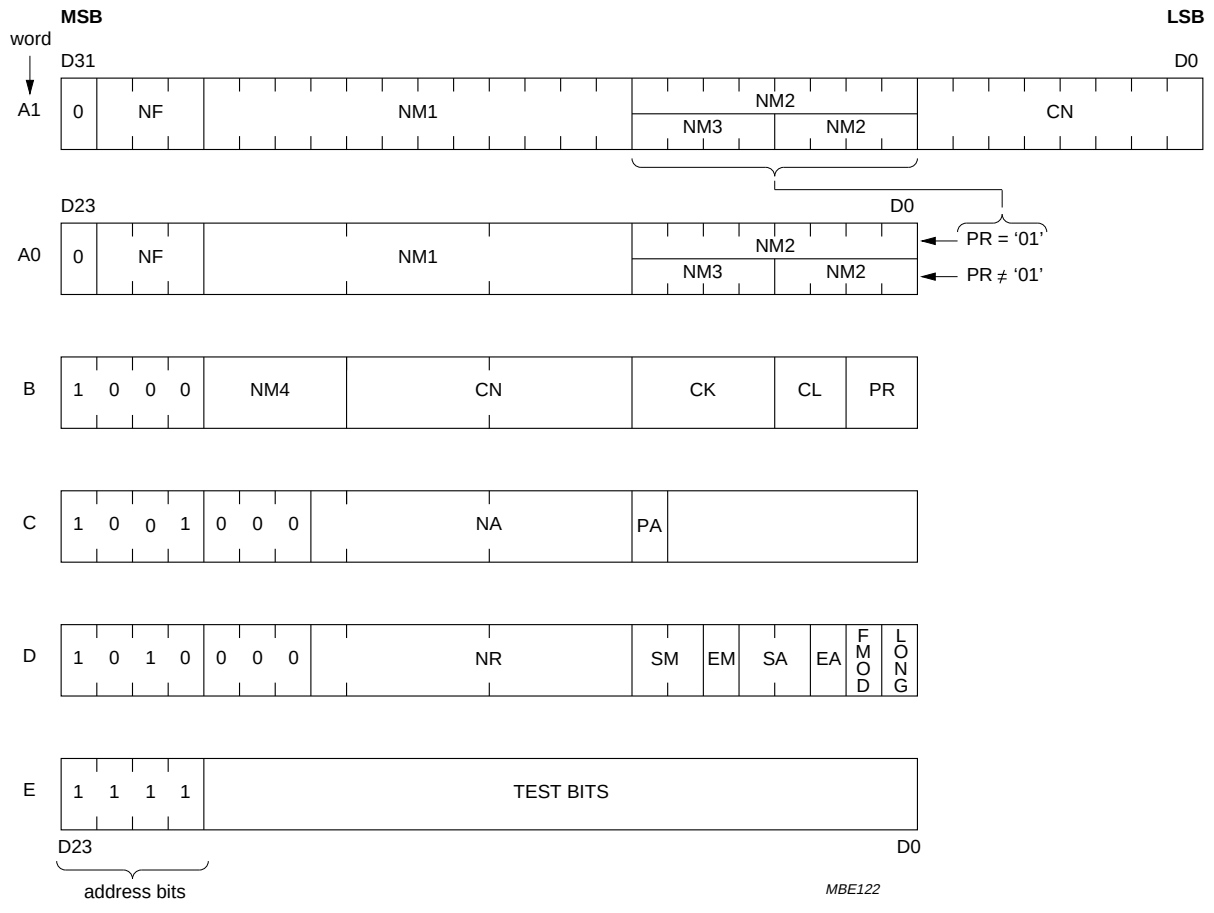

Fig.4 Serial input word format.

Table 1 Description of symbols used in Fig.4

SYMBOL	BITS(1)	FUNCTION
NM1	12	number of main divider cycles when prescaler is programmed in ratio R1 (FB1 = 1; FB2 = 0); note 2
NM2	8 if PR = 01	number of main divider cycles when prescaler is programmed in ratio R2 (FB1 = 0; FB2 = 0); note 2
	4 if PR ≠ 01	
NM3	4 if PR = 1X	number of main divider cycles when prescaler is programmed in ratio R3 (FB1 = 0; FB2 = 1); note 2
NM4	4 if PR = 11 or 00	number of main divider cycles when prescaler is programmed in ratio R4 (FB1 = 1; FB2 = 1); note 2
PR	2	prescaler type in use: PR = 01; modulus 2 prescaler PR = 10; modulus 3 prescaler PR = 11; modulus 4 prescaler PR = 00; modulus 4 prescaler (inhibit ratio 3)
NF	3	fractional-N increment
FMOD	1	fraction-N modulus selection flag: 1 = modulo 8 0 = modulo 5
LONG	1	A word format selection flag: 0 = 24-bit A0 format 1 = 32-bit A1 format
CN	8	binary current setting factor for main charge pumps
CL	2	binary acceleration factor for proportional charge pump current
CK	4	binary acceleration factor for integral charge pump current
EM	1	main divider enable flag
EA	1	auxiliary divider enable flag
SM	2	reference select for main phase detector
SA	2	reference select for auxiliary phase detector
NR	9	reference divider ratio
NA	9	auxiliary divider ratio
PA	1	auxiliary prescaler mode: PA = 0; divide-by-4 PA = 1; divide-by-1

Notes

1. X = don’t care.
2. Not including reset cycles and fractional-N effects.

Auxiliary variable divider

The input signal on INA is amplified to a logic level by a single ended input buffer, which accepts LOW level AC coupled input signals. This input stage is enabled if the serial control bit EA = 1. Disabling means that all currents in the input stage are switched off. A fixed divide by 4 is enabled if PA = 0. This divider has been optimized to accept a high-frequency (90 MHz at a supply voltage range of 4.75 to 5.5 V) input signal. If PA = 1 this divider is disabled and the input signal is fed directly to the second

stage, which is a 9-bit programmable divider with standard input frequency (30 MHz). The division ratio can be expressed as:

If PA = 0; N = 4 × NA.

If PA = 1; N = NA; with NA = 4 to 511.

Reference variable divider (Fig.5)

The input signal on INR is amplified to a logic level by a single ended input buffer, which accepts LOW level AC coupled input signals. This input stage is enabled by the OR function of the serial input bits EA and EM. Disabling means that all currents in the input stage are switched off. The reference divider consists of a programmable divider by NR (NR = 4 to 511) followed by a 3-bit binary counter. The 2-bit SM determines which of the 4 output pulses is selected as main phase detector input. The 2-bit SA determines the selection of the auxiliary phase detector signal. To obtain the best time spacing for the main and auxiliary reference signals, the opposite output will be used for the auxiliary phase detector, reducing the possibility of unwanted interactions. For this reason the programmable divider produces a symmetric output pulse for even ratios and a 1 input cycle asymmetric pulse for odd ratios.

Main variable divider

The input signals on INM1 and INM2 are amplified to a logic level by a balanced input comparator giving a common mode rejection. This input stage is enabled when serial control bit EM = 1. Disabling means that all currents in the comparator are switched off. The main divider is built-up by a 12-bit counter plus a sign bit. Depending on the serial input values of NM1, NM2, NM3, NM4 and the prescaler select PR, the counter will select a prescaler ratio during a number of input cycles in accordance with the information in Table 2.

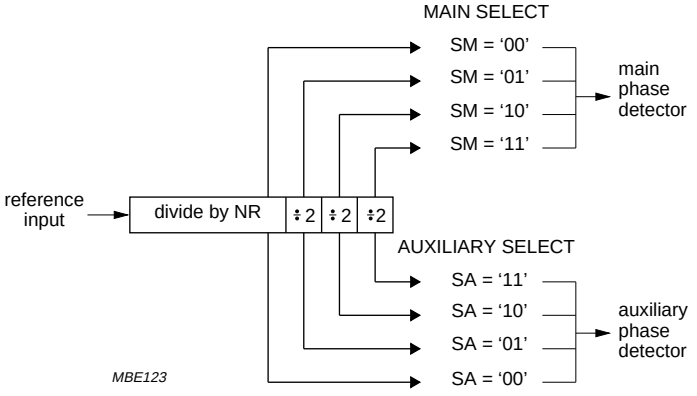

Fig.5 Reference variable divider.

Table 2 Selection of prescaler ratio

COUNTER STATUS	FB1	FB2	PRESCALER RATIO(1)
(–NM1 – 1) to 0	1	0	R1
(–NM1 – 1) to –1	1	0	R1(2)
1 to NM2	0	0	R2
0 to NM2	0	0	R2(2)
0 to NM3	0	1	R3; if PR = 1X
0 to NM4	1	1	R4; if PR = 11 or 00

Notes

1. X = don’t care.
2. When the fractional accumulator overflows.

The total division ratio from prescaler to the phase detector expressions are given in Table 3.

Table 3 Total division from prescaler to phase detector expressions

CONDITION	EXPRESSION
PR = 01	$N = (NM1 + 2) \times R1 + NM2 \times R2$
	$N' = (NM1 + 1) \times R1 + (NM2 + 1) \times R2$; note 1
PR = 10	$N = (NM1 + 2) \times R1 + NM2 \times R2 + (NM3 + 1) \times R3$
	$N' = (NM1 + 1) \times R1 + (NM2 + 1) \times R2 + (NM3 + 1) \times R3$; note 1
PR = 11	$N = (NM1 + 2) \times R1 + NM2 \times R2 + (NM3 + 1) \times R3 + (NM4 + 1) \times R4$
	$N' = (NM1 + 1) \times R1 + (NM2 + 1) \times R2 + (NM3 + 1) \times R3 + (NM4 + 1) \times R4$; note 1
PR = 00	$N = (NM1 + 2) \times R1 + NM2 \times R2 + (NM4 + 1) \times R4$
	$N' = (NM1 + 1) \times R1 + (NM2 + 1) \times R2 + (NM4 + 1) \times R4$; note 1

Note

1. When the fractional accumulator overflows.

When the prescaler ratio is R2 = R1 + 1 the total division ratio N′ = N + 1.

Table 4 Modulus prescaler

PR	MODULUS PRESCALER	BIT CAPACITY			
		NM1	NM2	NM3	NM4
00	4	12	4	–	4
01	2	12	8	–	–
10	3	12	4	4	–
11	4	12	4	4	4

The loading of the work registers NM1, NM2, NM3, NM4 and PR is synchronized with the state of the main counter, to avoid extra phase disturbance when switching over to another main divider ratio as is explained in Section “Serial programming input”.

At the completion of a main divider cycle, a main divider output pulse is generated which will drive the main phase comparator. Also the fractional accumulator is incremented with NF. The accumulator works modulo Q. Q is preset by the serial control bit FMOD to 8 when FMOD = 1. Each time the accumulator overflows, the feedback to the prescaler will select one cycle using prescaler ratio R2 instead of R1.

As shown above, this will increase the overall division ratio by 1 if R2 = R1 + 1. The mean division ratio over Q main divider cycles will then be: $NQ = N + \frac{NF}{Q}$

Programming a fraction means the prescaler with main divider will divide by N or N + 1.

The output of the main divider will be modulated with a fractional phase ripple. This phase ripple is proportional to the contents of the fractional accumulator FRD, which is used for fractional current compensation.

Phase detectors (Fig.6)

The auxiliary and main phase detectors are a 2 D-type flip-flop phase and frequency detector. The flip-flops are set by the negative edges of output signals of the dividers. The reset inputs are activated when both flip-flops have been set and when the reset enable signal is active (LOW). Around zero phase error this has the effect of delaying the reset for 1 reference input cycle. This avoids non-linearity or dead band around zero phase error. The flip-flops drive on-chip charge pumps. A pull-up current from the charge pump indicates that the VCO frequency shall be increased while a pull-down pulse indicates that the VCO frequency shall be decreased.

Current settings

The UMA1005T has 3 current setting pins RA, RN and RF. The active charge pump currents and the fractional compensation currents are linearly dependent on the current in the current setting pins. This current I_R can be set by an external resistor to be connected between the current setting pin (pin 9) and V_{SS}. The typical value for R (current setting resistor) can be calculated with the equation:

$$R = \frac{(V_{DDA} - 0.5) - 237\sqrt{I_R}}{I_R}$$

The current can be set to zero by connecting the corresponding pin to V_{DDA}.

Auxiliary output charge pumps

The auxiliary charge pumps on pin PHA are driven by the auxiliary phase detector and the current value is determined by the external resistor (R_{ext}) at pin RA. The active charge pump current is typically: $|I_{PHA}| = 8 \times I_{RA}$.

Main output charge pumps and fractional compensation currents

The main charge pumps on pins PHP and PHI are driven by the main phase detector and the current value is determined by the current at pin RN and via a number of DACs which are driven by registers of the serial input. The fractional compensation current is determined by the current at pin RF, the contents of the fractional accumulator FRD and a number of DACs driven by registers from the serial input. The timing for the fractional compensation is derived from the reference divider. The current is on during 1 input reference cycle before and 1 cycle after the output signal to the phase comparator. Figure 7 shows the waveforms for a typical case.

When the serial input A word is loaded, the output circuits are in the ‘speed-up mode’ as long as the STROBE is HIGH, else the ‘normal mode’ is active.

NORMAL MODE

In the ‘normal mode’ the current output at PHP is: $I_{PHP(N)} = I_{pump10} + I_{comp10}$.

Where:

$|I_{pump10}| = \frac{CN \times I_{RN}}{29}$; charge pump current.

$I_{comp10} = \frac{FRD \times I_{RF}}{128}$; fractional compensation current.

In ‘normal mode’ the current at output PHI is zero.

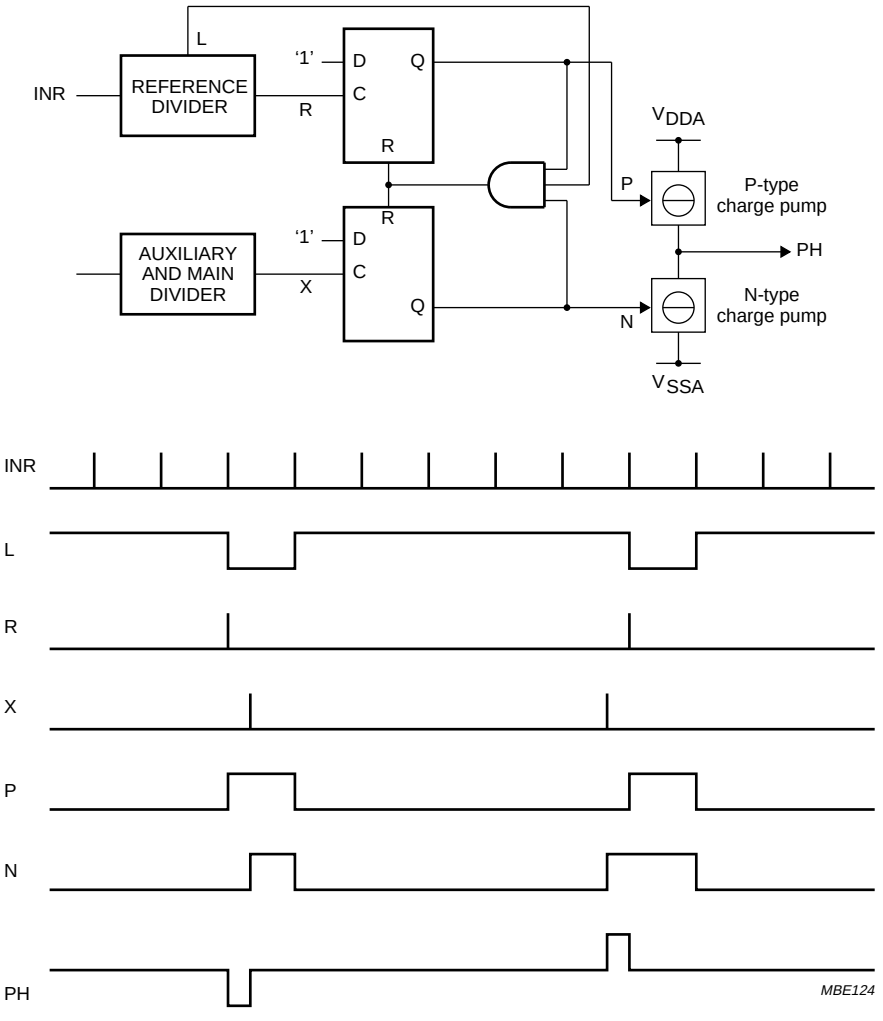

Fig.6 Phase detector structure with timing.

SPEED-UP MODE

In 'speed-up mode' the current in output PHP is:
$I_{PHP(S)} = I_{PHP(N)} + I_{pump11} + I_{comp11}$.

Where:

$I_{pump11} = I_{pump10} \times 2^{(CL + 1)}$; charge pump current.

$I_{comp11} = I_{comp10} \times 2^{(CL + 1)}$; fractional compensation current.

In 'speed-up mode' the current in output PHI is:
$I_{PHI(S)} = I_{pump21} + I_{comp21}$.

Where:

$I_{pump21} = I_{pump11} \times CK$; charge pump current.

$I_{comp21} = I_{comp11} \times CK$; fractional compensation current.

Figure 7 shows that for a proper fractional compensation the area of the fractional compensation current pulse must be equal to the area of the charge pump ripple output. This means that the current setting on the inputs RN and RF must have following ratio: $\frac{I_{RN}}{I_{RF}} = \frac{29 \times Q \times f_{VCO}}{64 \times CN \times f_{i(max)2}}$.

Where:

Q = fractional-N modulus.

$f_{VCO} = f_{i(max)1} \times N$; input frequency of the prescaler.

$f_{i(max)1}$ = maximum input frequency of the main divider (pins INM1 and INM2).

$f_{i(max)2}$ = maximum input frequency of the reference divider (pin INR).

Lock detect

The output LOCK is HIGH when the auxiliary phase detector and the main phase detector indicate a lock condition. The lock condition is defined as a phase difference of less than ±1 cycle on the reference input INR. The lock condition is also fulfilled when the relative counter is disabled (EM = 0 or EA = 0 respectively) for the main or auxiliary counter respectively.

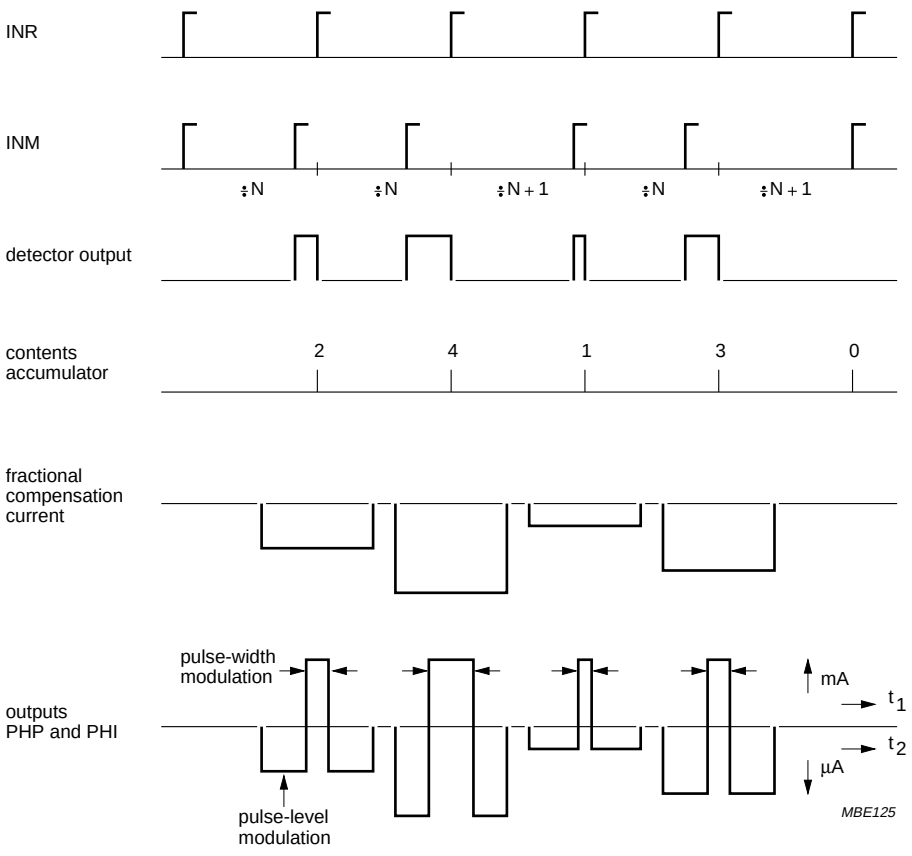

Fig.7 Waveforms for NF = 2 and fraction = 0.4.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage	–0.5	6.5	V
V_{DDA}	analog supply voltage	–0.5	6.5	V
V_I	voltage on any input	–0.5	V_{DD} + 0.5	V
I_n	DC current into any input or output	–10	+10	mA
P_{tot}	total power dissipation	–	25	mW
T_{stg}	storage temperature	–65	+150	°C
T_{amb}	operating ambient temperature	–40	+70	°C

DC CHARACTERISTICS

$V_{DDD} = V_{DDA}$ = 2.9 to 5.5 V; T_{amb} = –40 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
$I_{DDD(stb)}$	digital standby supply current	EM = EA = 0; inputs on V_{DD} or 0	–	–	5	µA
I_{DDD}	operating digital supply current	note 1	–	–	5	mA
$I_{DDA(stb)}$	analog standby supply current	$V_{RA} = V_{DDA}$; $V_{RF} = V_{DDA}$; $V_{RN} = V_{DDA}$	–	–	10	µA
I_{DDA}	operating analog supply current	note 1	–	–	0.6	mA
Digital inputs CLK, DATA and STROBE						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
Digital outputs FB1, FB2 and LOCK						
V_{OL}	LOW level output voltage	I_O = 2 mA; note 2	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = –2 mA; note 2	V_{DD} – 0.4	–	–	V
Charge pump PHA						
$\lvert I_{PHA} \rvert$	output current	I_{RA} = –62.5 µA; $V_{PHA} = \frac{1}{2}V_{DD}$; note 2	400	500	600	µA
		I_{RA} = –25 µA; $V_{PHA} = \frac{1}{2}V_{DD}$	160	200	240	µA
$\frac{\Delta I_{PHA}}{\lvert I_{PHA} \rvert}$	relative output current variation	I_{RA} = –62.5 µA; notes 2 and 3	–	2	6	%
$\Delta I_{PHA\,M}$	output current matching	I_{RA} = –62.5 µA; $V_{PHA} = \frac{1}{2}V_{DD}$; notes 2 and 4	–	–	±50	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Charge pump PHP; normal mode (notes 5, 6 and 7)**; $V_{RF} = V_{DD}$**						
$\lvert I_{PHP(N)} \rvert$	output current	I_{RN} = –62.5 μA; $V_{PHP} = \frac{1}{2}V_{DD}$; note 2	440	550	660	μA
		I_{RN} = –25 μA; $V_{PHP} = \frac{1}{2}V_{DD}$	175	220	265	μA
$\Delta I_{PHP(N)}$	relative output current variation	I_{RN} = –62.5 μA; note 3	–	2	6	%
$\Delta I_{PHP(N\ M)}$	output current matching	I_{RN} = –62.5 μA; $V_{PHP} = \frac{1}{2}V_{DD}$; notes 2 and 4	–	–	±50	μA
Charge pump PHP; speed-up mode (notes 5, 6 and 8)**; $V_{RF} = V_{DD}$**						
$\lvert I_{PHP(S)} \rvert$	output current	I_{RN} = –62.5 μA; $V_{PHP} = \frac{1}{2}V_{DD}$; note 2	2.20	2.75	3.30	mA
		I_{RN} = –25 μA; $V_{PHP} = \frac{1}{2}V_{DD}$	0.85	1.1	1.35	mA
$\Delta I_{PHP(S)}$	relative output current variation	I_{RN} = –62.5 μA; notes 2 and 3	–	2	6	%
$\Delta I_{PHP(S\ M)}$	output current matching	I_{RN} = –62.5 μA; $V_{PHP} = \frac{1}{2}V_{DD}$; notes 2 and 4	–	–	±250	μA
Charge pump PHI; speed-up mode (notes 5, 6 and 9)**; $V_{RF} = V_{DD}$**						
$\lvert I_{PHI(S)} \rvert$	output current	I_{RN} = –62.5 μA; $V_{PHI} = \frac{1}{2}V_{DD}$; note 2	4.4	5.5	6.6	mA
		I_{RN} = –25 μA; $V_{PHI} = \frac{1}{2}V_{DD}$	1.75	2.2	2.65	mA
$\Delta I_{PHI(S)}$	relative output current variation	I_{RN} = –62.5 μA; notes 2 and 3	–	2	8	%
$\Delta I_{PHI(S\ M)}$	output current matching	I_{RN} = –62.5 μA; $V_{PHI} = \frac{1}{2}V_{DD}$; notes 2 and 4	–	–	±500	μA
Fractional compensation PHP; normal mode (notes 5, 10 and 11)**; $V_{RN} = V_{DD}$; $V_{PHP} = \frac{1}{2}V_{DD}$**						
$I_{PHP(F\ N)}$	fractional compensation output current PHP as a function of FRD	I_{RF} = –62.5 μA; FRD = 1 to 7; notes 2 and 12	–675	–500	–325	nA
		I_{RF} = –25 μA; FRD = 1 to 7; note 12	–270	–200	–130	nA
Fractional compensation PHP; speed-up mode (notes 5, 11 and 13)**; $V_{RN} = V_{DD}$; $V_{PHP} = \frac{1}{2}V_{DD}$**						
$I_{PHP(F\ S)}$	fractional compensation output current PHP as a function of FRD	I_{RN} = –62.5 μA; FRD = 1 to 7; notes 2 and 12	–3.35	–2.50	–1.65	μA
		I_{RN} = –25 μA; FRD = 1 to 7; note 12	–1.35	–1.00	–0.65	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Fractional compensation PHI; speed-up mode (notes 5, 11 and 14)**; $V_{RN} = V_{DD}$; $V_{PHP} = \frac{1}{2}V_{DD}$**						
$I_{PHI(F)}$	fractional compensation output current PHI as a function of FRD	I_{RN} = –62.5 μA; FRD = 1 to 7; notes 2 and 12	–5.4	–4.0	–2.6	μA
		I_{RN} = –25 μA; FRD = 1 to 7; note 12	–2.15	–1.60	–1.05	μA
Charge pump leakage currents; charge pump not active						
$I_{PHP(LO)}$	output leakage current PHP	normal mode; V_{PHP} = 0.7 to V_{DDA} – 0.8 V note 5	–	10	750	nA
$I_{PHI(LO)}$	output leakage current PHI	normal mode; V_{PHI} = 0.7 to V_{DDA} – 0.8 V note 5	–	10	100	nA
$I_{PHA(LO)}$	output leakage current PHA	V_{PHA} = 0.7 to V_{DDA} – 0.8 V	–	10	750	nA

Notes

1. Operational conditions:
   a) Main and auxiliary divider enabled (EM = EA = 1).
   b) NA = 125.
   c) NR = 125.
   d) NM1 = 60.
   e) NM2 = 63.
   f) $f_{i(max)1} = f_{i(max)2}$ = 15 MHz.
   g) $f_{i(max)3}$ = 60 MHz.
   h) Lock condition.
   i) Normal mode; note 5
   j) $I_{RN} = I_{RF} = I_{RA}$ = 25 μA.
   k) CN = 255.
   l) PA = 0.
2. Limited supply voltage range 4.5 to 5.5 V.
3. The relative output current variation is defined as:
   $\frac{\Delta I_O}{I_O} = 2 \times \frac{I_2 - I_1}{|I_2 + I_1|}$; with V_1 = 0.7 V; $V_2 = V_{DD}$ – 0.8 V (see Fig.8).
4. The output current matching is measured when both (positive and negative current) sections of the output charge pumps are on.
5. When a serial ‘A’ word is programmed, the main charge pumps on PHP and PHI are in the ‘speed-up mode’ as long as STROBE = HIGH, otherwise the main charge pumps are in the ‘normal mode’.
6. Monotonicity is guaranteed with CN = 0 to 255.
7. Typical output current: $|I_{PHP(N)}| = -I_{RN} \times \frac{CN}{29}$; specification condition: CN = 255.

8. Typical output current: $|I_{PHP(S)}| = -I_{RN} \times CN \times \frac{2^{(CL+1)}+1}{29}$; specification conditions:
   a) CN = 255; CL = 1 or,
   b) CN = 75; CL = 3.
9. Typical output current: $|I_{PHI}| = -I_{RN} \times CN \times 2^{(CL+1)} \times \frac{CK}{29}$; specification conditions:
   a) CN = 160; CL = 3; CK = 1 or,
   b) CN = 160; CL = 2; CK = 2 or,
   c) CN = 160; CL = 1; CK = 4 or,
   d) CN = 160; CL = 0; CK = 8.
10. Typical fractional compensation output current: $I_{PHP(FN)} = I_{RF} \times \frac{FRD}{128}$; specification condition: FRD = 1 to 7.
11. The compensation current specified does not include the leakage current of this output.
12. FRD is the value of the 3-bit fractional accumulator.
13. Typical fractional compensation output current: $I_{PHP(FS)} = I_{RF} \times FRD \times \frac{2^{(CL+1)}+1}{128}$; specification conditions: FRD = 1 to 7; CL = 1.
14. Typical fractional compensation output current: $I_{PHI(F)} = I_{RF} \times FRD \times 2^{(CL+1)} \times \frac{CK}{128}$; specification conditions:
   a) FRD = 1 to 7; CL = 1; CK = 2 or,
   b) FRD = 1 to 7; CL = 2; CK = 1.

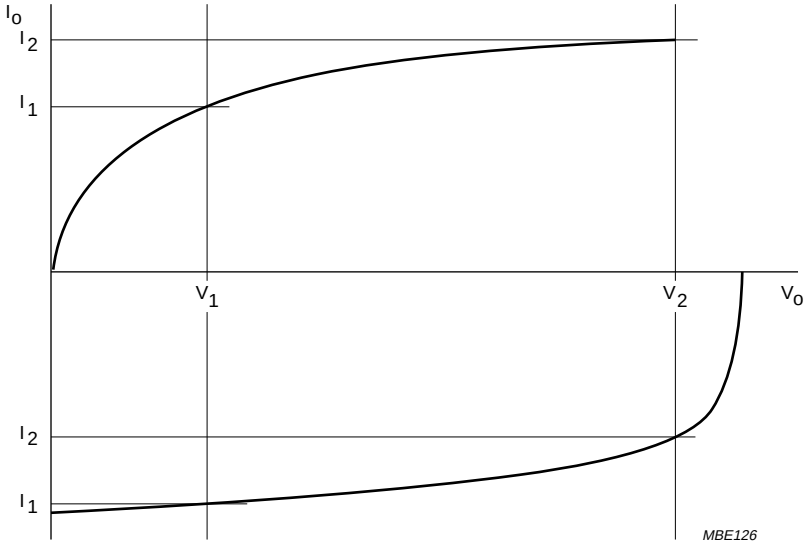

Fig.8 Relative output current variation.

AC CHARACTERISTICS

$V_{DDD} = V_{DDA}$ = 2.9 to 5.5 V; T_{amb} = –40 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Main divider (inputs INM1 and INM2)						
$f_{i(max)1}$	maximum input frequency		10	–	–	MHz
		note 1	30	–	–	MHz
$\Delta V_{INM(p-p)}$	differential input signal amplitude $V_{INM1} - V_{INM2}$ (peak-to-peak value)		600	–	–	mV
V_{CM}	common mode range for V_{INM1} and V_{INM2}		1	–	$V_{DD} - 1$	V
t_{pd}	propagation delay time from I_{NM1} and I_{NM2} to FB1 and FB2		–	–	60	ns
		note 1	–	18	30	ns
msr	mark-to-space ratio for differential input signals		35 : 65	–	65 : 35	
$Z_{i(min)}$	minimum input impedance	resistive; note 2	5	–	–	kΩ
		capacitive; note 2	–	–	5	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference divider (input INR)						
$f_{i(max)2}$	maximum input frequency		15	–	–	MHz
		note 1	30	–	–	MHz
$V_{i(p-p)}$	input signal amplitude AC coupled (peak-to-peak value)		300	–	–	mV
$Z_{i(min)}$	minimum input impedance	resistive; note 2	5	–	–	kΩ
		capacitive; note 2	–	–	5	pF
Auxiliary divider (input INA)						
$f_{i(max)3}$	maximum input frequency	prescaler enabled; PA = 0	35	–	–	MHz
		prescaler enabled; PA = 0; note 1	90	–	–	MHz
		prescaler disabled; PA = 1	15	–	–	MHz
		prescaler disabled; PA = 1; note 1	30	–	–	MHz
$V_{i(p-p)}$	input signal amplitude AC coupled (peak-to-peak value)		300	–	–	mV
$Z_{i(min)}$	minimum input impedance	resistive; note 2	5	–	–	kΩ
		capacitive; note 2	–	–	5	pF
Serial interface (inputs DATA, CLOCK and STROBE); see Fig.3						
f_{clk}	clock frequency		–	–	10	MHz
t_{HC}	clock HIGH time		30	–	–	ns
t_{LC}	clock LOW time		30	–	–	ns
t_{suDA}	DATA set-up time		30	–	–	ns
t_{hDA}	DATA hold time		30	–	–	ns
t_{suST}	STROBE set-up time		30	–	–	ns
t_{hST}	STROBE hold time		30	–	–	ns

Notes

1. Limited supply voltage range 4.5 to 5.5 V.
2. Periodically sampled; not 100% tested.