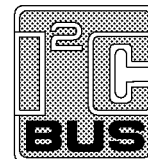# Data processor for cellular radio (DPROC)

UMA1000LT

FEATURES

- Single chip solution to all the data handling and supervisory functions
- Configuration to both AMPS and TACS
- I²C serial bus control
- All analog interface and filtering functions fully implemented on chip
- Error handling in hardware reduces software requirements
- Robust SAT decoding and transponding circuitry
- Low current consumption
- Small physical size
- Minimum external peripheral components required.

GENERAL DESCRIPTION

The UMA1000LT is a low power CMOS LSI device incorporating the data transceiving, data processing, and SAT functions (including on-chip filtering) for an AMPS or TACS hand-held portable cellular radio telephone.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage (pin 28)	3.0	5.0	5.5	V
I_{DD}	supply current (pin 28) normal operation with external clock	–	2.5	–	mA
T_{amb}	operating ambient temperature	–30	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1000LT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

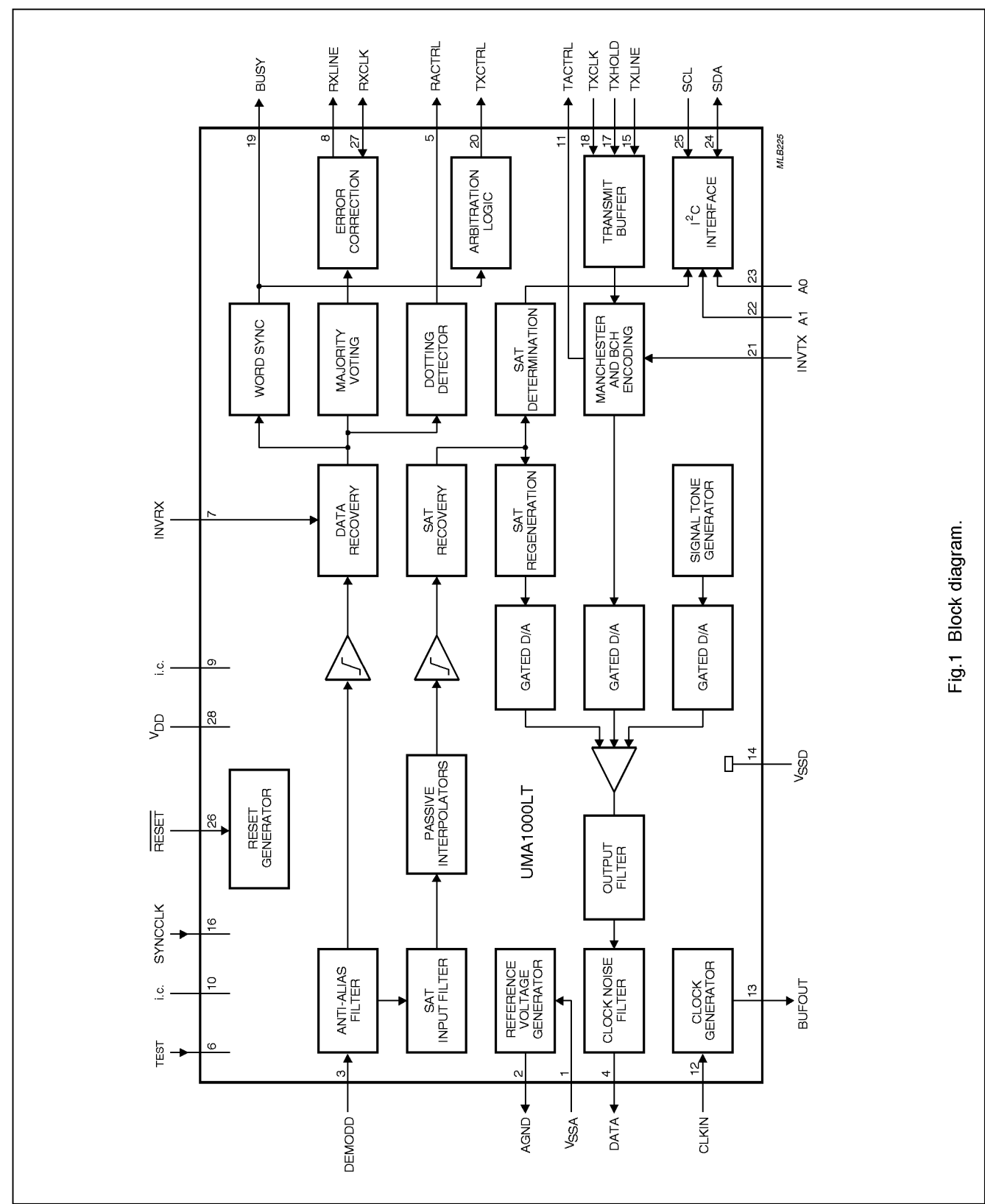## Data processor for cellular radio (DPROC)

UMA1000LT

BLOCK DIAGRAM

Fig.1 Block diagram.

Data processor for cellular radio (DPROC)   UMA1000LT

PINNING

| SYMBOL	PIN	DESCRIPTION
V_{SSA}	1	analog negative supply (0 V)
AGND	2	$(V_{DD} - V_{SSA})/2$ analog reference ground
DEMODD	3	received data signal input
DATA	4	transmitted data signal output
RACTRL	5	received audio control output
TEST	6	SCAN control input; used for power-on reset
INVRX	7	inverts sense of received data stream
RXLINE	8	received data signal output
i.c	9	internally connected; must be left open-circuit
i.c	10	internally connected; must be left open-circuit
TACTRL	11	transmitter audio control output
CLKIN	12	1.2 MHz external master clock input
BUFOUT	13	buffered output of internal clock oscillator
V_{SSD}	14	digital ground
TXLINE	15	transmitted data signal
SYNCCLK	16	SCAN CLOCK control input; used for power-on reset
TXHOLD	17	holds off transmission of data
TXCLK	18	transmitted data clock input
BUSY	19	reverse control channel status output
TXCTRL	20	transmitter control output
INVTX	21	inverts sense of transmitted data stream
A1	22	address input 1; used for power-on reset (I^2C-bus)
A0	23	address input 0 (I^2C-bus)
SDA	24	serial data input/output (I^2C-bus)
SCL	25	serial clock input (I^2C-bus)
$\overline{RESET}$	26	master reset input
RXCLK	27	received data clock input
V_{DD}	28	supply voltage (+5 V)
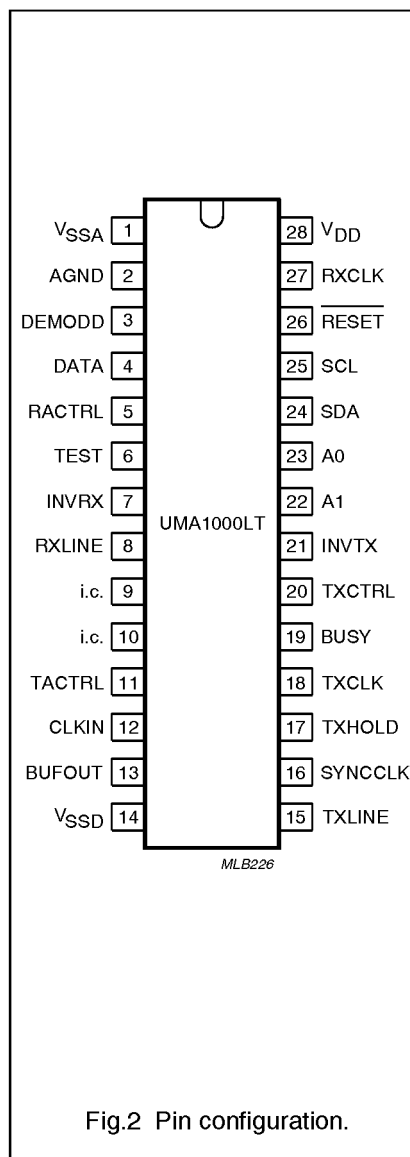
Fig.2 Pin configuration.

Data processor for cellular radio (DPROC)

UMA1000LT

LIMITING VALUES

In accordance with Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.8	+8.0	V
I_{DD}	supply current	−	50	mA
I_I	DC current (any input)	−	±10	mA
I_O	DC current (any output)	−	±10	mA
V_I	all input voltages	−0.8	$V_{DD} + 0.8$	V
P_{tot}	total power dissipation	−	300	mW
P_o	power dissipation per output	−	50	mW
T_{amb}	operating ambient temperature	−30	+70	°C
T_{stg}	storage temperature	−65	+150	°C

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = −30 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		3.0	5.0	5.5	V
I_{DD}	supply current	normal operation; note 1	−	2.5	−	mA
Digital inputs (note 2)						
V_{IL}	LOW level input voltage		−0.3	−	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	−	$V_{DD} + 0.3$	V
C_I	input capacitance		−	−	6	pF
Digital outputs (note 2)						
V_{OL}	LOW level output voltage	I_{sink} = 1 mA	−	−	0.4	V
V_{OH}	HIGH level output voltage	I_{source} = 1 mA	V_{DD}−0.4	−	−	V
Open-drain outputs (note 3)						
V_{OL}	LOW level output voltage	I_{sink} = 2 mA	−	−	0.4	V
Open-drain SDA						
V_{OL}	LOW level output voltage	I_{sink} = 3 mA	−	−	0.4	V

Notes

1. 1.2 MHz clock on CLKIN, SYNCCLK HIGH, outputs unloaded analog part operating.

2. All digital inputs and outputs of DPROC are compatible with standard CMOS devices and the following general characteristics apply.

3. Open-drain outputs have no internal pull-up resistors.

Data processor for cellular radio (DPROC)

UMA1000LT

FUNCTIONAL DESCRIPTION

General

The UMA1000LT (DPROC) is a single-chip CMOS device which handles the data and supervisory functions of an AMPS or TACS subscriber set.

These functions are:

• Data reception and transmission

• Control and voice channel exchanges

• Error detection, correction, decoding and encoding

• Supervisory Audio Tone decoding and transponding

• Signalling Tone generation.

control data occurs on these voice channels by briefly blanking the audio and simultaneously transmitting the data. The data burst is brief and barely noticeable by the user. A data rate of 10 kbits/s is used in the AMPS system and 8 kbits/s in TACS. The signalling formats for both Forward Channels (base to mobile) and Reverse Channels (mobile to base) are shown in Fig.3.

A function known as Supervisory Audio Tone (SAT), a set of 3 audio tones (5970, 6000 and 6030 Hz), is used to indicate the presence of the mobile on the designated voice channel. This signal, which is analogous to the On-Hook signal on land lines, is sent out to the mobile by the base station on the Forward Voice

Another voice channel associated signal is Signalling Tone (ST). This tone (8 kHz TACS, 10 kHz AMPS) is generated by the mobile and is sent in conjunction with SAT on the Reverse Voice Channel to serve as an acknowledgement signal to a number of system orders.
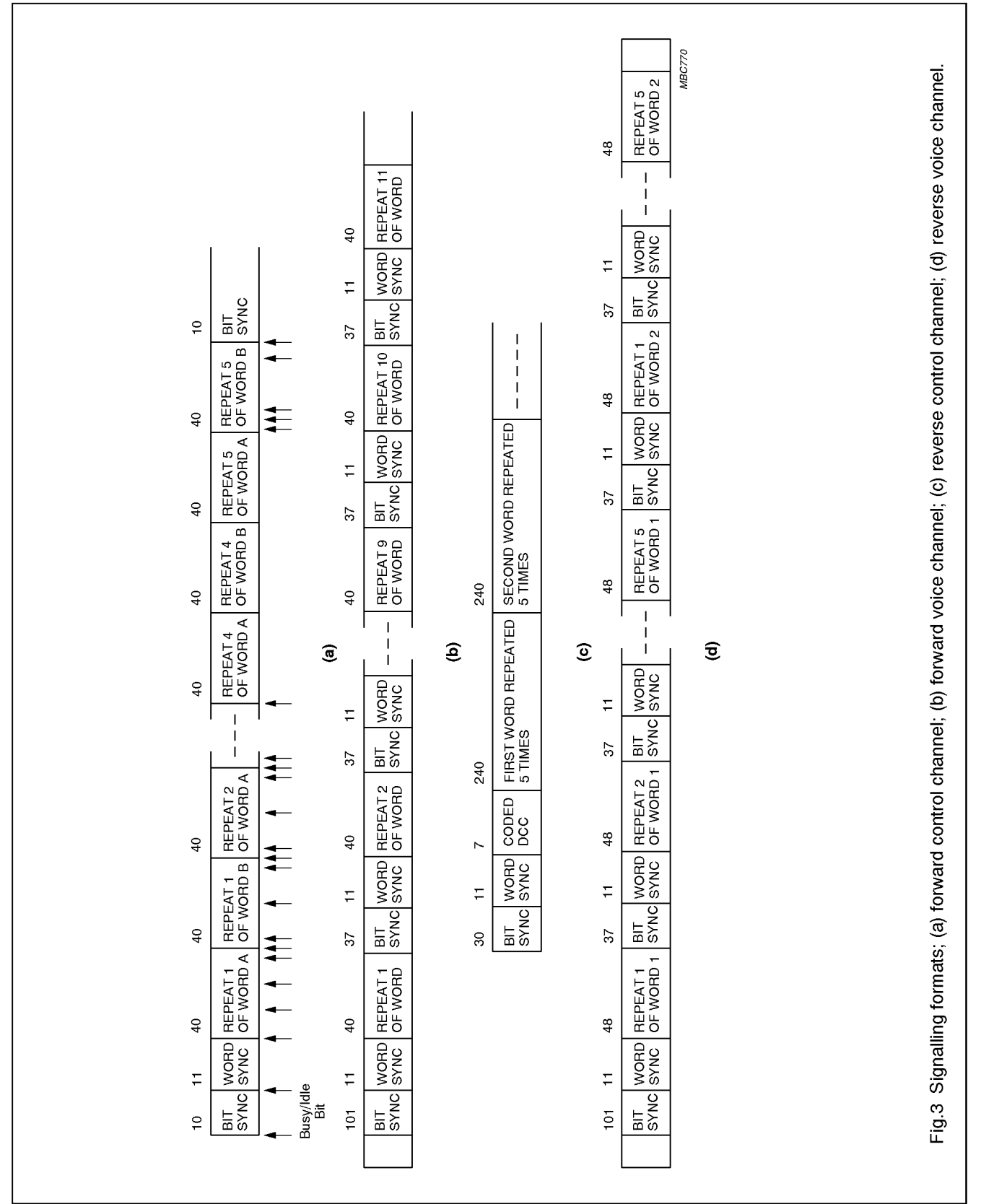
The key requirements of a hand-held portable cellular set are:

• Small physical size

• Minimum number of interconnections (serial bus)

• Low power consumption

• Low cost.

The DPROC is a member of our Cellular Radio chip set, based on the I^2C-bus, which meets these

Fig.3 Signalling formats; (a) forward control channel; (b) forward voice channel; (c) reverse control channel; (d) reverse voice channel.

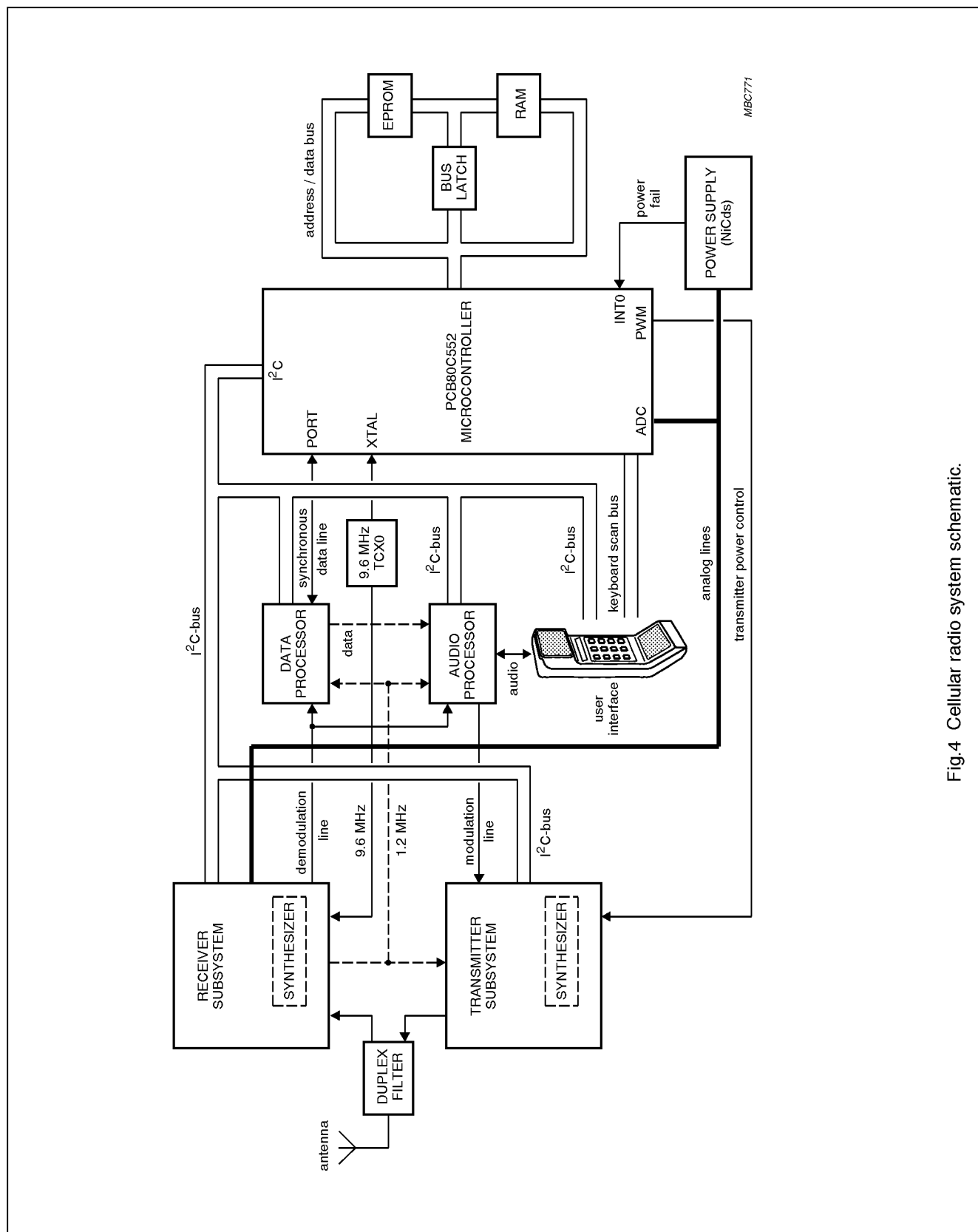# Data processor for cellular radio (DPROC)

UMA1000LT

Fig.4 Cellular radio system schematic.

MBC771

Data processor for cellular radio (DPROC)

UMA1000LT

EXTERNAL PIN DESCRIPTION

Supply (V_{DD}; V_{SSA}; V_{SSD}; AGND)

Both V_{SSA} and V_{SSD} must be connected to common ground.

SYMBOL	DESCRIPTION
V_{DD}	positive supply voltage for digital and analog circuitry
V_{SSA}	negative supply voltage for analog circuitry (0 V)
V_{SSD}	digital ground (0 V)
AGND	internally generated reference ground based by internal analog circuitry; voltage level $(V_{DD}-V_{SSA})/2 \pm 2\%$

System clock (CLKIN; BUFOUT)

CLKIN is a digital input for the externally generated 1.2 MHz master clock. This signal should be accurate to 100×10^{-6} and have a worst case of 60:40 mark-space ratio. BUFOUT is the buffered output of the clock oscillator and provides the option of generating the clock signal on chip by connecting a 1.2 MHz crystal between BUFOUT and CLKIN.
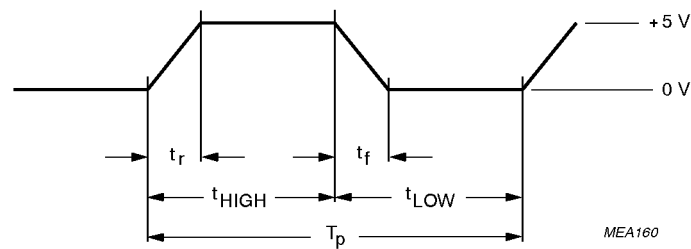

Fig.5 System clock timing diagram.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
T_p	clock period time	833.25	833.33	833.42	ns
t_{HIGH}	HIGH time	40%	50%	60%	T_p
t_{LOW}	LOW time	–	$T_p - t_{HIGH}$	–	
t_r	rise time	–	50	–	ns
t_f	fall time	–	50	–	ns

I²C serial data link (SDA; SCL)

SDA is the bi-directional data line; SCL the clock input from an I²C master. These constitute a typical I²C link and conform to standard characteristics as defined in the I²C-bus specification.

• Data rate: up to 100 kbits/s.

Data processor for cellular radio (DPROC)

UMA1000LT

Slave Address Select (A0; A1)

Selection of the device slave address is achieved by connecting A0 to either V_{SSD} or V_{DD} and connecting A1 to either pin 16 and pin 6 or to V_{DD}. The slave address is defined in accordance with the I^{2}C specifications as shown in Fig.6.

| 1 | 1 | 0 | 1 | 1 | A1 | A0 | R/$\overline{W}$ |

MBC766

Fig.6 Device slave address.
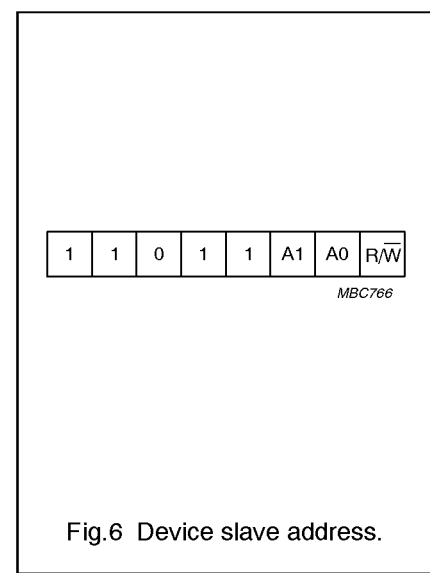
Power-up state

DPROC will not respond reliably to any inputs (including $\overline{RESET}$) until 100 μs after the power supply has settled within the specified tolerance. The analog sections of the device will have stabilized within 5 ms. No power-on reset is provided, therefore before the device can enter normal operation TEST and SYNCCLK must be pulsed HIGH. The reset pulse on these pins must have a minimum period of 250 μs and the fall time of the negative going edge must be faster than 1 μs. Pin A1 must remain HIGH during this reset period therefore if the A1 bit of the I^{2}C address is required to be logic 0. A1 may be connected to TEST and SYNCCLK. If it is required to be at logic 1 then A1 may be permanently connected to V_{DD}. If it is required that A0 = logic 1, then a normal master reset (pin 26) sequence must follow the power-on reset sequence to get the internal registers in the defined state.

After the power-on reset a dummy transmission should be made to initiate internal DPROC counters. This transmission should be made with arbitration (ABREN) disabled and the RF transmitter stage switched OFF. Figure 7 shows the power-on reset sequence.

Master reset ($\overline{RESET}$)

$\overline{RESET}$ is an asynchronous active LOW master reset input, with a minimum active pulse width of 2 μs which may be used to reset certain logic within DPROC to a predefined state as illustrated in Tables 1 and 2. Alternatively, DPROC may be set into a known initial state be setting the I^{2}C control register as required. The internal reset sequence after a negative pulse on $\overline{RESET}$ takes 250 μs.
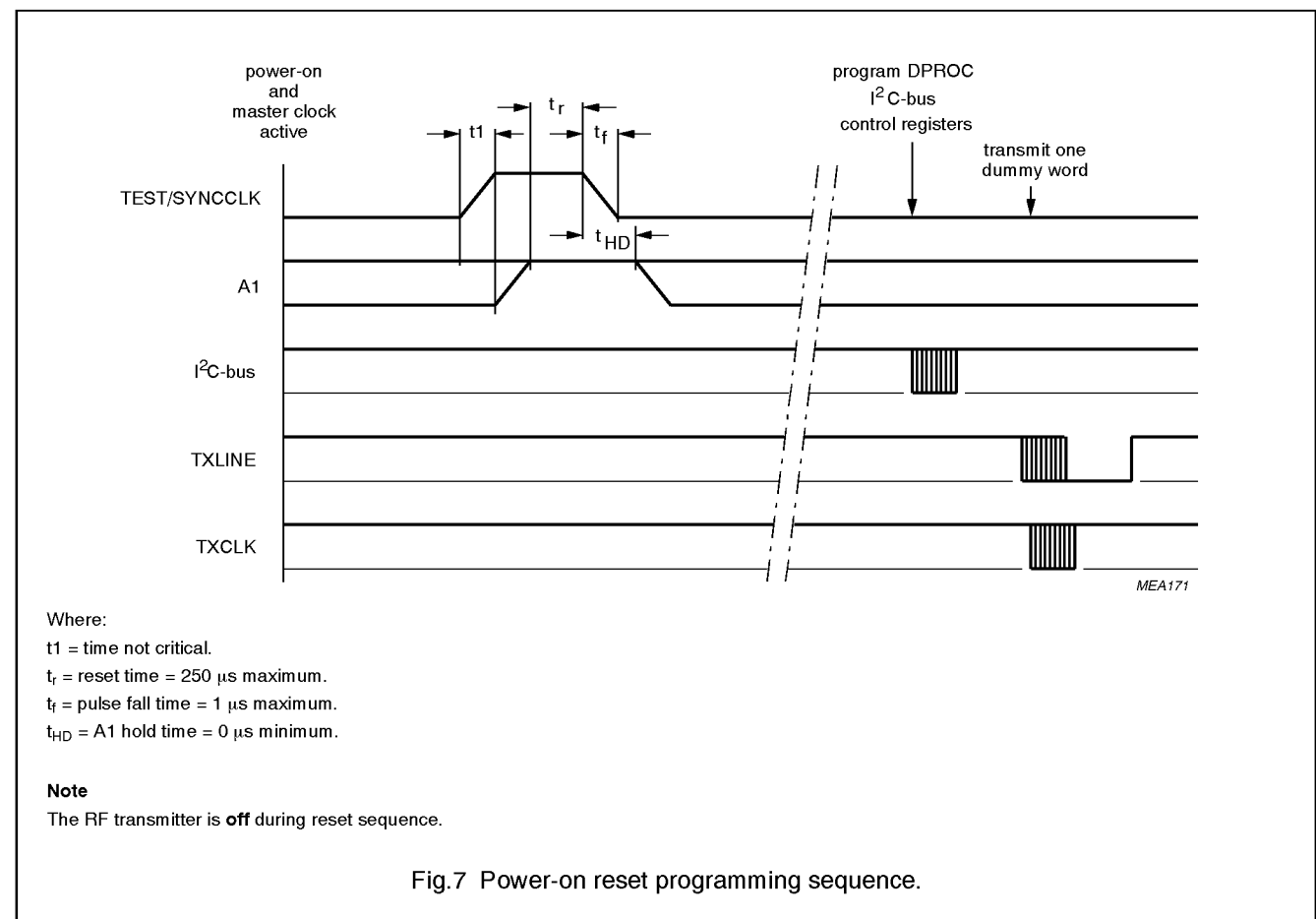
Data processor for cellular radio (DPROC)

UMA1000LT

Fig.7 Power-on reset programming sequence.

Where:

t1 = time not critical.

t_r = reset time = 250 μs maximum.

t_f = pulse fall time = 1 μs maximum.

t_{HD} = A1 hold time = 0 μs minimum.

Note

The RF transmitter is **off** during reset sequence.

Table 1   Predefined state of the digital output pins

OUTPUT	STATE
RXLINE	HIGH
TXCTRL	HIGH
TACTRL	HIGH
RACTRL	HIGH
BUSY	HIGH

Table 2   Predefined state of I^{2}C registers

REGISTER	BIT							
	7	6	5	4	3	2	1	0
Control	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
SATD	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
TST	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW

Data processor for cellular radio (DPROC)   UMA1000LT

Data Transfer Link (RXLINE; TXLINE; TXHOLD; TXCLK and RXCLK)

RXLINE, TXLINE, TXCLK and RXCLK provide a dedicated serial data link for the transfer of system data messages between DPROC and the system controller at variable rates of up to 200 kbits/s.

TXHOLD allows the system controller to preload the DPROC transmit register with one word without the data being transmitted. DPROC then starts transmitting the instant TXHOLD is driven LOW.

- RXCLK: clock input from system controller
- RXLINE: data output from DPROC to system controller
- TXCLK: clock input from system controller
- TXLINE: open drain data bi-directional line to the system controller
- TXHOLD: (HIGH) holds off transmission of data
- Data rate: up to 200 kbits/s.

Note

A minimum mean data transfer rate for the received data of 2.1 kbits/s (AMPS) and 1.7 kbits/s (TACS) is required to ensure contiguity of message words.

The format for received and transmitted data words is shown in Fig.15(a) and Fig.15(b) respectively. The receive and transmit data timing is illustrated in Fig.16(a) and Fig.16(b) respectively.

Transmitter Control (TXCTRL)

TXCTRL is an open-drain output used to disable the transmitter during a Reverse Control Channel access failure.

- output level HIGH: RF enable
- output level LOW: RF disable.

Transmitter Audio Enable (TACTRL)

TACTRL is an open-drain digital output signal used to blank the audio path and enable the data path to the modulator during data bursts on the Reverse Voice Channel.

- output level HIGH: audio enabled
- output level LOW: audio muted.

Receiver Audio Enable (RACTRL)

RACTRL is an open-drain digital output used to blank the audio path to the earpiece when a sequence of dotting and word sync is detected.

RACTRL and TACTRL functions can be combined using one line.

- output level HIGH: audio enabled
- output level LOW: audio muted.

Reverse Control Channel Status (BUSY)

BUSY is a digital output giving the status of the Reverse Control Channel. This is determined by a majority decision on the result of the last 3 consecutive Busy/Idle bits and has the following logic levels:

- output level HIGH: channel busy
- output level LOW: channel idle.

On a voice channel BUSY indicates channel idle.

Invert Receive Data (INVRX)

Enables an additional inverter in the receive data path. This allows RF demodulators with high or low local oscillators to be used. The TACS and AMPS specifications define a NRZ encoded logic 1 as a LOW-to-HIGH transition in the centre of a data bit period. The polarity of the demodulated data stream into DPROC depends on the receiver local oscillator.

- input HIGH: data inverted
- input LOW: data normal.

Invert Transmit Data (INVTX)

Enables an additional inverter in the transmit data path. This allows RF modulators with high or low local oscillators to be used. The TACS and AMPS specifications define a NRZ encoded logic 1 as a LOW-to-HIGH transition in the centre of a data bit period. The polarity of the modulated data stream depends on the transmitter local oscillator.

- input HIGH: data inverted
- input LOW: data normal.

Transmitted Data Output (DATA)

Data is an analog output which provides Manchester encoded and filtered data signal SAT and signalling tone. This signal should normally be AC coupled into the Audio/Data summer.

- DC level: analog ground (AGND)

- signal level: $\frac{2}{5}V_{DD}$ V (p-p) for signalling tone; signal level with filtered data signal

- signal tolerance: 2% + supply voltage variation (ΔV_{DD})

- minimum load capacitance: 10 kΩ

- maximum load capacitance: 2 nF

- maximum output impedance: 50 Ω.

Received Data Input (DEMODD)

Demodd inputs analog data and SAT signals from the RF demodulator. This pin should normally be AC coupled.

- DC level: analog ground (AGND)

- maximum data level: $\frac{V_{DD}}{5} \times 1$ V (p-p)

- nominal data level: $\frac{V_{DD}}{5} \times 250$ mV (p-p)

- minimum data level: $\frac{V_{DD}}{5} \times 200$ mV (p-p)

- minimum SAT level: 50 mV (p-p)

- input impedance: min. 1 MΩ.

Data processor for cellular radio (DPROC)   UMA1000LT

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

System configuration

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

Timing specifications

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig.12.

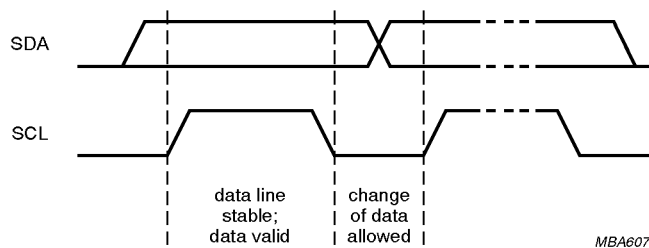Data processor for cellular radio (DPROC)
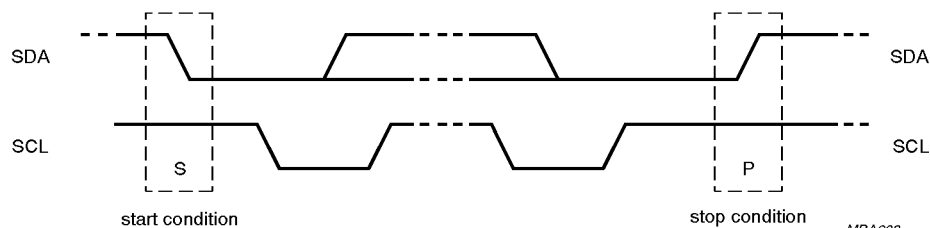
UMA1000LT

Fig.8 Bit transfer.

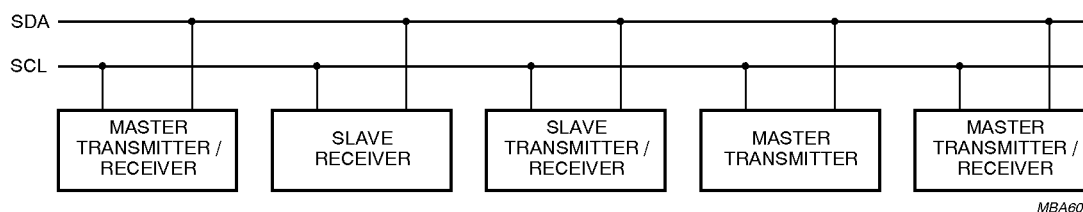Fig.9 Definition of start and stop conditions.

Fig.10 System configuration.

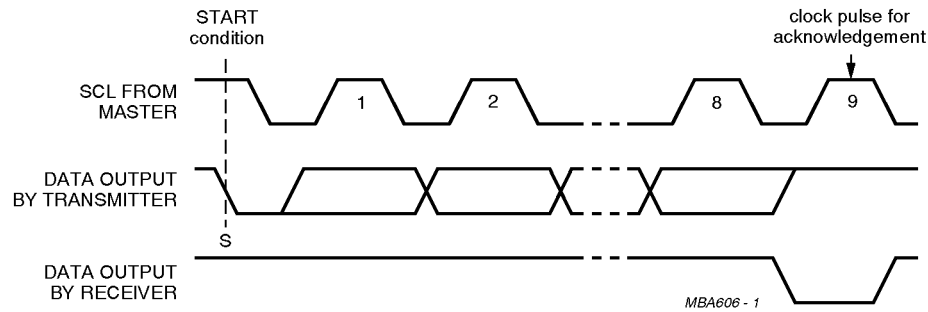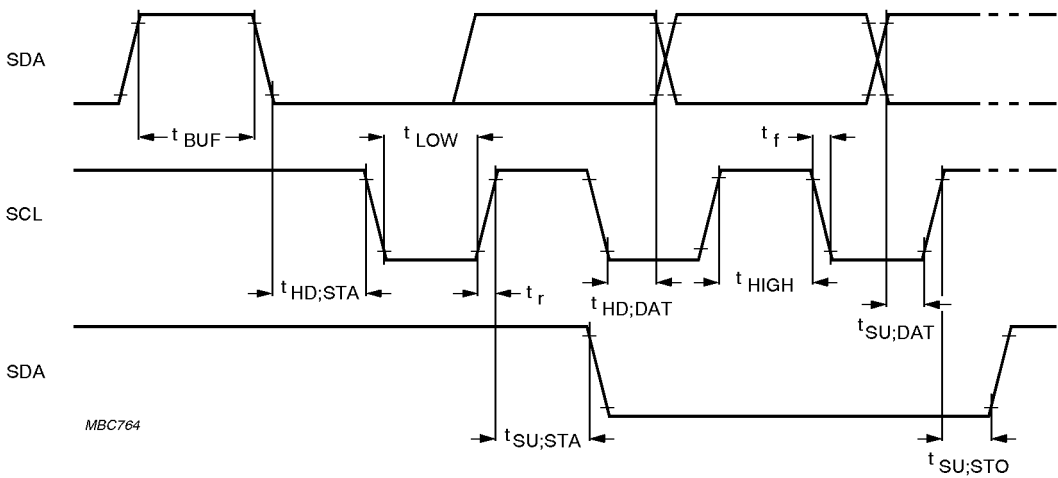## Data processor for cellular radio (DPROC)

UMA1000LT

Fig.11 Acknowledgement on the I²C-bus.

All the values refer to 10% and 90% levels with a voltage swing of V_{DD} to V_{SS}.

Fig.12 Timing.

Data processor for cellular radio (DPROC)   UMA1000LT

Timing

SYMBOL	TIMING	DESCRIPTION
t_{BUF}	$t \geq t_{LOW(min)}$	the minimum time the bus must be free before a new transmission can start
$t_{HD; STA}$	$t \geq t_{HIGH(min)}$	start condition hold time
$t_{LOW(min)}$	4.7 μs	clock LOW period
$t_{HIGH(min)}$	4 μs	clock HIGH period
$t_{SU; STA}$	$t \geq t_{LOW(min)}$	start condition set-up time, only valid for repeated start code
$t_{HD; DAT}$	$t \geq 0$ μs	data hold time
$t_{SU; DAT}$	$t \geq 250$ ns	data set-up time
t_r	$t \leq 1$ μs	rise time of both the SDA and SCL line
t_f	$t \leq 300$ ns	fall time of both the SDA and SCL line
$t_{SU; STO}$	$t \geq t_{LOW(min)}$	stop condition set-up time
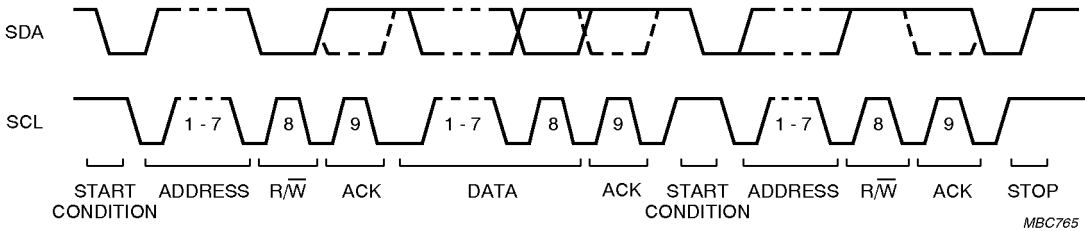
Where:
Clock $t_{LOW(min)}$: 4.7 μs.
Clock $t_{HIGH(min)}$: 4 μs.
The dashed line is the acknowledgement of the receiver.
Maximum number of bytes: unrestricted.
Premature termination of transfer: allowed by generation of STOP condition.
Acknowledge clock bit: must be provided by the master.

Fig.13 Complete data transfer.

Data processor for cellular radio (DPROC)

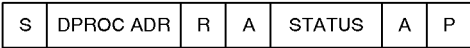## UMA1000LT

I²C REGISTERS

General

The I²C register block resides internally within the I²C interface block and contains various items of status and control information which are transferred to and from DPROC via the I²C-bus. The block is organized into four 8-bit registers:

- Status Register: contain read only items
- Control Register: contain write only items
- SAT Programmable Phase Shift Register: contain write only items
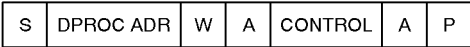- TEST Register.

Note

In normal operation the SAT delay register and the TEST register require programming only after a device reset.
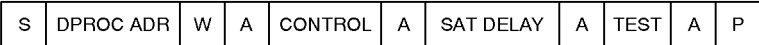
Table 3 Register map

REGISTER	BIT							
	7	6	5	4	3	2	1	0
Status	–	–	WYNSC	BUSY	TXABRT	TXIP	MSCC1	MSCC0
Control	–	SERV	STS	TXRST	ABREN	FVC	STEN	SATEN
SATD	<---SAT delay data--->							

```
┌───┬───────────┬───┬───┬────────┬───┬───┐
│ S │ DPROC ADR │ R │ A │ STATUS │ A │ P │
└───┴───────────┴───┴───┴────────┴───┴───┘
```

(a)

```
┌───┬───────────┬───┬───┬─────────┬───┬───┐
│ S │ DPROC ADR │ W │ A │ CONTROL │ A │ P │
└───┴───────────┴───┴───┴─────────┴───┴───┘
```

(b)

```
┌───┬───────────┬───┬───┬─────────┬───┬───────────┬───┬──────┬───┬───┐
│ S │ DPROC ADR │ W │ A │ CONTROL │ A │ SAT DELAY │ A │ TEST │ A │ P │
└───┴───────────┴───┴───┴─────────┴───┴───────────┴───┴──────┴───┴───┘
```

MBC767

(c)

Where:
S: START condition.
W: read/write bit (logic 0 = write).
R: read/write bit (logic 1 = read).
A: acknowledge bit.
P: STOP condition.
DPROC ADR: slave address of DPROC.
TEST: must be programmed to logic 0 for normal operation.

Fig.14 I²C data format; (a) read from DPROC status register; (b) write to DPROC control register; (c) write to all DPROC registers.

Data processor for cellular radio (DPROC)

UMA1000LT

Status Register

This is read only register containing DPROC status information.

MEASURED SAT COLOUR CODE (MSCC1; MSCC0)

MSCC1 and MSCC0 provide information about the current measured SAT colour code in accordance with Table 4.

Table 4 Measured SAT colour code

MSCC1	MSCC0	SAT frequency (Hz)
0	0	5970
0	1	6000
1	0	6030
1	1	no valid SAT

TRANSMISSION IN PROGRESS (TXIP)

TXIP indicates whether DPROC is currently accessing the Reverse Control or Voice Channels.

• logic 1: data transmission in progress

• logic 0: transmission not in progress.

TRANSMISSION ABORT STATUS (TXABRT)

TXABRT indicates that a Reverse Control Channel Access Attempt has been aborted by DPROC without successful message transmission.

• logic 1: transmission attempt aborted

• logic 0: no access collision detected.

REVERSE CONTROL CHANNEL STATUS (BUSY)

BUSY gives the status of the Reverse Control Channel. This is determined by a majority decision on the result of the last 3 consecutive Busy/Idle bits on the Forward Control Channel.

• logic 1: channel busy

• logic 0: channel idle.

On a voice channel the BUSY bit defaults to the set state.

Note

This signal is also routed to the BUSY output pin.

WORD SYNCHRONIZATION INDICATOR (WSYNC)

WSYNC indicates whether DPROC has acquired frame synchronization according to the Forward Control Channel format.

• logic 1: frame synchronization acquired

• logic 0: no frame synchronization.

Data processor for cellular radio (DPROC)   UMA1000LT

Control Register

This is a write only register containing DPROC control information.

SAT PATH ENABLE (SATEN)

SATEN enables the SAT transponded signal to be output on external pin DATA.
- logic 1: SAT tone enabled
- logic 0: SAT tone inhibited.

SIGNALLING TONE (ST) PATH ENABLE (STEN)

STEN enables the Signalling Tone to be output on external pin DATA.
- logic 1: ST enabled
- logic 0: ST inhibited.

CHANNEL FORMAT SELECT (FVC)

FVC selects the required channel format.
- logic 1: voice channel format
- logic 0: control channel format.

TRANSMISSION ABORT PERMISSION (ABREN)

ABREN indicates whether DPROC has permission to abort data transmission and disable RF on the Reverse Control Channel following the detection of a channel access attempt collision.
- logic 1: RF disable allowed
- logic 0: RF disable inhibited.

MESSAGE TRANSMISSION ABORT (TXRST)

TXRST terminates a message being transmitted on the reverse channel. It is a monostable signal which when activated causes a reset of the message transmission circuitry and causes TXABRT and TXIP I²C signals to be reset.

This signal does not clear the DPROC transmit register; therefore if a word has been loaded into DPROC after a TXABRT has occurred the control line TXHOLD should be held LOW to allow the word to be cleared from the DPROC input register.
- logic 1: reset active
- logic 0: reset inactive.

SYSTEM TYPE SELECT (STS)

STS selects required system format.
- logic 1: AMPS
- logic 0: TACS.

Note

Toggling this signal also resets the receive logic in DPROC.

SERVING SYSTEM SELECT (SERV)

SERV selects which of the serving system data streams (A or B) is accepted.
- logic 1: system A selected
- logic 0: system B selected.

SAT PROGRAMMABLE DELAY REGISTER (SATD)

SATD programs the value of phase shift which is applied to the SAT tones in the SAT Regeneration Block. This value will be determined and programmed into the System Controller during manufacture. The recovered SAT is delayed in time by approximately 0.8 μs x value in the register which corresponds to approximately 1.8 degrees x value in the register. The total phase shift is limited to 360 degrees.

The ability to adjust SAT phase angle is not necessary in current AMPS and TACS systems. Therefore this register should normally be in AMPS and TACS, this function is not necessary and should programmed to zero.

Data processor for cellular radio (DPROC)   UMA1000LT

DIGITAL CIRCUIT BLOCKS

General

The majority of the digital circuitry within the DPROC device is identical for both AMPS and TACS. The device has little additional redundancy to implement both systems. The functions of these blocks are described in the following sections and relate to those shown in Fig.1.

Data Recovery

The Data Recovery Block receives wideband Manchester encoded data in sampled and sliced form from the Strobed Comparator Block, on which it performs the following functions:

• clock recovery

• Manchester decoding

• data regeneration.

The Clock Recovery Block extracts an 8 or 10 kHz (TACS or AMPS) phase-locked clock signal from the Manchester encoded data stream. This is implemented using a digital-phase-locked-loop (PLL) which has an adjustable 'bandwidth' to provide both fast acquisition and low jitter.

Manchester decoding is performed by exclusive ORing the recovered Manchester encoded data with the recovered clock.

The NRZ data regeneration is performed by a digital integrate and dump circuit. This consists of an up/down counter that counts 1.2 MHz cycles during the data period. The sense of the count is determined by the result of the Manchester Decoder output. The number of counts is sampled at the end of a data period. If this number exceeds a threshold the data is latched as a 1 otherwise it is latched as a 0.

SAT Processing

The Supervisory Audio Tone processing consists of the following functions:

• SAT recovery

• SAT determination

• SAT regeneration.

SAT RECOVERY

The SAT Recovery Block receives a filtered and sliced SAT signal which must be recovered before being routed to the Determination and Regeneration Blocks.

The recovery is performed using a digital phase-locked-loop.

SAT DETERMINATION

The SAT Determination Block indicates which, if any, of the valid SAT tones is detected from the recovered SAT. The AMPS and TACS specifications require that a determination is made at least every 250 ms. Determination involves counting the number of cycles of the regenerated SAT in this time period. This count is then compared to a set of four known counts which define the boundaries between the SAT frequencies and the SAT not valid events. The result is then coded into the I²C status registers MSCC0 and MSCC1 as shown in Table 5.

SAT REGENERATION

The SAT Regeneration Block generates a digital SAT stream from the recovered SAT stream for transponding back to the base station. The AMPS and TACS specifications require the SAT to be

transponded with a maximum phase shift of 20 degrees between the point the modulated RF signal enters the mobile from the base station, and the point the modulated RF leaves the mobile. A variable phase compensation circuit is provided in DPROC to shift the recovered SAT through 0 to 360 degrees before being passed to the output summing network. The degree of phase shift is determined during manufacture of the set and the required additional phase shift is stored in non-volatile RAM and programmed via I²C at each power-on cycle. The phase correction is performed by a counter delay method using signals which are phase locked to the recovered SAT.

Dotting Detector

The Dotting Detector Block determines whether a data inversion (dotting) pattern has been received on the Forward Voice Channel. The detection of 32 bits of data inversion indicates that the Clock Recovery Block has acquired bit synchronization and that the narrow bandwidth mode on the clock recovery phase-locked-loop is selected. This signal is also used to indicate that a data burst is expected and activates the audio mute RACTRL, after a Word Synchronization Block has been received, for the duration of the burst.

Data processor for cellular radio (DPROC)

UMA1000LT

Table 5 Status registers MSCC0, MSCC1; decoded SAT frequencies

REGISTER		SAT frequency band (Hz ±2 Hz)	decoded SAT (Hz)
MSCC0	MSCC1		
1	1	max. 5956	not valid
0	0	5956 to 5986	5970
0	1	5986 to 6014	6000
1	0	6014 to 6046	6030
1	1	min. 6046	not valid

Word Synchronization Detector

The Word Synchronization Block performs the following functions:

• Frame Synchronization

• Reverse Control Channel status (B/I determination)

• Valid Serving System determination.

These functions are associated solely with the Forward Control Channel and have no meaning on the Forward Voice Channel.

Information in a data stream is identified by its position with respect to a unique synchronization word. This synchronization word is an 11-bit Barker code which has a low probability of simulation in an error environment, and can be easily detected. Data received is only considered valid at times when DPROC has achieved frame synchronization. In this condition the block leaves its search mode and enters its lock mode. This is indicated by bit WSYNC being set HIGH. In order to achieve this two consecutive synchronization words separated by 463 bits must be detected. Once in lock mode, the synchronization word detector is examined every 463 bits

and only loses frame synchronization after 5 consecutive unsuccessful attempts at detecting the synchronization word have been made. At this point bit WSYNC is cleared and the device is returned to its search mode. On the Forward Voice Channel detection of the synchronization word indicates that the following 40 bits are valid data. Information detailing the status of the Reverse Control Channel is given by the Busy/Idle bits. These occur at intervals of 11 bits within the frame, the first occurring immediately following the synchronization word. The status of the channel is determined by a majority decision on the last three consecutive Busy/Idle bits.

Majority Voting Block

The Majority Voting Block performs the following functions:

• identifying position and validity of frames in the received data stream

• extracting five repeats of each word from a valid frame

• performing a bit-wise majority decision on the five repeats of the data word.

The validity of the frames is determined by setting a counter in operation which times out and resets the circuitry after 920 or 463 bit periods from detecting valid word synchronization. The time out period selected depends on whether DPROC is monitoring the Forward Voice or Control Channel respectively.

Up to five repeats of the message word are searched for and extracted by DPROC. On the forward Voice Channel DPROC will extract the first five words that occur for which a correct synchronization word is found. These words can occur in any position in the frame. A serial majority vote is performed as the fifth word is being extracted.

Data processor for cellular radio (DPROC)

UMA1000LT

Error Correction Block

The Error Correction Block performs the following functions:

- extraction of a valid message from the Majority-Voted Word
- computation of the S1 and S3 syndromes
- correction of up to one error in the word
- communication of received data to the System Controller via the Received Data Serial Link.

Interpretation of parity of a received word is obtained from knowledge of the syndromes of the word. The syndromes are calculated using feedback shift registers with two characteristic equations:

$1 + X + X^6$ and $1 + X + X^2 + X^4 + X^6$

Once the syndromes of a received word are known, it is possible to determine if a correctable error is present. DPROC only corrects up to one error although the code used has a Hamming distance of five. The occurrence of two or more errors is signalled by setting the BCH error flag, which is communicated to the System Controller via the Received Data Serial Link.

Received Data Serial Link

The Received Data Serial Link transfers data and control information from DPROC to the System Controller. The data is transferred on RXLINE under control of a clock signal RXCLK, generated by the System Controller. The system controller is informed of the arrival of a decoded data word in the DPROC output register by RXLINE being driven LOW. If the system controller chooses to ignore the received data or only partially clock the data out, the DPROC will reset the receive buffer for the next word after the period RWIN (see Fig.16).

DATA FORMAT

Each Received Data word consists of 4 bytes. The word format is shown in Fig.15(a). The sense and function of the fields is shown in Table 6.

LINK PROTOCOL

The Received Data protocol is described by the timing diagram Fig.16(a) and has the following parameters:

- maximum receive window (RWIN)
    - Control Channel (TACS) = 47 ms
    - Control Channel (AMPS) = 37 ms
- minimum clock period ($t_{CLK(min)}$) = 2 μs
- minimum clock hold-off (t_{WAIT}) = 100 μs.

Transmit Data Serial Interface

The Transmit Data Serial Link performs reception of data from the System Controller to DPROC over a dedicated line TXLINE. The transfer of data is synchronous with a clock signal TXCLK, generated by the System Controller.

DATA FORMAT

Each Transmit Data word consists of 5 bytes. The word format is shown in Fig.15(b). The sense and function of the fields is shown in Table 7.

LINK PROTOCOL

Messages are normally up to 5 words in length on the Reverse Control Channel and up to 2 words in length on the Reverse Voice Channel. However, DPROC will transmit messages of any word length. These must be transmitted on the data stream without interruption. To avoid the need for large buffer areas, a flexible protocol is used to allow DPROC to control the transfer of data

words. DPROC has an on-chip buffer which can hold one complete word of a message. While new words are being loaded into DPROC, within the time period Buffer clear to end of TWIN, DPROC will maintain uninterrupted data transmission. The System Controller can abort the transmission of a message at any point activating the I²C signal TXRST. This signal causes the interface to return to its power-up state and resets TXIP and TXABRT (see Table 3). On completion of these tasks TXRST will return to its inactive state. The Transmit Data Protocol is described by the timing diagram shown in Fig.16(b) and has the following parameters:

- maximum transmit window (TWIN)
    - voice channel (TACS) = 60 ms
    - voice channel (AMPS) = 48 ms
    - control channel (TACS) = 29 ms
    - control channel (AMPS) = 23 ms
- minimum clock period ($t_{CLK(min)}$) = 2 μs.
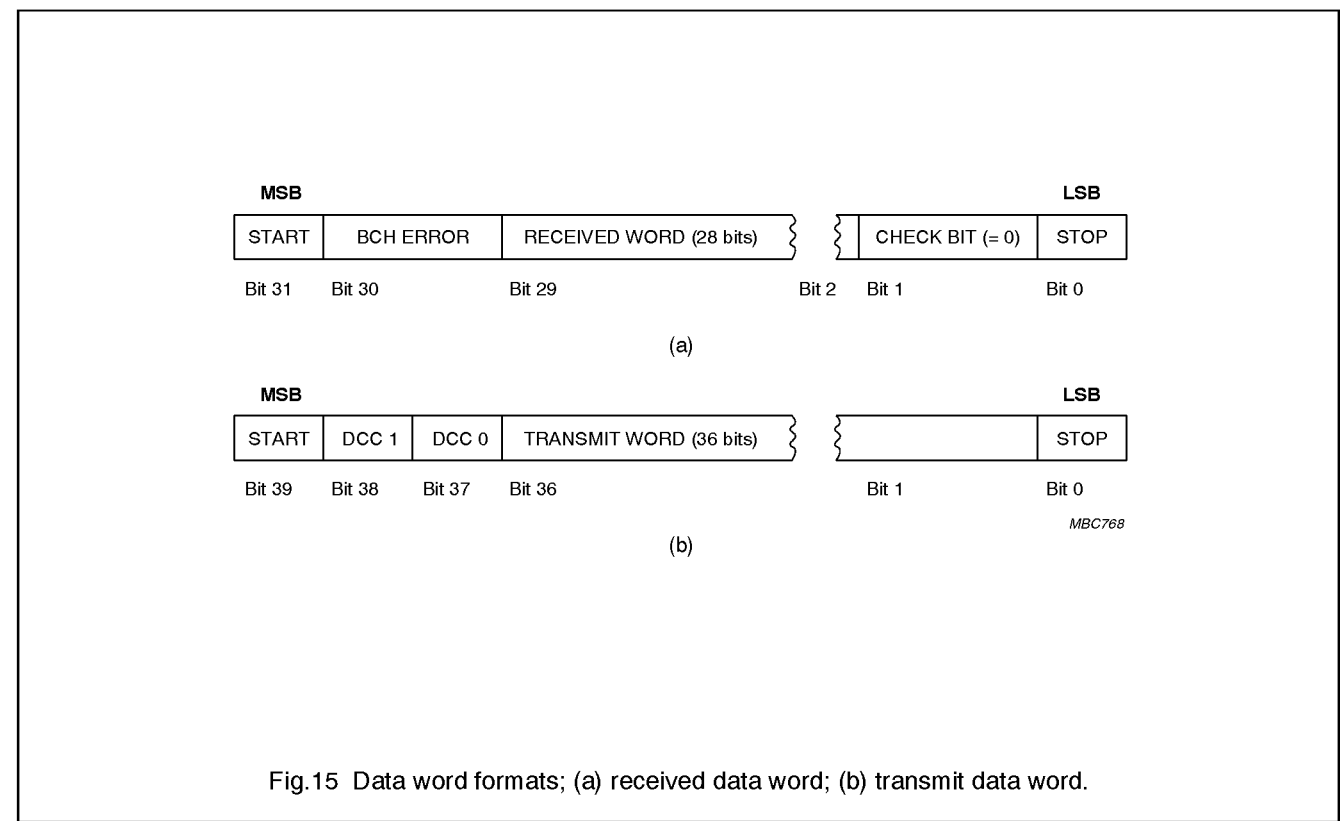
Data processor for cellular radio (DPROC)

UMA1000LT

Table 6 Received Data word

| BIT	TITLE	SENSE	FUNCTION
31	start	LOW	identifies start of word
30	BCH error	active HIGH	indicates that an uncorrected BCH error is associated with the word
29 to 2	received data	binary data	received data word
1	RXLINE error	LOW	if detected as HIGH indicates that a transmission error has occurred on the microprocessor to DPROC serial link
0	stop	HIGH	identifies end of the word

Table 7 Transmit data word

BIT	TITLE	SENSE	FUNCTION
39	start	LOW	identifies start of word
38, 37	DCC	binary data	digital colour code
36 to 1	transmit data	binary data	transmit data word
0	stop	HIGH	identifies end of the word

Fig.15 Data word formats; (a) received data word; (b) transmit data word.

Data processor for cellular radio (DPROC)   UMA1000LT
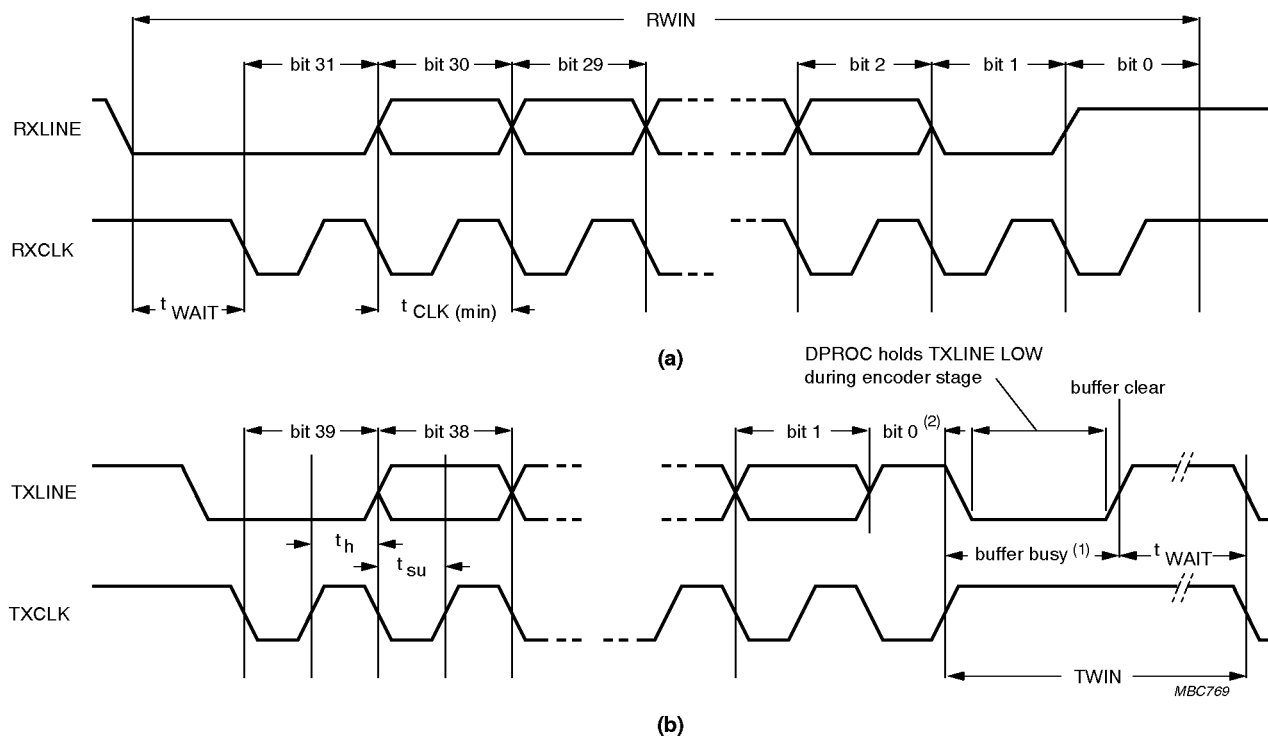
Where:

t_{HD} = 100 ns minimum.

t_{SU} = 0 ns minimum.

t_{WAIT} = 0 ns minimum.

(1) The buffer busy time depends on whether the first or subsequent words are being loaded.

(2) The system controller should monitor the TXLINE during bit 0, if the status of TXLINE does not change from a HIGH to a LOW on the rising edge of TXCLK, then a framing error has occurred. This can be caused by glitches on the clock line or if an arbitration error occurred while the DPROC transmit register was being loaded. The system controller should recover the situation by holding TXLINE HIGH and supplying clocks on TXCLK until TXLINE goes LOW. Then the situation should be treated as a normal channel arbitration failure as described in **Reverse Control Channel Access Arbitration** - Abort Procedure.

Fig.16 Data timing diagrams; (a) DPROC to microcontroller link; receive data timing; (b) microcontroller to DPROC link; transmit data timing.

Data processor for cellular radio (DPROC)

UMA1000LT

BCH and Manchester Encoding Block

The functions performed by this circuit block include:

• reception of data from the System Controller

• parity generation

• message construction

• Manchester encoding.

Each 36-bit Information Word sent on the Reverse Voice and Control Channels is coded into a 48-bit code word. The code word consists of the 36-bit word followed by 12 parity bits. These parity bits are formed by clocking the information word into a 12-bit feedback shift register with characteristic equation:

$$1 + X^3 + X^4 + X^5 + X^8 + X^{10} + X^{12}$$

The BCH Encoder Block constructs the Reverse Voice and Control Channel data streams from the information it receives from the System Controller.
The streams are formed out of the four possible field types:

• Dotting (data inversions)

• 11-bit Synchronization Word

• Digital Colour Code

• 48-bit code word.

The 2 bits of DCC received from the System Controller are coded into a 7-bit word as shown in Table 8.

The data sense for Manchester Encoding has a NRZ logic 1 encoded as a 0-to-1 transition and a NRZ logic 0 encoded as a 1-to-0 transition.

Reverse Control Channel Access Arbitration

The AMPS and TACS specifications require a method of arbitration on the Reverse Control Channel to prevent two mobiles from transmitting on the same channel at the same time. This function is performed by DPROC

monitoring the Busy/Idle stream sent on the Forward Control Channel.

The AMPS and TACS specifications state that once the mobile has commenced transmitting on the Reverse Control Channel it must monitor the Busy/Idle stream. If this stream becomes active outside a predetermined 'window', measured from the start of the transmission of the message, the mobile must terminate its transmission and disable the transmitter immediately.

In the Cellular Radio chip-set there are two levels of control of the RF transmitter; the first is absolute control by the System Controller, the second is conditional by other devices in the set. In DPROC the conditional control of the transmitter is performed via the output TXCTRL. This line is effectively wired ANDed together, using open-drain outputs, with other devices which may wish to control the transmitter. When these devices do not wish to disable the transmitter their output is in a HIGH impedance state.

An exception to this procedure occurs when the Serving System instructs the mobile not to monitor the Busy/Idle bits. In this event the arbitration logic can be disabled by clearing I²C register bit ABREN.

The flow of events during a Control Channel Access attempt is as follows:

INITIAL STATE

• transmitter power off via I²C

• DPROC transmit circuitry in power-up state

• TXCTRL line HIGH.

ACCESS ATTEMPT PROCEDURE

1. System Controller decides to send message (see **Note to the Access Attempt Procedure**).

2. System Controller drives TXCTRL LOW directly.

3. System Controller switches transmitter power-on and waits for power-up for the transmitter module (RF transmitter is still disabled by TXCTRL).

4. System Controller sets TXRST via I²C to DPROC.

5. System Controller sets ABREN via I²C (if required) allowing DPROC to control the transmitter.

6. System Controller determines status of Reverse Control Channel by monitoring the Busy/Idle bit. If busy, waits a random time then tries again.

7. System Controller releases TXCTRL allowing it to be pulled HIGH enabling the transmitter output.

8. System Controller transfers the first word of the message to DPROC via serial link (see **Note to the Access Attempt Procedure**).

9. DPROC sets I²C signal TXIP and starts sending message while monitoring Busy/Idle status.

10. If channel becomes busy before 56 bits and ABREN is set then perform Abort Procedure.

11. If channel remains idle after 104 bits and ABREN is set then perform Abort Procedure.

12. System controller loads the subsequent words of the message into DPROC when the buffer becomes clear (Fig.16b).

13. On completion of entire message DRPCO clears TXIP and 25 ms later the System Controller disables transmitter via I²C.

14. System Controller finally sends TXRST to prepare DPROC for next transmission.

Data processor for cellular radio (DPROC)

UMA1000LT

Note to the Access Attempt Procedure

At stage 1 the system controller may choose to preload DPROC with the first word of the message and hold it from transmission until stage 7 using the TXHOLD line. This gives a lower time overhead between detecting an IDLE channel and commencing the transmission. To use this feature TXHOLD must be driven HIGH before the last bit of data has been transferred into DPROC. Figure 17 illustrates the DPROC data transmission timing.

ABORT PROCEDURE (SEE Fig.18)

1. DPROC immediately disables transmitter output by driving TXCTRL LOW.
2. DPROC sets TXABRT.
3. System Controller detects failure by monitoring TXCTRL and TXABRT.
4. System Controller disables transmitter via RF power amplifier.
5. System Controller sends TXRST to prepare DPROC for next transmission.

Note to the Abort Procedure

If a message is loaded into DPROC after a TXABRT has occurred this word will remain in the DPROC transmit register and will not be cleared to TXRST.

If this situation arises the method of clearing the buffer ready for a second access attempt is to leave TXHOLD LOW and then send a TXRST prior to setting up a new transmission after TXLINE goes HIGH; this will clear any residual data in the buffer.

Signal Tone Generation (ST)

The 8 or 10 kHz (TACS or AMPS) tone generated from the Manchester Encoding Block is used as the Signalling Tone stream.

ANALOG CIRCUIT BLOCKS

General

The analog signal processing functions on DPROC are implemented using switched-capacitor techniques. The main filtering functions are operated at 300 kHz, and these circuits are 'interfaced' to the continuous time and sampled digital domains by distributed RC active filters, passive interpolators and comparators.

The distributed RC sections, the Anti-Alias Filter and the Clock Noise Filter, are non-critical and are designed to tolerate process spreads. The critical filtering in the SAT Filter and the Output Filter, is performed by 300 kHz switched-capacitor circuitry. The Passive Interpolators increase the sampling rate from 300 kHz to 1.2 MHz. The sampled analog signals from the Passive Interpolators are

converted to sampled 2-state digital signals by the Strobed Comparators. The Gated Digital-to-Analog converters and Analog Summer blocks perform resynchronization and sub-sampling of the digitally generated DPROC output signals, and conversion to the sampled analog domain.

These analog section of the device are shown in Fig.1.

Reference Voltage Generator

The Reference Voltage Generator generates the analog ground reference voltage (AGND) used internally within the DPROC device. To minimize noise AGND must be externally decoupled to VSSA as shown in Fig.19.

Anti-Alias Filter

The Anti-Alias Filter is placed before the SAT sampling block to prevent any unwanted signals or high-frequency noise present on the DEMODD pin being aliased into the pass-band by the sampling action of the switched-capacitor filter. To achieve this the Anti-Alias Filter is a continuous time-distributed RC-active low-pass filter.

Table 8 Digital Colour Code; 7-bit word

DCC1	DCC0	Coded DCC						
0	0	0	0	0	0	0	0	0
0	1	0	0	1	1	1	1	1
1	0	1	1	0	0	0	1	1
1	1	1	1	1	1	1	0	0
		DCC1		DCC0		DCC1.EXOR.DCC0		

Data processor for cellular radio (DPROC)
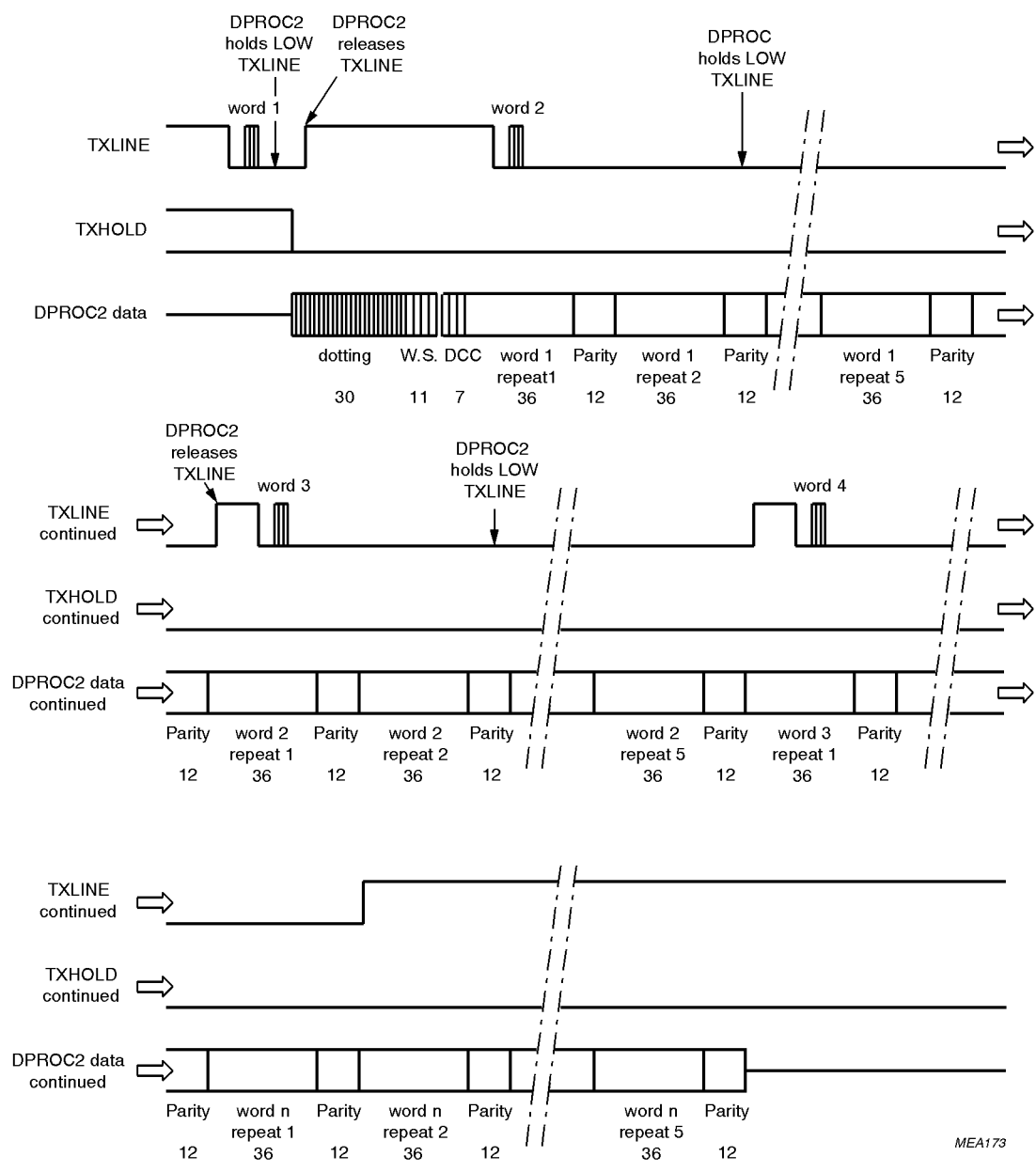
UMA1000LT

Fig.17 DPROC data transmission timing/microcontroller interface.

Data processor for cellular radio (DPROC)

UMA1000LT

SAT Input Filter

The SAT Input Filter is a switched-capacitor filter which provides band-pass filtering of the SAT signals from the DEMODD pin to improve the SAT signal-to-noise ratio prior to recovery and transponding.

Passive Interpolator

The function of the Passive Interpolator is to increase the sampling rate at the output of the switched-capacitor filters. This reduces the coarseness of the zero-crossing information which would otherwise cause unacceptable isochronous distortion in the recovered signal.

Strobed Comparators

The Strobed Comparators form the analog-to-digital interface for the received data and SAT signals from the DEMODD pin. These comparators act as limiting amplifiers which convert the filtered sampled analog signals into 2-state sampled digital signals containing only the zero-crossing information from the analog signal.

Gated Digital-to-Analog and Analog Summer

The Gated Digital-to-Analog converters and Analog Summer form the interface between the digital and analog circuitry on the transmit path of DPROC. It is at this point that the three sampled digital signals, containing SAT, ST and encoded digital data, are combined to form a composite signal.

The data streams are enabled by the I^2C signals STEN, SATEN and the internal signal DATAEN respectively (DATAEN disables SAT and ST when data is being transmitted). The digital-to-analog conversion and sub-sampling operation is performed by the Gated Digital-to-Analog converters and Analog Summer. The relative signal weights applied in the summer (with respect to the data path) are shown in Table 9.

Output Filter

The Output Filter is a switched-capacitor filter which performs band-limiting of the DPROC output signals in accordance with the AMPS and TACS specifications. The required below band roll-off is achieved via external AC coupling from the DATA pin.

Clock Noise Filter

The filter is a non-critical continuous time-distributed RC-active low-pass filter used to remove any switching transient residues from the output signal.

Table 9 Relative signal weights

SIGNAL	RELATIVE OUTPUT LEVEL AMPS AND TACS
ST	1.0
SAT	0.25
DATA	1.0

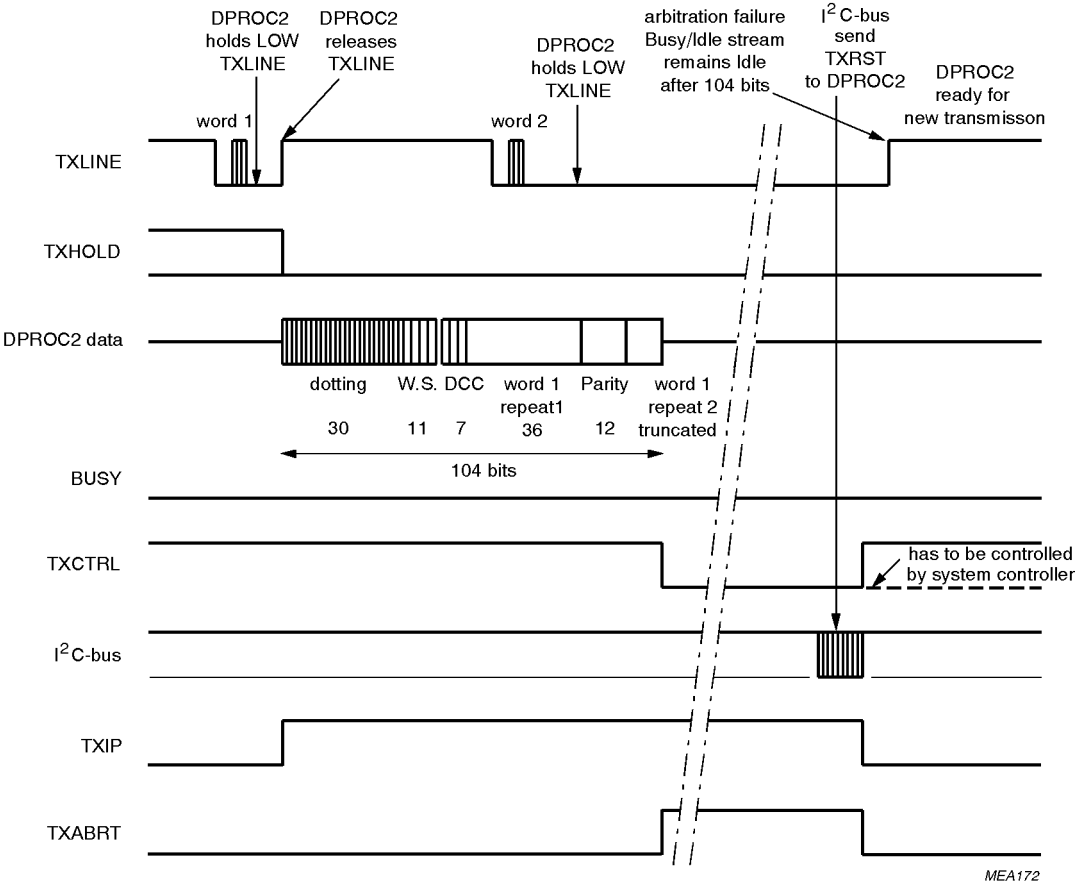## Data processor for cellular radio (DPROC)

Fig.18 DPROC data transmission timing/microcontroller interface during arbitration failure.

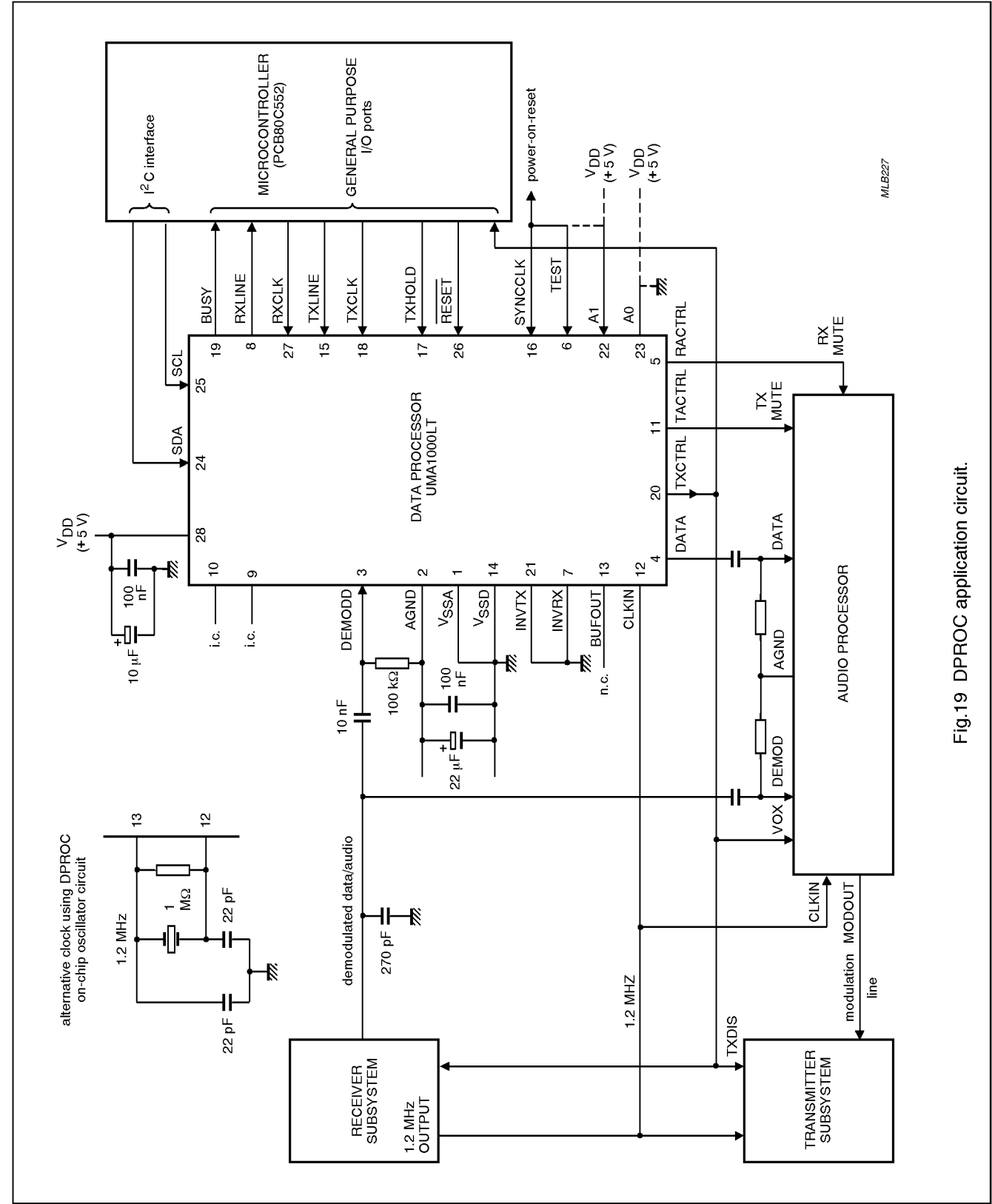# Data processor for cellular radio (DPROC)

UMA1000LT

APPLICATION INFORMATION

Fig.19 DPROC application circuit.