DATA SHEET

UDA1321
Universal Serial Bus (USB) Digital-to-Analog Converter (DAC)

Preliminary specification
File under Integrated Circuits, IC01

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Philips Semiconductors

PHILIPS

Universal Serial Bus (USB) Digital-to-Analog Converter (DAC)

UDA1321

FEATURES

General

- Complete stereo USB-DAC system with integrated filtering and line output drivers
- Supports USB-compliant audio multimedia devices over an industry standard USB-compatible 4-wire cable
- Supports 12 Mbits/s 'full speed' serial data transmission
- Fully automatic 'Plug-and-Play' operation
- Supports multiple audio data formats
- 3.3 V power supply
- Low power consumption
- Efficient power management mode
- On-chip master clock oscillator, only an external crystal is required
- High linearity
- Wide dynamic range
- Superior signal-to-noise ratio
- Low total harmonic distortion
- Easy application and inexpensive to implement
- Partly programmable USB descriptors via EEROM
- 28 lead Small Outline package (SO28) or 32 Shrink Dual Inline package (SDIP32).

Sound processing

- Separate digital volume control for left and right channel
- Soft mute
- Digital bass and treble tone control
- External Digital Sound Processor (DSP) option possible via standard I^2S or Japanese digital I/O-format
- Selectable clipping prevention
- Selectable Dynamic Bass Boost (DBB)
- On-chip digital de-emphasis.

Document references

- *"USB Specification"*, release 1.0
- *"USB Device Class Definition for Audio Devices"*, release 0.9
- *"Device Class Definition for Human Interface Devices (HID)"*, release 1.0 draft 4
- *"USB HID Usage Table",* release 0.7f.

GENERAL DESCRIPTION

The UDA1321 is a stereo CMOS digital-to-analog bitstream converter designed for USB-compliant audio devices and multimedia audio applications. The UDA1321 is an adaptive asynchronous sink USB audio device with a continuous sampling frequency range from 5 to 55 kHz. It contains a USB-interface, an embedded micro controller and an Asynchronous Digital-to-Analog Converter (ADAC).

The USB-interface is the interface between the USB, the ADAC and the microcontroller. The USB-interface consists of an analog front-end and a USB-processor. The analog front-end transforms the differential USB-data to a digital data stream. The USB-processor buffers incoming and outgoing data from the analog front-end and handles all low level USB protocols. The USB-processor selects the relevant data from the bus, performs an extensive error detection and separates control information (in- and out-going) and audio information (in-going only). The control information is made accessible to the microcontroller. The audio information becomes available at the digital I/O-output or is fed directly to the ADAC.

The microcontroller handles the high level USB protocols, translates the incoming control requests and takes care of the user interface, through general purpose pins, and an I^2C port.

The ADAC enables the wide and continuous range of input sampling frequencies. By means of a Sample Frequency Generator (SFG), the ADAC is able to reconstruct the average sample frequency from the incoming audio samples. Furthermore the ADAC performs the sound processing. The ADAC consists of a FIFO, an unique audio feature processing DSP, the SFG, digital upsample filters, a variable hold register, a Noise Shaper (NS) and a Filter Stream DAC (FSDAC) with integrated filter and line output drivers. The audio information is applied to the ADAC via the USB-processor or via the digital I/O-input.

Via the digital I/O-bus an external DSP can be used for adding extra sound processing features.

The UDA1321 supports the standard I^2S-bus data input format and the LSB justified serial data input format with word lengths of 16, 18 and 20 bits.

Universal Serial Bus (USB) Digital-to-Analog Converter (DAC)

UDA1321

The wide dynamic range of the bitstream conversion technique used in the UDA1321 guarantees a high audio sound quality.

APPLICATIONS

- USB monitors
- USB speakers
- USB headsets
- USB telephone/answering machines
- USB links in consumer audio devices.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power supplies						
V_{DD}	supply voltage	note 1	3.0	3.3	3.6	V
I_{DD}	supply current		–	50		mA
$I_{DD(ps)}$	supply current (power-saving mode)		–	18	–	mA
Dynamic performance DAC						
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	f_s = 44.1 kHz; R_L = 5 kΩ				
		at input signal of 1 kHz (0 dB)	–	–85	–80	dB
			–	0.0056	0.01	%
		at input signal of 1 kHz (–60 dB)	–	–30	–20	dB
			–	3.2	10.0	%
S/N	signal-to-noise ratio at bipolar zero	A-weighted at code 0000H	90	95	–	dBA
$V_{FS(o)(rms)}$	full-scale output voltage (RMS value)	V_{DD} = 3.3 V	–	0.66	–	V
General characteristics						
$f_{i(sample)}$	audio sample input frequency		5	–	55	kHz
T_{amb}	operating ambient temperature		0	25	70	°C

Note

1. All V_{DD} and V_{SS} pins must be connected to the same supply or ground respectively.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UDA1321T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
UDA1321	SDIP32	plastic shrink dual in-line package; 32 leads (400 mil)	SOT232-1

BLOCK DIAGRAM

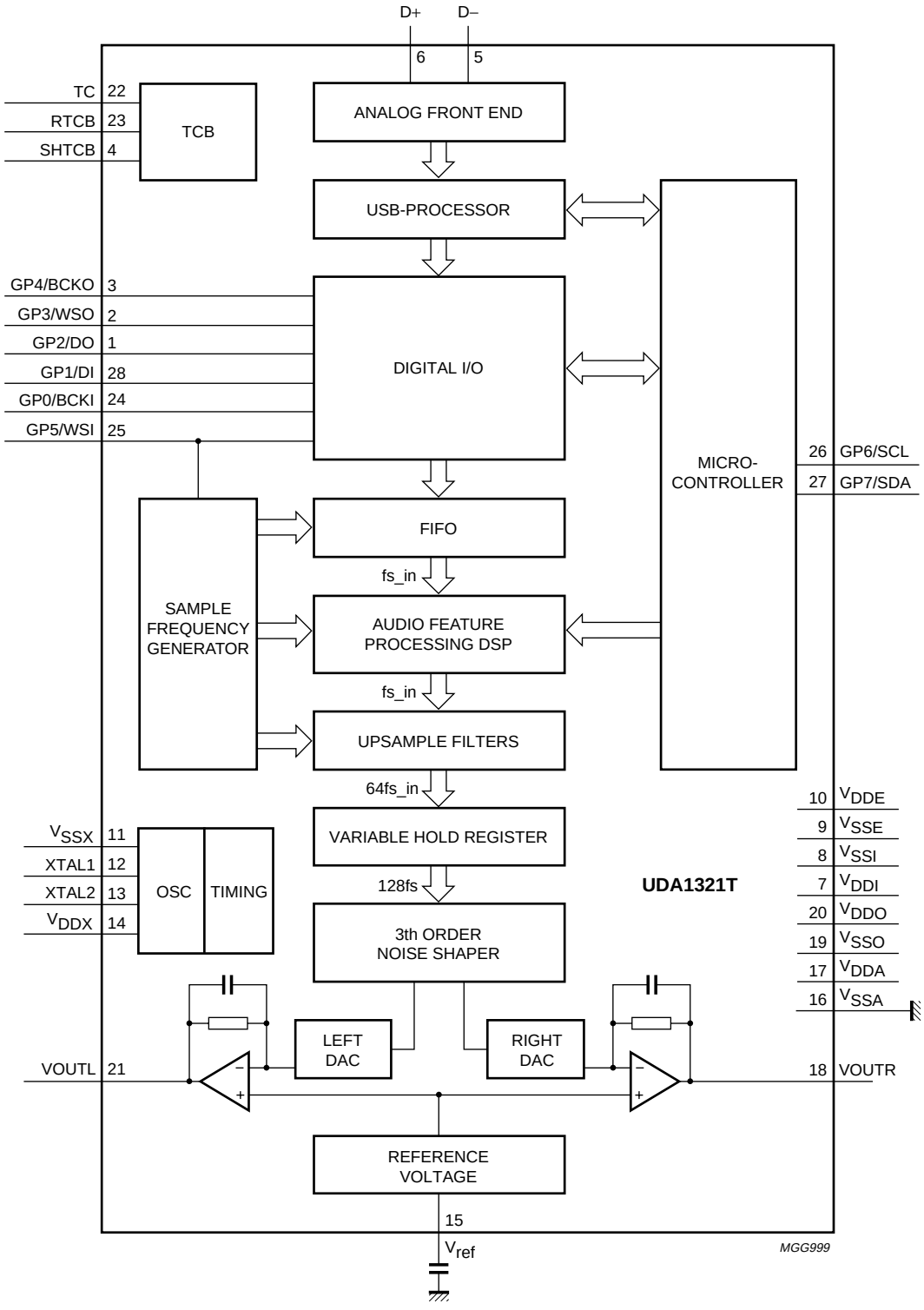


Fig.1 Block diagram SO28 pinning.

PINNING

SYMBOL	PIN SDIP32	PIN SO28	I/O	DESCRIPTION
GP2/DO	1	1	I/O	general purpose pin/data output pin for extra DSP chip (digital)
GP3/WSO	2	2	I/O	general purpose pin/master word select output pin for extra DSP chip (digital)
GP4/BCKO	3	3	I/O	general purpose pin/master bit clock output pin for extra DSP chip (digital)
SHTCB	4	4	I	shift clock TCB (active HIGH; digital)
	5		–	n.c.
D–	6	5	I/O	negative data line of the differential data bus conforming to the USB-standard (analog)
D+	7	6	I/O	positive data line of the differential data bus conforming to the USB-standard (analog)
V_{DDI}	8	7	–	digital supply digital core
V_{SSI}	9	8	–	digital ground core
V_{SSE}	10	9	–	digital ground I/O pads
V_{DDE}	11	10	–	digital supply I/O pads
	12		–	n.c.
V_{SSX}	13	11	–	crystal oscillator ground
XTAL1	14	12	I	crystal connection (analog)
XTAL2	15	13	O	crystal connection (analog)
V_{DDX}	16	14	–	supply crystal oscillator
	17		–	n.c.
V_{ref}	18	15	I	V_{ref} output pin (analog)
V_{SSA}	19	16	–	analog ground
V_{DDA}	20	17	–	analog supply
VOUTR	21	18	O	voltage output pin right channel (analog)
V_{SSO}	22	19	–	opamp ground
V_{DDO}	23	20	–	opamp supply
VOUTL	24	21	O	voltage output pin left channel (analog)
TC	25	22	I	test control pin (active HIGH; analog)
RTCB	26	23	I	asynchronous reset TCB (active HIGH; digital)
GP0/BCKI	27	24	I/O	general purpose pin (digital)
	28		–	n.c.
GP5/WSI	29	25	I/O	general purpose pin (digital)
GP6/SCL	30	26	I/O	general purpose pin/clock line I^2C-bus (digital)
GP7/SDA	31	27	I/O	general purpose pin/data line I^2C-bus (digital)
GP1/DI	32	28	I/O	general purpose pin/data input pin from extra DSP chip (digital)

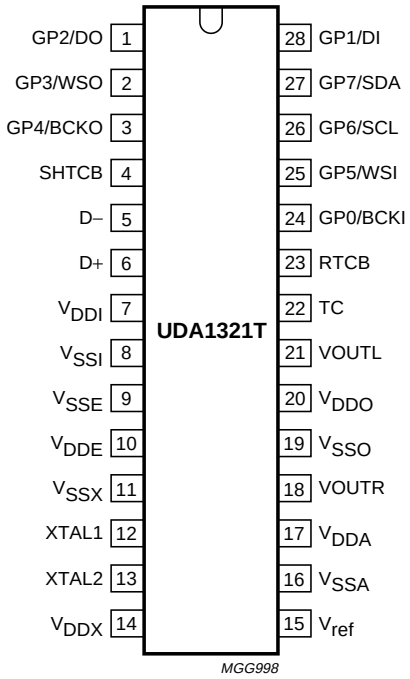


Fig.2 Pin configuration SO28.

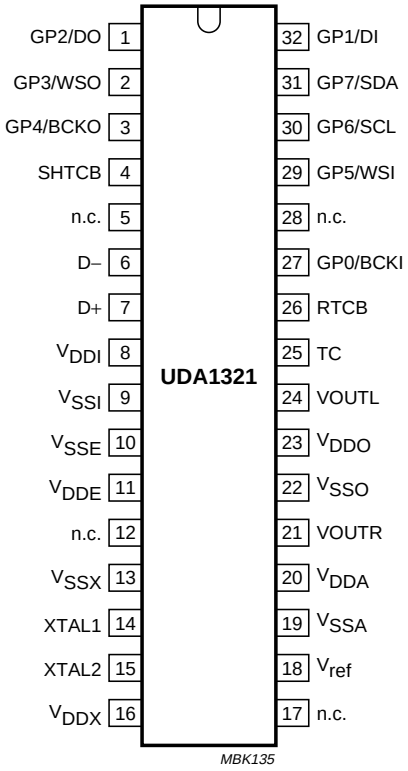


Fig.3 Pin configuration SDIP32.

FUNCTIONAL DESCRIPTION

The Universal Serial Bus (USB)

Data and power is transferred via the USB over a 4-wire cable.
The signalling occurs over two wires and point-to-point segments. The signals on each segment are differentially driven into a cable of 90 Ω intrinsic impedance.
The differential receiver features input sensitivity of at least 200 mV and sufficient common mode rejection.

The analog front-end

The analog front-end is an on-chip generic USB transceiver.
It is designed to allow voltage levels up to V_{DD} from standard or programmable logic to interface with the physical layer of the USB. It is capable of receiving and transmitting serial data at full speed (12 Mbits/s).

The analog front-end can be switched in power saving mode.

The USB-processor

The USB-processor forms the interface between the analog front-end, the ADAC and the microcontroller.
The USB-processor consists of:

- The Philips Serial Interface Engine (PSIE)
- The Memory Management Unit (MMU)
- The Audio Sample Redistribution (ASR) module.

The Philips Serial Interface Engine and Memory Management Unit (PSIE_MMU)

The PSIE_MMU translates the electrical USB signals into bytes and signals. Depending upon the device USB address and the USB endpoint address, the USB data is directed to the correct endpoint buffer on the PSIE_MMU interface. The data transfer could be of bulk, isochronous, control or interrupt type. The device USB address is configured during the enumeration process. The UDA1321 has three endpoints. These are:

- Control Endpoint 0
- Status Interrupt Endpoint
- Isochronous Data Sink Endpoint

The amount of bytes/packet on the control endpoint is limited by the PSIE_MMU hardware to 8 bytes/packet.

The PSIE is the digital front-end of the USB-processor. This module recovers the 12 MHz USB-clock, detects the USB sync-word and handles all low-level USB protocols and error checking.

The MMU is the digital back-end of the USB-processor. It handles the temporary data storage of all USB packets that are received or sent over the bus. On the USB, three types of packets are defined. These are:

- Token packets
- Data packets
- Handshake packets.

The token packet contains information about the destination of the data packet. The audio data is transferred via an isochronous data sink endpoint and as a consequence no handshaking mechanism is used. The MMU also generates a 1 kHz clock that is locked to the USB Start-Of-Frame (SOF) token.

The Audio Sample Redistributor (ASR)

The ASR reads the audio samples from the MMU and distributes these samples equidistant over a 1 ms frame period. The distributed audio samples are translated by the digital I/O module to I^2S or Japanese digital I/O-format. The ASR generates the bit clock and the word select signal of the digital I/O. The digital I/O-formats the received audio samples to one of the four specified serial digital audio formats (I^2S, 16, 18 or 20 bits LSB-justified).

The microcontroller

The microcontroller receives the control information selected from the USB by the USB-processor. It handles the high level USB protocols and the user interfaces.

The major task of the software process, that is mapped upon the microcontroller, is to control the different modules of the UDA1321 in such a way that it behaves as a USB device.

Therefore the microcontroller:

- interprets the USB requests and maps them upon the UDA1321 application
- controls the internal operation of the UDA1321, the digital I/O-pins and the GP I/O-pins
- communicates with the external world (EEROM) using I^2C-bus facility and the GP I/O-pins.

The Asynchronous Digital-to-Analog Converter (ADAC)

The ADAC receives USB audio information from the USB-processor or from the digital I/O-bus. The ADAC is able to reconstruct the sample clock from the rate at which the audio samples arrive and takes care of the audio sound processing. After the processing, the audio signal is upsampled, noise-shaped and converted to analog output voltages capable of driving a line output. The ADAC consists of:

- A Sample Frequency Generator (SFG)
- FIFO registers
- An audio feature processing DSP
- Two digital upsample filters and a variable hold register
- A digital Noise Shaper (NS)
- A Filter Stream DAC (FSDAC) with integrated filter and line output drivers.

The Sample Frequency Generator (SFG)

The SFG controls the timing signals for the asynchronous D/A conversion. By means of a digital PLL, the SFG automatically recovers the applied sampling frequency and generates the accurate timing signals for the audio feature processing DSP and the upsample filters.

First In First Out (FIFO) registers

The FIFO registers are used to store the audio samples temporarily coming from the USB-processor or from the digital I/O-input. The use of a FIFO (in conjunction with the SFG) is necessary to remove all jitter present on the incoming audio signal.

The audio feature processing DSP

A DSP processes the sound features.
The control and mapping of the sound features is explained in Section “Controlling the USB-DAC”.
Depending on the sampling rate f_s the DSP knows four frequency domains in which the treble and bass are regulated. The domain is chosen automatically.

Table 1 Frequency domains for audio processing

DOMAIN	SAMPLE FREQUENCY
1	5..12 kHz
2	12..25 kHz
3	25..40 kHz
4	40.. 55 kHz

The upsample filters and variable hold function

After the audio feature processing DSP two upsample filters and a variable hold function increase the oversampling rate to $128f_s$.

The noise shaper

A third order noise shaper converts the oversampled data to a noise-shaped bitstream for the FSDAC. The in-band quantization noise is shifted to frequencies well above the audio band.

The Filter Stream DAC (FSDAC)

The FSDAC is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to an analog output voltage. The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier. In this way very high signal-to-noise performance and low clock jitter sensitivity is achieved. A postfilter is not needed because of the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output.

USB-DAC descriptors

In a typical USB environment the PC has to know which kind of devices are connected to its USB-bus. For this purpose each device contains a number of USB descriptors. These descriptors describe, from different points of view (USB-configuration, USB-interface and USB-endpoint), the capabilities of a device. Each of them can be requested by the host. The collection of descriptors is denoted as a descriptor map. This descriptor map will be reported to the USB host during enumeration.

The USB descriptors and their most important fields, in relationship to the characteristics of the UDA1321 are shortly explained below.

General descriptors

The UDA1321 supports one configuration containing a control interface, an audio interface and a HID interface. The descriptor map that describes this configuration is partly fixed and partly programmable.

The programmable part can be retrieved from one out of four internal configuration maps or from an I^2C EEROM. At start-up time one out of four internal configuration maps can be selected depending on the logical combination of GP3 and GP0. It is possible to overwrite this configuration map with a configuration map loaded from an I^2C EEROM.

The descriptors of the descriptor map as mentioned above are described in Tables 2 and 3. The programmable descriptors are marked with a star. The given values are examples used in Philips applications.

Table 2 Standard Device Descriptor and Configurations.

DEVICE DESCRIPTOR	VALUE HEX
bLength	12
bDescriptorType	01
bcdUSB	0001
cDeviceClass	00
cDeviceSubClass	00
cDeviceProtocol	00
bMaxPacketSize0	08
idVendor	7104*
idProduct	0101*
bcdDevice	0001
iManufactor	01
iProduct	02
iSerialNumber	03
bNumConfigurations	01

Table 3 Configuration Descriptor and Interfaces.

CONFIGURATION DESCRIPTOR	VALUE HEX
bLength	09
bDescriptortype	02
wTotalLength	tbf
bNumInterfaces	03
bConfigurationValue	01
iConfiguration	00
bmAttributes	40*
MaxPower	0*

Audio device class specific descriptors

The Audio Device Class is partly specified with Standard Descriptors and partly with Specific Audio Device Class Descriptors. The Standard Descriptors specify the number and the type of the interface or endpoint. The UDA1321 supports 7 different audio modes:

- 8-bit PCM mono or stereo audio data
- 16-bit PCM mono or stereo audio data
- 24-bit PCM mono or stereo audio data.
- Zero bandwidth mode.

Each mode is defined as an alternate setting of the audio interface, selectable with the standard audio streaming interface descriptor **bAlternateSetting** field; see Table 4.

Within the audio interface, an isochronous sink endpoint is defined.

Table 4 Standard Audio Control Interface Descriptor.

DESCRIPTOR	VALUE HEX
bLength	0B
bDescriptortype	04
bInterfaceNumber	00
bAlternateSetting	00
bNumEndpoints	00
bInterfaceClass	01
bInterfaceSubClass	01
bInterfaceProtocol	00
iInterface	00
wNumClasses	0100

The seven alternate settings are described in more detail by the Specific Audio Device Class Descriptors. For example, support of different sound features, such as Volume, Treble, Bass, Mute etc.

Table 5 Class Specific Audio Control Interface Descriptor Header.

DESCRIPTOR	VALUE HEX
bLength	09
bDescriptortype	24
bDescriptorSubtype	01
bcdADC	0900
wTotalLength	2B00
bInCollection	01
baInterfaceNr(1)	01

The UDA1321 supports the Input Terminal, Output Terminal and the Feature Unit Descriptors.

The Input and Output Terminals are not controllable via USB. The Feature Unit provides the basic manipulation of the incoming logical channels. The supported sound features are: Volume control, Mute control, Treble control Bass control and Bass Boost control.

Table 6 Class Specific Input Terminal Descriptor.

DESCRIPTOR	VALUE HEX
bLength	0C
bDescriptortype	24
bDescriptorSubtype	02
bTerminalID	01
wTerminalType	0101
bAssocTerminal	00
bNrChannels	02
wChannelConfig	0300
iChannelNames	00
iTerminal	00

Table 7 Class Specific Feature Unit Descriptor.

DESCRIPTOR	VALUE HEX
bLength	0D
bDescriptortype	24
bDescriptorSubtype	06
bUnitID	02
bSourceID	01
bControlSize	02
bmaControls(0)	1501*
bmaControls(1)	0200
bmaControls(2)	0200
iFeature	00

Table 8 Class Specific Output Terminal Descriptor.

DESCRIPTOR	VALUE HEX
bLength	09
bDescriptortype	24
bDescriptorSubtype	03
bTerminalID	03
wTerminalType	0103*
bAssocTerminal	00
bSourceID	02
iTerminal	00

The maximum number of audio data samples within an USB packet arriving on the isochronous sink endpoint is restricted by the buffer capacity of this isochronous endpoint. The maximum buffer capacity is 336 bytes/ms.

For each alternate setting with audio, a maximum bandwidth is claimed as indicated in the Standard Isochronous Audio Data Endpoint Descriptor **wMaxPacketSize** field. To allow a small overshoot in the number of audio samples per packet, the top sample frequency of 55 kHz is taken in the calculation of the bandwidth for each alternate setting.
For each alternate setting, with its own Isochronous Audio Data Endpoint Descriptor, **wMaxPacketSize** field is then defined as described in Table 9.

Table 9 Audio bandwidth at each audio mode.

AUDIO MODE	wMaxPacketSize
8-bit PCM, mono	56 ($^{8}/_{8} \times 1 \times 56$)
8-bit PCM, stereo	112 ($^{8}/_{8} \times 2 \times 56$)
16-bit PCM, mono	112 ($^{16}/_{8} \times 1 \times 56$)
16-bit PCM, stereo	224 ($^{16}/_{8} \times 2 \times 56$)
24-bit PCM, mono	168 ($^{24}/_{8} \times 1 \times 56$)
24-bit PCM, stereo	336 ($^{24}/_{8} \times 2 \times 56$)

The Standard Audio Streaming Interface Descriptor and the Standard Isochronous Audio Data Endpoint Descriptor are given below.

Table 10 Standard Audio Streaming Interface Descriptor fields for alternate setting 0.

DESCRIPTOR	VALUE HEX
bLength	0B
bDescriptortype	04
bInterfaceNumber	01
bAlternateSetting	00
bNumEndpoints	00
bInterfaceClass	01
bInterfaceSubClass	02
bInterfaceProtocol	00
iInterface	00
wNumClasses	0100

Table 11 Standard Audio Streaming Interface Descriptor fields for alternate setting 1 to 6.

DESCRIPTOR	VALUE HEX
bLength	0B
bDescriptortype	04
bInterfaceNumber	01
bAlternateSetting	01, 02, 03, 04, 05, 06
bNumEndpoints	01
bInterfaceClass	01
bInterfaceSubClass	02
bInterfaceProtocol	00
iInterface	00
wNumClasses	0100

Table 12 Class Specific Audio Streaming Interface General Descriptor for alternate setting 1 to 6.

DESCRIPTOR	VALUE HEX
bLength	07
bDescriptortype	24
bDescriptorSubtype	01
bTerminalLink	01
bDelay	00
wFormatTag	0100

Although in this specific UDA1321 application no endpoint control properties can be used upon the isochronous adaptive sink endpoint, the descriptors are still necessary to inform the host about the definition of this endpoint: isochronous, adaptive, sink, continuous sampling frequency (at input side of this endpoint) with lower bound of 5 kHz and upper bound of 55 kHz. These characteristics are defined in Table 13.

Table 13 Class Specific Audio Streaming Interface Format Type I Descriptor Continuous Sampling Frequency for alternate setting 1 to 6.

DESCRIPTOR	VALUE HEX
bLength	0E
bDescriptortype	24
bDescriptorSubtype	02
bFormatType	01
bNrChannels	depends on audio mode
bSubframeSize	depends on audio mode
bBitResolution	depends on audio mode
bSamFreqType	00
tLowerSamFreq	7E 13 00
tUpperSamFreq	E2 D6 00

Notice the **tLowerSamFreq** and **tUpperSamFreq** fields are defined in little Endian order (LSB first).
The Audio Class Specific Descriptors can be requested with the ‘Get Descriptor: Configuration request’, which returns all the descriptors, except the Device Descriptor.

Table 14 **bNrChannels, bSubframeSize** and **bBitResolution** Descriptor fields for audio mode 8 bit-PCM mono.

DESCRIPTOR	VALUE HEX
bNrChannels	01
bSubframeSize	01
bBitResolution	08

Table 15 **bNrChannels, bSubframeSize** and **bBitResolution** Descriptor fields for audio mode 8 bit-PCM stereo.

DESCRIPTOR	VALUE HEX
bNrChannels	02
bSubframeSize	01
bBitResolution	08

Table 16 **bNrChannels, bSubframeSize** and **bBitResolution** Descriptor fields for audio mode 16 bit-PCM mono.

DESCRIPTOR	VALUE HEX
bNrChannels	01
bSubframeSize	02
bBitResolution	10

Table 17 **bNrChannels, bSubframeSize** and **bBitResolution** Descriptor fields for audio mode 16 bit-PCM stereo.

DESCRIPTOR	VALUE HEX
bNrChannels	02
bSubframeSize	02
bBitResolution	10

Table 18 **bNrChannels, bSubframeSize** and **bBitResolution** Descriptor fields for audio mode 24 bit-PCM mono.

DESCRIPTOR	VALUE HEX
bNrChannels	01
bSubframeSize	03
bBitResolution	14

Table 19 **bNrChannels, bSubframeSize** and **bBitResolution** Descriptor fields for audio mode 24 bit-PCM stereo.

DESCRIPTOR	VALUE HEX
bNrChannels	02
bSubframeSize	03
bBitResolution	14

Table 20 Standard Isochronous Audio Data Endpoint Descriptor included for alternate setting 1 to 6.

DESCRIPTOR	VALUE HEX
bLength	09
bDescriptortype	05
bEndpointAddress	04
bmAttributes	09
wMaxPacketSize	depends on audio mode; see Table 9
bInterval	01
bRefresh	00
bSynchAddress	00

Table 21 Class Specific Isochronous Audio Data Endpoint Descriptor included for alternate setting 1 to 6.

DESCRIPTOR	VALUE HEX
bLength	07
bDescriptortype	25
bDescriptorSubtype	01
bmAttributes	00
bLockDelayUnits	02
bLockDelay	0002

HUMAN INTERFACE DEVICE SPECIFIC DESCRIPTORS

The inputs defined on the UDA1321 are transmitted via the USB to the host according to the HID Class. The host responds with the appropriate settings via the Audio Device Class for the Audio related parts or via the HID Class for the HID related in- and outputs of the UDA1321.

A HID descriptor is necessary to inform the host about the conception of the User Interface. The host communicates via the HID device driver using either the control pipe or the interrupt pipe. The UDA1321 is using USB endpoint 0 (control pipe) to respond to the HID specific 'Get/Set Report request' to receive/transmit data from/to the UDA1321. The UDA1321 is using USB endpoint 3 as interrupt pipe for polling asynchronous data.

The UDA1321 is a high-speed device. The maximum transaction size is 64 bytes per USB frame and the polling rate is defined at a maximum of every one millisecond.

The host requests the configuration Descriptor which includes the Standard Interface Descriptor, the HID Endpoint Descriptor and the HID Descriptor. Then the HID Device driver of the host requests the Report Descriptor.

Report descriptors are composed of pieces of information about the device. Each piece of information is called an item. All items have a one-byte prefix that contains the item tag, type and size. In the UDA1321 only the short item basic type is used.

The hosts HID device driver will parse the report descriptor and the defined items. By examining all of these items, the HID class driver is able to determine the size and composition of data reports from the device.

The main items of the UDA1321 are input and output reports. Input reports are sent via the interrupt pipe (UDA1321 USB address 3). Input and output reports can be requested by the host via the control endpoint (USB address 0).

In Tables 22 to24 some of the Standard Interface Descriptor fields and HID Descriptors are defined.

Table 22 Standard Interface Descriptor.

DESCRIPTOR	VALUE HEX
bLength	09
bDescriptortype	04
bInterfaceNumber	02
bAlternateSetting	00
bNumEndpoints	01
bInterfaceClass	03
bInterfaceSubClass	00
bInterfaceProtocol	00
iInterface	00

Table 23 HID Endpoint Descriptor

DESCRIPTOR	VALUE HEX
bLength	07
bDescriptortype	05
bEndpointAddress	83
bmAttributes	03
wMaxPacketSize	0100
bInterval	0A

Table 24 HID Descriptor.

DESCRIPTOR	VALUE HEX
bLength	09
bDescriptorType	21
bcdHID	0401
bCountryCode	00
bNumDescriptorsAvailable	01
bDescriptorType	22
bDescriptorLength	3300

The UDA1321 supports a maximum of three pushbuttons, which are representing a certain feature of the UDA1321.

If pressed by the user the pushbutton will go to its 'ON' state, if not pressed the pushbutton will go back to its 'OFF' state.

The UDA1321 only supports a maximum of two outputs for e.g. user LEDs.

For more information about the input and output functions of the UDA1321 see the application documentation of the device.

Controlling the USB-DAC

The sound features as defined in the *"USB Device Class Definition for Audio Devices"* are mapped on the UDA1321 specific feature registers by the microcontroller. These specific sound features are:

- Volume control (separate for left and right stereo channels, no master channel)
- Mute control (only master channel)
- Treble control (only master channel)
- Bass control (only master channel)
- Dynamic Bass Boost control (only master channel)

These specific features can be activated via the host (Audio Device Class requests) or via the GP I/O-pins (HID plus Audio Device Class requests). Via the I^2C-bus the user is able to download the necessary configuration data for different applications (definition of the function of the GP- pins, with or without digital I/O functionality etc.). The mapping and control of the standard USB audio features and UDA1321 specific features is described below.

Volume control

Volume control is possible via the host or via predefined GP I/O-pins. The setting of 0 dB is always referenced to the maximum available volume setting. Table 25 gives the mapping of **wVolume** value **(**as defined in the *"USB Device Class Definition for Audio Devices"*) upon the actual Volume setting of the USB-DAC. In case of using the UDA1321, the range is 0 dB downto -60 dB in steps of 1 dB and -∞ dB. Undependable control of 'left'/'right' Volume is possible. Notice **wVolume**$_{LSB}$ $b_7..b_0$ are not used. Values above 0 dB are returned as 0 dB. The volume value at start up of the device is defined in the selected configuration map.

Balance control is possible via the separate volume control option of both channels. Therefore the characteristics of the balance control are equal to the volume control characteristics.

Table 25 Volume control characteristics.

wVOLUME (MSB)								VOLUME USB SIDE	VOLUME USB-DAC	UNIT
B15	B14	B13	B12	B11	B10	B9	B8			
0	0	0	0	0	0	0	0	0	0	dB
1	1	1	1	1	1	1	1	0	0	dB
1	1	1	1	1	1	1	0	-1	-1	dB
1	1	1	1	1	1	0	1	-2	-2	dB
1	1	1	1	1	1	0	0	-3	-3	dB
1	1	1	1	1	0	1	1	-4	-4	dB
1	1	1	1	1	0	1	0	-5	-5	dB
1	1	1	1	1	0	0	1	-6	-6	dB
1	1	1	1	1	0	0	0	-7	-7	dB
1	1	1	1	0	1	1	1	-8	-8	dB
1	1	1	1	0	1	1	0	-9	-9	dB
...	...	...	...	...	...	...	...	...	...	...
1	1	0	0	0	1	0	1	-58	-58	dB
1	1	0	0	0	1	0	0	-59	-59	dB
1	1	0	0	0	0	1	1	-60	-60	dB
1	1	1	0	0	0	1	0	-61	−∞	dB
1	1	1	0	0	0	0	1	-62	−∞	dB
...	...	...	...	...	...	...	...	...	...	...
1	0	0	0	0	0	0	0	−∞	−∞	dB

Mute control

Mute is one of the sound features as defined in the *"USB Device Class Definition for Audio Devices"*. The mute control request data **bMute** controls the position of the mute switch. The position can be either on or off. When **bMute** is true the feature unit is muted. When **bMute** is false the feature unit is not muted.

When the mute is active for the master channel, the value of the sample is decreased smoothly to zero following a raised cosine curve. There are 32 coefficients used to step down the value of the data, each one being used 32 times before stepping to the next. This amounts to a mute transition of 23 ms at f_s = 44.1 kHz. When the mute is released, the samples are returned to the full level again following a raised cosine curve with the same coefficients being used in reversed order. The mute, on the master channel is synchronized to the sample clock, so that operation always takes place on complete samples.

A mute can be given via the host or by pressing a predefined GP pin.

Treble control

The Treble control is available for the master channel of the UDA1321. Treble can be regulated in three modes: minimum, flat and maximum mode. The preferred mode is selected at start-up of the device (configuration map). The corner frequency is 3000 Hz for the minimum mode and 1500 Hz for the maximum mode. The treble range is from 0 dB up to 6 dB in steps of 2 dB. Notice that the negative treble values as defined in the *"USB Device Class Definition for Audio Devices"* are not supported by the UDA1321; the 0 dB value is returned as 0 dB. Table 26 gives the mapping of the **bTreble** value upon the actual Treble setting of the USB-DAC.

Table 26 Treble control characteristics.

bTREBLE								TREBLE USB SIDE	TREBLE USB-DAC			UNIT
B7	B6	B5	B4	B3	B2	B1	B0		minimum	flat	maximum	
0	0	0	0	0	0	0	0	0.00	0	0	0	dB
0	0	0	0	0	0	0	1	0.25				dB
0	0	0	0	0	0	1	0	0.50				dB
0	0	0	0	0	0	1	1	0.75				dB
0	0	0	0	0	1	0	0	1.00				dB
0	0	0	0	0	1	0	1	1.25	2	0	2	dB
0	0	0	0	0	1	1	0	1.50				dB
0	0	0	0	0	1	1	1	1.75				dB
0	0	0	0	1	0	0	0	2.00				dB
0	0	0	0	1	0	0	1	2.25				dB
0	0	0	0	1	0	1	0	2.50				dB
0	0	0	0	1	0	1	1	2.75				dB
0	0	0	0	1	1	0	0	3.00				dB
0	0	0	0	1	1	0	1	3.25	4	0	4	dB
								...				dB
0	0	0	1	0	1	0	1	5.25	6	0	6	dB
								...				dB

bTREBLE								TREBLE USB SIDE	TREBLE USB-DAC			UNIT
B7	B6	B5	B4	B3	B2	B1	B0		minimum	flat	maximum	
0	0	0	1	1	1	0	1	7.25	6	0	6	dB
								...				dB
0	0	1	0	0	1	0	1	9.25	6	0	6	dB
								...				dB
0	1	1	1	1	1	1	1	31.75	6	0	6	dB

Bass control

The Bass control is available for the master channel of the UDA1321. Bass can be regulated in three modes: minimum, flat and maximum mode. The preferred mode is selected at start-up of the device (configuration map). The Bass range is from 0 dB up to 18 dB (minimum mode) or 24 dB (maximum mode) in steps of 2 dB. Notice that the negative Bass values as defined in the *"USB Device Class Definition for Audio Devices"* are not supported by the UDA1321; the 0 dB value is returned as 0 dB. The corner frequency is 500 Hz for the minimum mode and 300 Hz for the maximum mode. Table 27 gives the mapping of the **bBass** value upon the actual Bass setting of the USB-DAC.

Table 27 Bass control characteristics.

bBASS								BASS USB SIDE	BASS USB-DAC			UNIT
B7	B6	B5	B4	B3	B2	B1	B0		minimum	flat	maximum	
0	0	0	0	0	0	0	0	0.00	0	0	0	dB
0	0	0	0	0	0	0	1	0.25				dB
0	0	0	0	0	0	1	0	0.50				dB
0	0	0	0	0	0	1	1	0.75				dB
0	0	0	0	0	1	0	0	1.00				dB
0	0	0	0	0	1	0	1	1.25	2	0	2	dB
0	0	0	0	0	1	1	0	1.50				dB
0	0	0	0	0	1	1	1	1.75				dB
0	0	0	0	1	0	0	0	2.00				dB
0	0	0	0	1	0	0	1	2.25				dB
0	0	0	0	1	0	1	0	2.50				dB
0	0	0	0	1	0	1	1	2.75				dB
0	0	0	0	1	1	0	0	3.00				dB
0	0	0	0	1	1	0	1	3.25	4	0	4	dB
								...				dB
0	0	0	1	0	1	0	1	5.25	6	0	6	dB
								...				dB
0	0	0	1	1	1	0	1	7.25	8	0	8	dB
								...				dB
0	0	1	0	0	1	0	1	9.25	10	0	10	dB
								...				dB

bBASS								BASS USB SIDE	BASS USB-DAC			UNIT
B7	B6	B5	B4	B3	B2	B1	B0		minimum	flat	maximum	
0	0	1	0	1	1	0	1	11.25	12	0	12	dB
								...				dB
0	0	1	1	0	1	0	1	13.25	14	0	14	dB
								...				dB
0	0	1	1	1	1	0	1	15.25	16	0	16	dB
								...				dB
0	1	0	0	0	1	0	1	17.25	18	0	18	dB
								...				dB
0	1	0	0	1	1	0	1	19.25	18	0	20	dB
								...				dB
0	0	1	1	1	0	1	1	21.25	18	0	22	dB
								...				dB
0	1	0	1	0	1	0	1	23.25	18	0	24	dB
								...				dB
0	1	1	0	0	1	0	1	25.25	18	0	24	dB
								...				dB
0	1	1	0	1	1	0	1	27.25	18	0	24	dB
								...				dB
0	1	1	1	0	1	0	1	29.25	18	0	24	dB
								...				dB
0	1	1	1	1	1	0	1	31.25	18	0	24	dB
								...				dB
0	1	1	1	1	1	1	1	31.75	18	0	24	dB

Dynamic Bass Boost control

Bass Boost is one of the sound features as defined in the *"USB Device Class Definition for Audio Devices"*. The Bass Boost control request data **bBassBoost** controls the position of the Bass Boost switch. The position can be either on or off. When **bBassBoost** is true the Bass Boost is activated. When **bBassBoost** is false the Bass Boost is off.

When clipping prevention is active, the Bass is reduced to avoid clipping with high volume settings. Bass Boost is selectable via the configuration map.

Clipping prevention

If the maximum of the Bass plus Volume gives clipping, the Bass is reduced. Clipping prevention is selectable via the configuration map.

De-emphasis

De-emphasis is one of the properties which is not supported by the USB. De-emphasis for 44.1 kHz can be predefined in the configuration map selected at start-up of the UDA1321.

Start-up and configuration of the UDA1321

START-UP OF THE UDA1321

After power-on, an internal power-on reset signal becomes HIGH after a certain RC-time (R = 5000 Ω, C = C_{ref}). During 10 ms after power-on reset the UDA1321 has to initiate the internal settings. 120 ms after the power-on reset the UDA1321 becomes master of the I²C-bus. The UDA1321 tries to read the eventually connected EEROM and if an EEROM is detected, the internal descriptors are overwritten and the selected port configuration is applied. If no EEROM is detected, the UDA1321 tries to read the logical levels of GP3 and GP0.Via these two GP-pins a choice can be made out of four internal configuration maps.

CONFIGURATION SELECTION OF THE UDA1321 VIA A DIODE MATRIX

The UDA1321 uses a configuration map to hold a number of specific configurable data on Hardware-, Product-, Component- and USB configuration level. At startup without EEROM, the UDA1321 will scan the logical levels of GP3 and GP0. With these two GP-pins it is possible to select one out of the four possible (vendor specific) configuration maps which are hold in the internal ROM space of the UDA1321 This selection can be done via a diode matrix (see Fig.4).

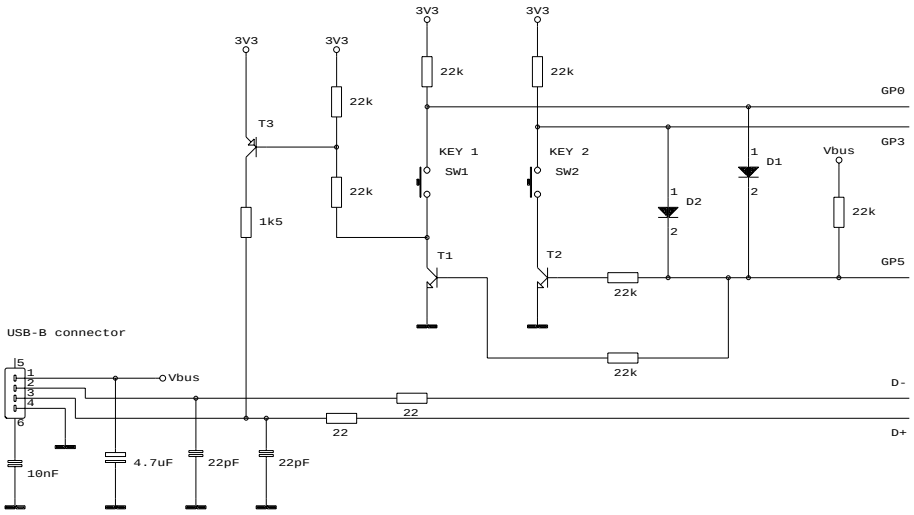


Fig.4 Diode matrix selection.

After choosing an internal configuration map the user cannot change the choosen settings for the GP-pins, internal configuration, descriptors etc. The internal congiguration map can be overwritten by connecting an I²C EEROM at start-up.

For more information about the internal (vendor specific) configuration maps see the application documentation.

CONFIGURATION OPTIONS OF THE UDA1321 VIA AN I²C EEROM

If an EEROM is detected (reading byte 0 as AA and byte 1 as 55) the UDA1321 will use the configuration map in the EEROM instead of one out of four internal configuration maps. The layout of the configuration map is fixed, the values (except bytes 0 and 1) are user definable see Table 28. If the user wants to change e.g. the manufacturer name this can be done via the EEROM code.

The communication between the UDA1321 and the external I²C device is based on the standard I²C-bus protocol given in the Philips specification *"The I²C-bus and how to use it (including specifications)"*, which can be ordered using the code 9398 393 40011. The I²C bus has two lines; a clock line SCL and a serial data line SDA (see Fig.5).

Table 28 Control options for the UDA1321 via EEROM Configuration map.

BYTE HEX	AFFECTS	COMMENTS	BIT	VALUE
0		recognition pattern do not change it		AA (HEX)
1		recognition pattern do not change it		55 (HEX)
2	ASR control register	ASR register start-up mode	0	0 = stop 1 = go
		audio mode	1	0 = mono 1 = stereo
		bits per sample modi	2 and 3	00 = reserved 01 = 8-bit audio 10 = 16-bit audio 11 = 24-bit audio
		Phase inversal	4	0 = mono phase inversal off 1 = mono phase inversal on
		serial I^2S output format	5 and 6	00 = I^2S 01 = 8-bit LSB 10 = 16-bit LSB 11 = 20-bit LSB
		Robust word clock	7	0 = off 1 = on
3	ADAC mode register 0	Reset ADAC	0	0 = No reset ADAC 1 = reset ADAC
		Mute control	1	0 = No mute 1 = Mute active
		Synchronous/Asynchronous control	2	0 = Asynchronous 1 = Synchronous
		Channel Manipulation	3	0 = L->L, R->R 1 = L->R, R->L
		De-emphasis	4	0 = de-emphasis off 1 = de-emphasis on
		Audio feature mode	5 and 6	00 = flat 01 = minimum 10 = minimum 11 = maximum
		Selection ADAC mode register	7	0

BYTE HEX	AFFECTS	COMMENTS	BIT	VALUE
4	ADAC mode register 1	serial I^2S input format	0 and 1	00 = I^2S 01 = 8-bit LSB 10 = 16-bit LSB 11 = 20-bit LSB
		digital PLL mode	2 and 3	00 = adaptive 01 = fixed state 1 10 = fixed state 2 11 = fixed state 3
		digital PLL lock mode	4	0 = adaptive 1 = fixed
		digital PLL lock speed	5 and 6	00 = lock after 512 samples 01 = lock after 2048 samples 10 = lock after 4096 samples 11 = lock after 16348 samples
		Selection ADAC mode register	7	1 (HEX)
5	I/O selection register	GP0	0	0 = Function 1 1 = Function 2
		GP1	1	
		GP2	2	
		GP3	3	
		GP4	4	
		4/6 pins IIS	5	Only if IIS is used; 0 = 4 pins IIS 1 = 6 pins IIS
		IIS	6	0 = no IIS used 1 = IIS used
		Clipping	7	0 = no clipping 1 = clipping function active
6		GP0 usagepage Tag if HID selected		
7		GP0 usage Tag if HID selected		
8		GP1 usagepage Tag if HID selected		
9		GP1 usage Tag if HID selected		
A		GP2 usagepage Tag if HID selected		
B		GP2 usage Tag if HID selected		
C		GP3 usagepage Tag if HID selected		
D		GP3 usage Tag if HID selected		
E		GP4 usagepage Tag if HID selected		
F		GP4 usage Tag if HID selected		
10		Rise Time power Amplifier, steps of 20 msec		

BYTE HEX	AFFECTS	COMMENTS	BIT	VALUE
11		Time between Mute and Play, steps of 1 sec		
12		Time between Mute and Standby, steps of 5 sec		
13		DBB value steps of 1dB with max. 255 dB		0= no DBB active 1..FF = DBB active
14		Absolute default volume value		
15		**idVendor** High Byte		
16		**idVendor** Low Byte		
17		**idProduct** High Byte		
18		**idProduct** Low Byte		
19		**bmAttributes**		
1A		MaxPower steps of 2 mA with max. 500 mA		
1B		pointer language string		20
1C		pointer manufacturer string		30
1D		pointer product string		40
1E		pointer serial Number		50
1F				
20->		Language string		
30->		Manufacturer string		
40->		Product string		
50->		Serial Number		

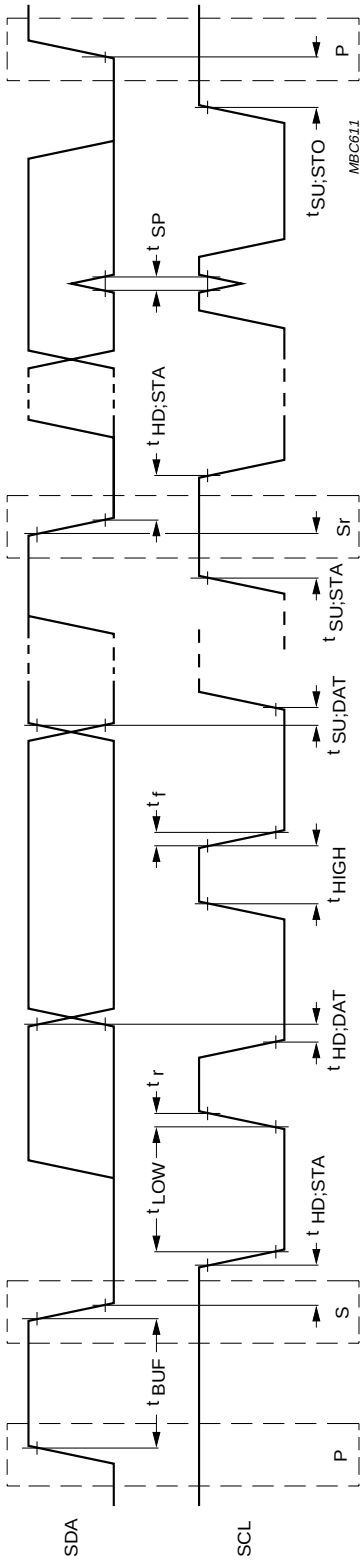


Fig.5 Definition of timing of the I²C-bus.

The general purpose I/O-pins (GP0 to GP7)

The UDA1321 has 8 General Purpose (GP) I/O-pins.
Six of these can be used either for digital I/O functionality or for general purposes; these are pins GP0, GP1, GP2, GP3, GP4 and GP5. Two of the 8 GP I/O-pins can be used for I^{2}C-bus communication with an external IC; these are pins GP6 and GP7.

There are basically three port configurations:

- No digital I/O communication
- 4-pin digital I/O communication
- 6-pin digital I/O communication.

These port configurations can be chosen via the configuration map at start-up of the UDA1321.

The user can make a choice between two functions for ports GP0 to GP4 (see I/O selection register; Table 28), except if digital I/O communication is selected (see Tables 29, 30 and 31).

Table 29 No digital I/O communication

PIN	INPUT/OUTPUT	FUNCTION 1	FUNCTION 2
GP7	I^{2}C-bus pins, not programmable(1)	I^{2}C-bus data	I^{2}C-bus data
GP6		I^{2}C-bus clock	I^{2}C-bus clock
GP5	output, not programmable(2)	connect/disconnect	connect/disconnect
GP4	inputs, programmable	alarm mute(3)	HID input 3
GP3		HID input 2	HID input 2
GP0		HID input 1	HID input 1
GP2	outputs, programmable	standby(4)	HID output 2
GP1		mute(5)	HID output 1

Notes

1. These lines must have a pull-up resistor.
2. connect/disconnect: holds the USB ‘disconnected’ as long as the initialization is not finished.
3. Alarm mute: input to switch the sound off; specially used if the USB-host program does not respond to the control. This button acts directly on the sound and passes the mute to the USB-host.
4. Standby: switched on if the mute is active for 2 minutes programmable time.
5. Mute: is switched on if the isochronous data flow is interrupted.

Table 30 Four pins digital I/O communication

PIN	INPUT/OUTPUT	FUNCTION 1	FUNCTION 2
GP7	I^2C-bus pins, not programmable	I^2C-bus data	I^2C-bus data
GP6		I^2C-bus clock	I^2C-bus clock
GP5	output, not programmable(1)	connect/disconnect	connect/disconnect
GP4	digital I/O-bus	BCK output	BCK output
GP3		WS output	WS output
GP2		DATA output	DATA output
GP1		DATA input	DATA input
GP0	inputs, programmable	HID input 1	alarm mute(2)

Notes

1. connect/disconnect: holds the USB ‘disconnected’ as long as the initialization is not finished.
2. Alarm mute: input to switch the sound off; specially used if the USB-host program does not respond to the control. This button acts directly on the sound and passes the mute to the USB-host.

Table 31 Six pins digital I/O communication

PIN	INPUT/OUTPUT	FUNCTION 1
GP7	I^2C-pins, not programmable	SDA
GP6		SCL
GP5	digital I/O-bus	WS input
GP4		BCK output
GP3		WS output
GP2		DATA output
GP1		DATA input
GP0		BCK input

Filter characteristics

The overall filter characteristic of the UDA1321 in flat mode is given in the figure below. The overall filter characteristic of the UDA1321 includes the filter characteristics of the DSP in flat mode plus the filter characteristic of the FSDAC.

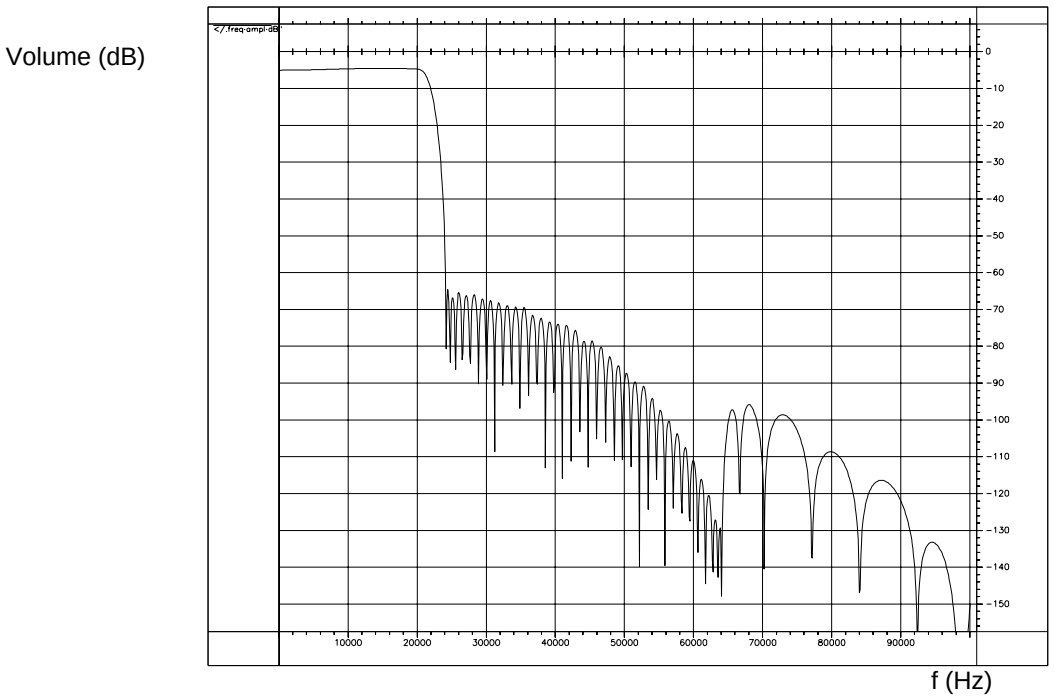


Fig.6 Overall filter characteristics of the UDA1321.

DSP extension port

Via the digital I/O-bus an external DSP can be used for adding extra sound processing features. The UDA1321 supports the standard I^2S data protocol and the LSB justified serial data input format with word lengths of 16, 18 and 20 bits. Using the 4-pin digital I/O-bus the UDA1321 device acts as a master, controlling the BCK and WS signals. The period of the WS signal is determined by the number of samples in the 1 ms frame of the USB. This implies that the WS signal has not a constant period time, but is jittery. Using the 6-pin digital I/O-pins GP2, GP3 and GP4 are output pins (master) and GP0, GP1 and GP5 are input pins (slave).

For characteristic timing of the I^2S-bus input interface see Figs 7 and 8.

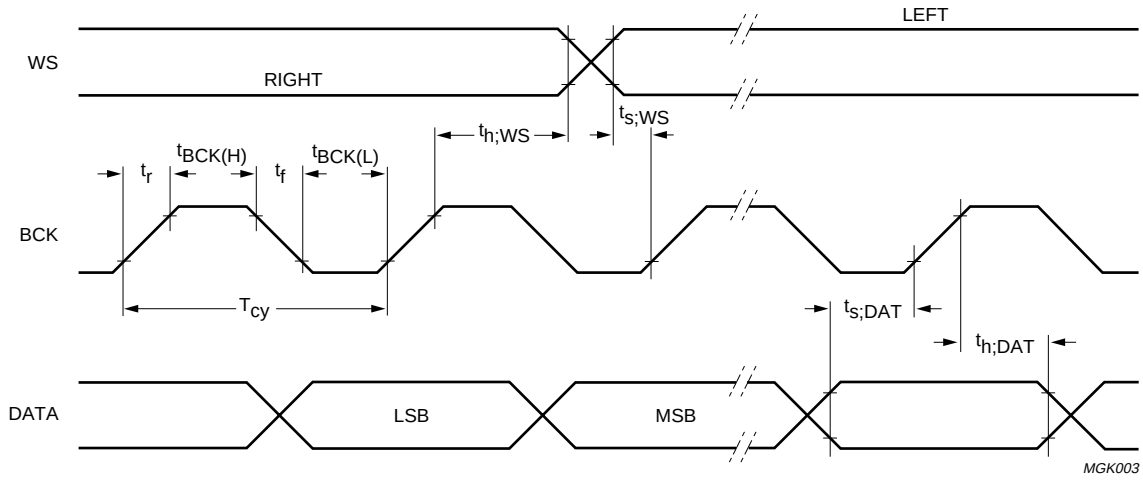


Fig.7 Timing and digital I/O-input signals.

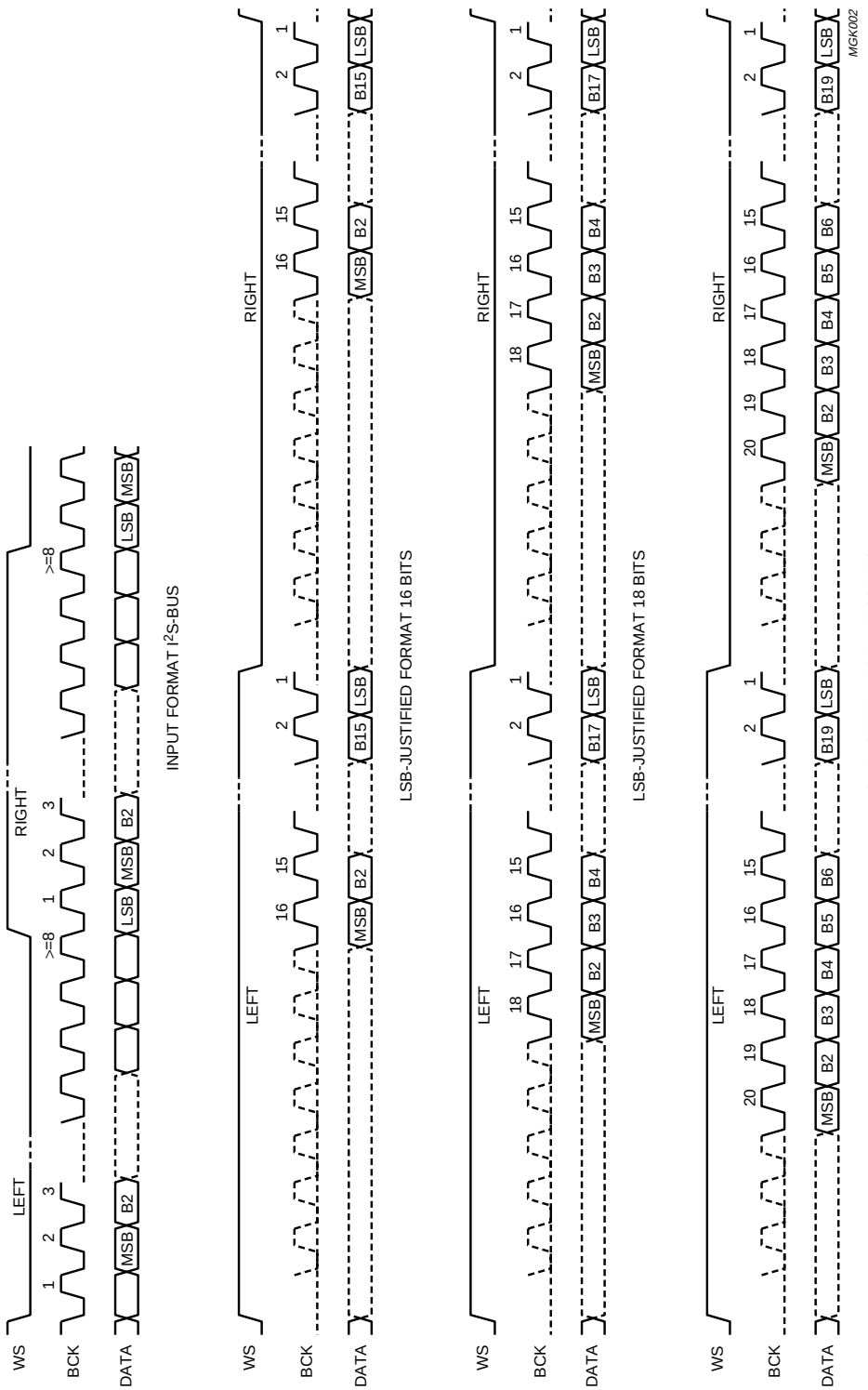


Fig.8 Input formats.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
All digital I/Os						
$V_{I/O}$	DC input/output voltage range for I/Os		–0.5	–	V_{DD}	V
I_O	input/output current		–	–	4	mA
Temperature						
T_j	junction temperature		0	–	125	°C
T_{stg}	storage temperature		–55	–	+150	°C
T_{amb}	operating ambient temperature		0	25	70	°C
Electrostatic handling						
V_{es}	electrostatic handling	note 1	–3000	–	+3000	V
		note 2	–300	–	+300	V

Notes

1. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.
2. Equivalent to discharging a 200 pF capacitor through a 2.5 μH series inductor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	57	K/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3.0	3.3	3.6	V
V_I	DC input voltage D+ and D–		0.0	–	V_{DD}	V
$V_{I/O}$	DC input voltage for I/Os		0.0	–	V_{DD}	V

DC CHARACTERISTICS

VDD = 3.3 V; VSS = 0 V; Tamb = 25 °C; fosc = 48 MHz; fs = 44.1 kHz unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Supply					
V_{DDE}	digital supply voltage (I/O)	3.0	3.3	3.6	V
V_{DDI}	digital supply voltage core	3.0	3.3	3.6	V
V_{DDA}	analog supply voltage	3.0	3.3	3.6	V
V_{DDO}	operational amplifier supply voltage	3.0	3.3	3.6	V
V_{DDX}	crystal oscillator supply voltage	3.0	3.3	3.6	V
I_{DDE}	digital supply current periphery	–	3	–	mA
I_{DDI}	digital supply current core	–	36	–	mA
I_{DDA}	analog supply current	–	4.2	–	mA
I_{DDO}	operational amplifier supply current	–	4.0	–	mA
I_{DDX}	crystal oscillator supply current	–	2.1	–	mA
P_{tot}	total power dissipation	–	165	-	mW
P_{ps}	total power dissipation in power saving mode	–	60	-	mW
Inputs/outputs D+ and D–					
V_I	static DC input voltage	–0.5	–	V_{DDE}	V
V_O	static DC output voltage	0.0	–	V_{DDE}	V
Digital input pins					
V_{IL}	LOW level input voltage	–	–	$0.3V_{DDI}$	V
V_{IH}	HIGH level input voltage	$0.7V_{DDI}$	–	V_{DDI} + 0.5	V
$\lvert I_{LI} \rvert$	input leakage current	–	–	1	μA
C_i	input capacitance	–	–	tbf	pF
Filter stream DAC					
V_{ref}	reference voltage	-	$0.5V_{DDA}$	-	V
$V_{o(cm)}$	common mode output voltage	-	$0.5V_{DDA}$	-	V
R_o	output resistance at pins VOUTL and VOUTR	–	0.14	0.16	Ω
$R_{o(L)}$	output load resistance	2.0	–	–	kΩ
$C_{o(L)}$	output load capacitance	–	–	50	pF

AC CHARACTERISTICS

VDD = 3.3 V; VSS = 0 V; Tamb = 25 °C; fosc = 48 MHz; fs = 44.1 kHz unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Driver characteristics D+ and D– (full speed mode)						
t_r	rise time	C_L = 50 pF	4	–	20	ns
t_f	fall time	C_L = 50 pF	4	–	20	ns
t_{rfm}	rise/fall time matching (T_r/T_f)		90	–	110	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{cr}	output signal crossover voltage		1.3	–	2.0	V
$R_{(o)DRV}$	driver output resistance	steady-state drive	28	–	43	Ω
Data source timings D+ and D– (full speed mode)						
$f_{i(sample)}$	audio sample input frequency		5	–	55	kHz
$f_{fs(D)}$	full speed data rate		11.97	12.00	12.03	Mbits/s
t_{FRAME}	frame interval		0.9995	1.0000	1.0005	ms
t_{DJ1}	source differential jitter to next transition		–3.5	0.0	+3.5	ns
t_{DJ2}	source differential jitter for paired transitions		–4.0	0.0	+4.0	ns
t_{EOPT}[1]	source EOP width		160	–	175	ns
t_{DEOP}	differential to EOP transition skew		–2.0	–	+5.0	ns
t_{JR1}	receiver data jitter tolerance to next transition		–18.5	0.0	+18.5	ns
t_{JR2}	receiver data jitter tolerance for paired transitions		–9.0	0.0	+9.0	ns
t_{EOPR1}	EOP width at receiver must reject as EOP		40	–	–	ns
t_{EOPR2}	EOP width at receiver must accept as EOP		82	–	–	ns
Serial input/output data timing; see Fig.7						
f_{sys}	system clock frequency		–	12	–	MHz
$f_{i(sel)(WS)}$	word selection input frequency		5	–	55	kHz
t_r	rise time		–	–	20	ns
t_f	fall time		–	–	20	ns
$t_{BCK(H)}$	bit clock HIGH time		55	–	–	ns
$t_{BCK(L)}$	bit clock LOW time		55	–	–	ns
$t_{s;DAT}$	data set-up time		10	–	–	ns
$t_{h;DAT}$	data hold time		20	–	–	ns
$t_{s;WS}$	word selection set-up time		20	–	–	ns
$t_{h;WS}$	word selection hold time		10	–	–	ns
SDA and SCL lines (fast mode I^2C-bus); see Fig.5						
f_{SCL}	SCL clock frequency		0	–	100	kHz
t_{BUF}	bus free time between a STOP and START condition		4.7	–	–	µs
$t_{HD;STA}$	hold time (repeated) start condition		4.0	–	–	µs
t_{LOW}	LOW period of the SCL clock		4.7	–	–	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	–	–	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	–	–	µs
$t_{SU;STO}$	set-up time for STOP condition		4.0	–	–	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{HD;DAT}$	data hold time		5.0	–	0.9	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
t_{SP}	pulse width of spikes which must be suppressed by the input filter		tbf	–	tbf	ns
t_r	rise time of both SDA and SCL signals		–	–	1000	ns
t_f	fall time of both SDA and SCL signals		–	–	300	ns
C_b	capacitive load for each bus line		–	–	400	pF
Oscillator						
f_{osc}	oscillator frequency		–	48	–	MHz
δ	duty factor		–	50	–	%
g_m	transconductance		13.5	23.0	30.5	mS
R_o	output resistance		450	700	1450	Ω
$C_{i(xtal1)}$	parasitic input capacitance XTAL1		10	11	12	pF
$C_{i(xtal2)}$	parasitic input capacitance XTAL2		4.5	5.0	5.5	pF
I_{start}	start-up current		4.3	8.8	15.0	mA
Power-on reset						
$t_{su(PO)}$	power-on set-up time	note 2	$5C_{ref}$[3]	–	–	ms
Filter Stream DAC (FSDAC)						
RES	resolution		16	–	–	bits
$V_{FS(rms)}$	full-scale output voltage (RMS value)	V_{DD} = 3.3 V	–	0.66	–	V
SVRR	supply voltage ripple rejection V_{DDA} and V_{DDO}	f_{ripple} = 1 kHz $V_{ripple(p-p)}$ = 0.1 V	–	60	–	dB
$\lvert\Delta V_o\rvert$	channel unbalance	maximum volume	–	0.03	–	dB
α_{ct}	crosstalk between channels	R_L = 5 kΩ	–	95	–	dB
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	f_s = 44.1 kHz; R_L = 5 kΩ				
		at input signal of 1 kHz (0 dB)	–	–85	–80	dB
			–	0.0056	0.01	%
		at input signal of 1 kHz (–60 dB)	–	–30	–20	dB
			–	3.2	10	%
S/N	signal-to-noise ratio at bipolar zero	A-weighted at code 0000H	90	95	–	dBA

Notes

1. EOP means End Of Packet.
2. Strongly depends on the external decoupling capacitor connected to V_{ref} (pin 15).
3. C_{ref} in µF.

APPLICATION INFORMATION

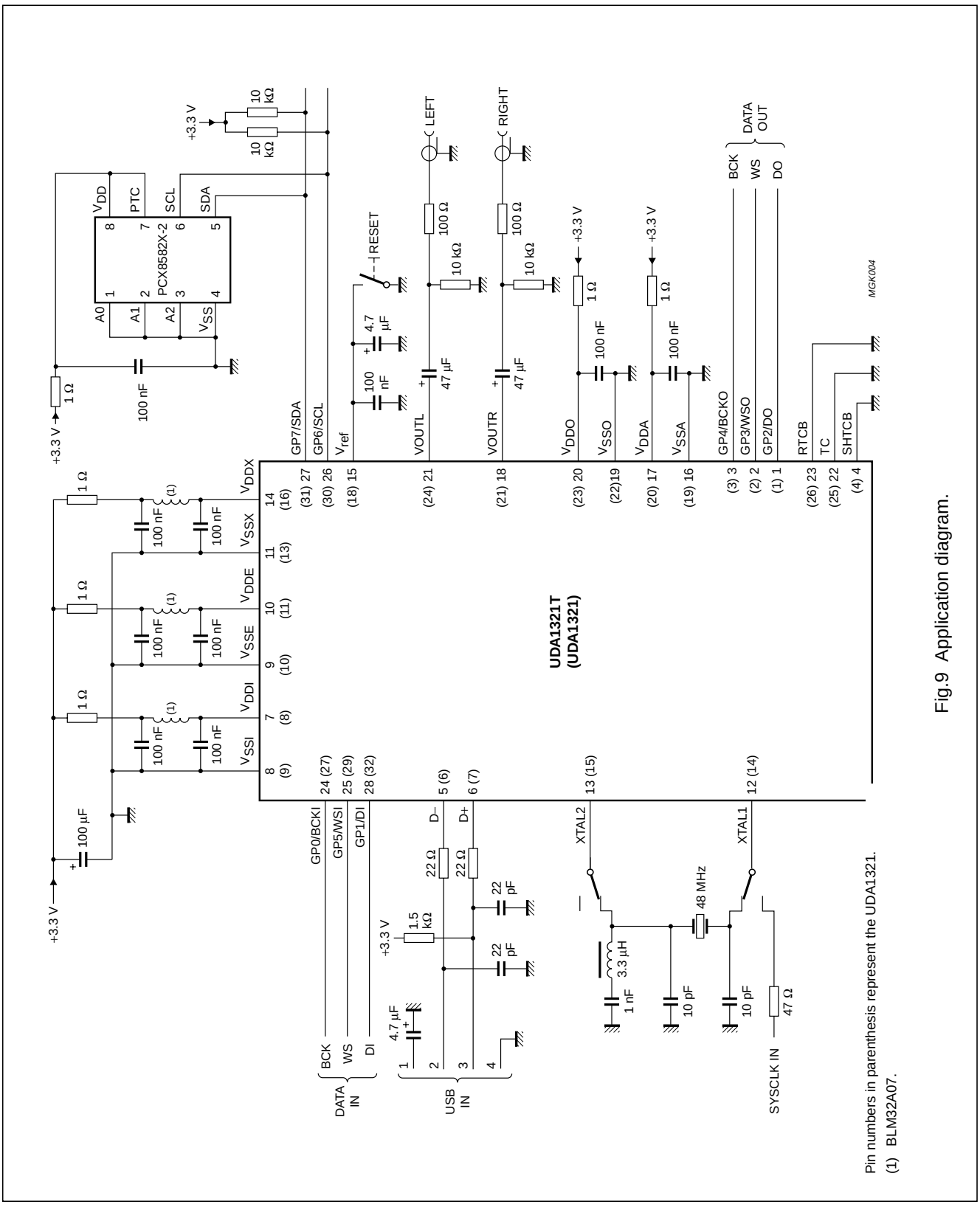


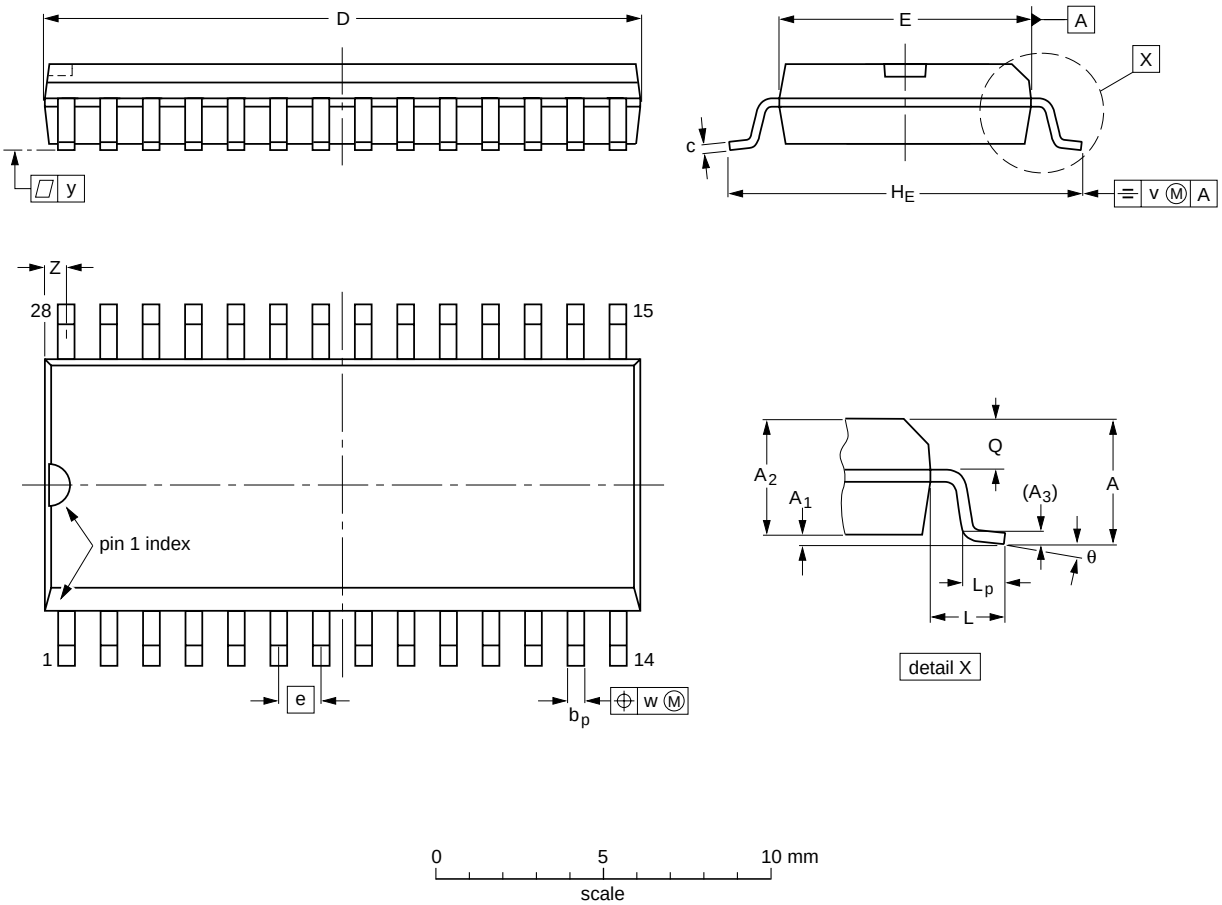
Fig.9 Application diagram.

Pin numbers in parenthesis represent the UDA1321.

(1) BLM32A07.

PACKAGE OUTLINE

SO28: plastic small outline package; 28 leads; body width 7.5 mm **SOT136-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

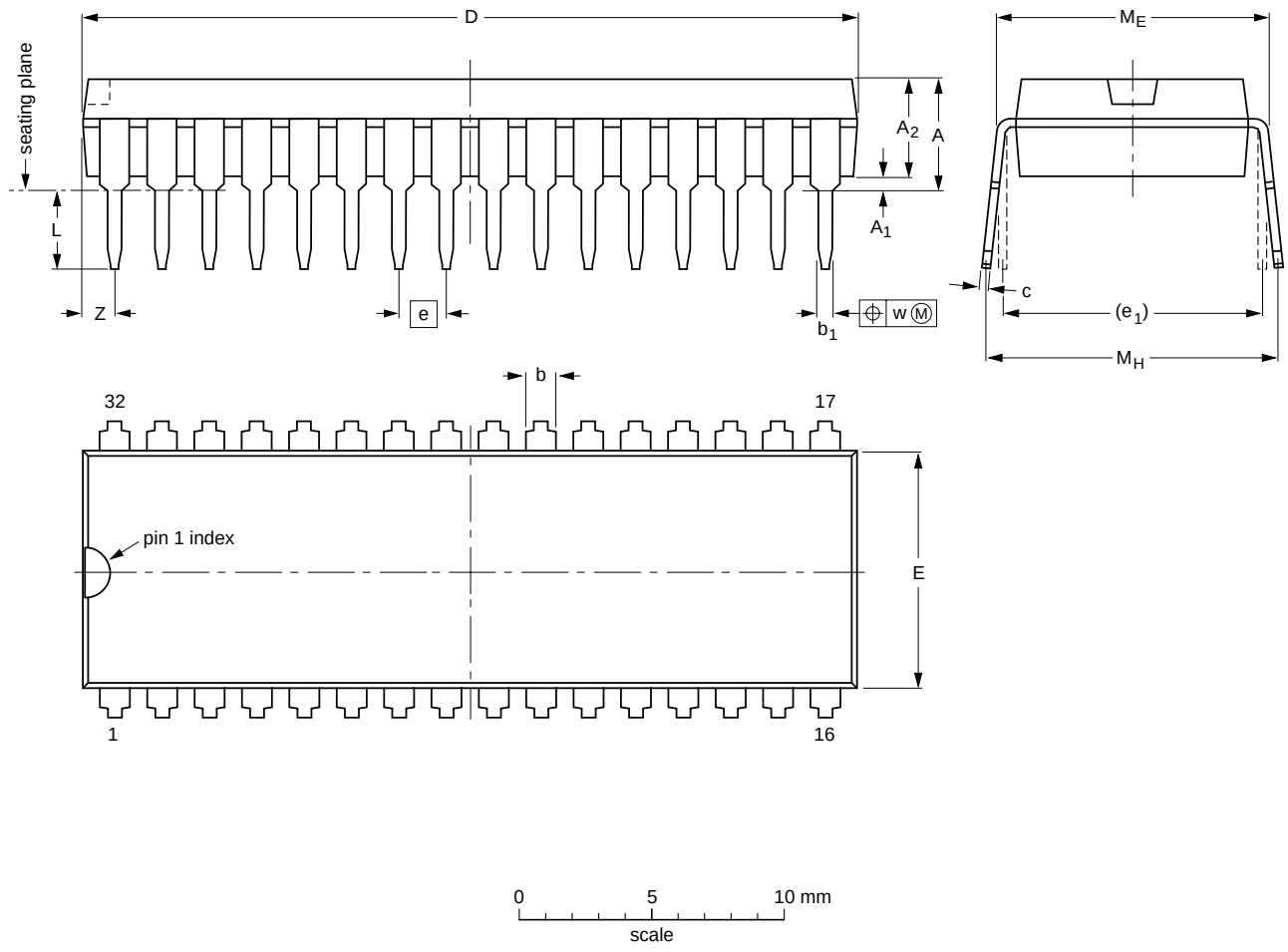
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~95-01-24~~ 97-05-22

PACKAGE OUTLINE

SDIP32: plastic shrink dual in-line package; 32 leads (400 mil) **SOT232-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.8	1.3 0.8	0.53 0.40	0.32 0.23	29.4 28.5	9.1 8.7	1.778	10.16	3.2 2.8	10.7 10.2	12.2 10.5	0.18	1.6

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT232-1						~~92-11-17~~ 95-02-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

SDIP

SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
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