DATA SHEET

UBA2021
630 V driver IC for CFL and TL lamps

Product specification
File under Integrated Circuits, IC11

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Philips Semiconductors

PHILIPS

FEATURES

- Adjustable preheat and ignition time
- Adjustable preheat current
- Adjustable lamp power
- Lamp temperature stress protection at higher mains voltages
- Capacitive mode protection
- Protection against a too low drive voltage for the power MOSFETs.

GENERAL DESCRIPTION

The UBA2021 is a high voltage IC intended to drive and control a Compact Fluorescent Lamp (CFL). It contains a driver circuit for an external half-bridge, an oscillator and a control circuit for starting up, preheating, ignition, lamp burning and protection.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
High voltage supply						
V_{FS}	high side supply voltage	I_{FS} < 15 µA; t < 0.5 s	–	–	630	V
Start-up state						
V_{start}	oscillator start voltage		–	11.95	–	V
V_{stop}	oscillator stop voltage		–	10.15	–	V
I_{stb}	standby current	V_{VS} = 11 V	–	200	–	µA
Preheat mode						
f_{start}	start frequency		–	108	–	kHz
t_{ph}	preheat time	C_{CP} = 100 nF	–	666	–	ms
$V_{ctrl(RS)}$	control voltage at pin RS		–	–600	–	mV
Frequency sweep to ignition						
f_B	bottom frequency		–	43	–	kHz
t_{ign}	ignition time		–	625	–	ms
Normal operation						
f_B	bottom frequency		–	42.9	–	kHz
t_{no}	non-overlap time		–	1.4	–	µs
I_{tot}	total supply current	f_B = 43 kHz	–	1	–	mA
$R_{on(FS,VS)}$	high and low side on resistance		–	126	–	Ω
$R_{off(FS,VS)}$	high and low side off resistance		–	75	–	Ω
Feedforward						
f_{ff}	feedforward frequency	I_{RHV} = 0.75 mA	–	64	–	kHz
		I_{RHV} = 1.0 mA	–	84.5	–	kHz
$I_{i(op)(RHV)}$	operating range of the input current at pin RHV		0	–	1000	µA

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UBA2021T	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
UBA2021P	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1

BLOCK DIAGRAM

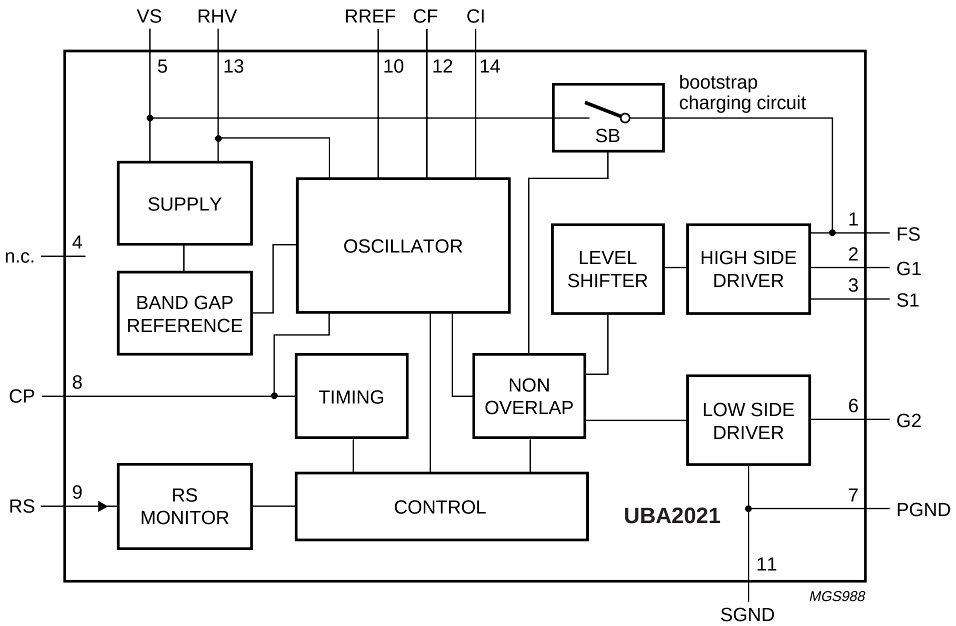


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
FS	1	high side floating supply voltage
G1	2	gate high transistor (T1)
S1	3	source high transistor (T1)
n.c.	4	high-voltage spacer, not to be connected
VS	5	low side floating supply voltage
G2	6	gate low transistor (T2)
PGND	7	power ground
CP	8	timing/averaging capacitor
RS	9	current monitoring input
RREF	10	reference resistor
SGND	11	signal ground
CF	12	oscillator capacitor
RHV	13	start-up resistor/feedforward resistor
CI	14	integrating capacitor

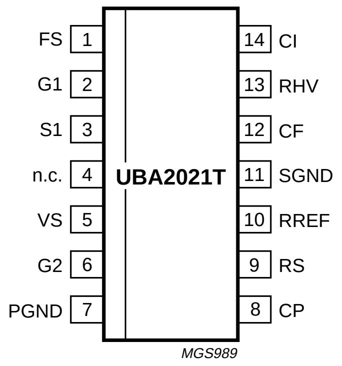


Fig.2 Pin configuration (SO14).

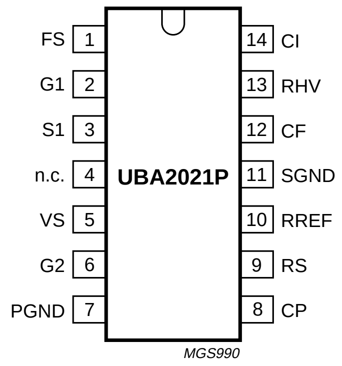


Fig.3 Pin configuration (DIP14).

FUNCTIONAL DESCRIPTION

Introduction

The IC is a integrated circuit for electronically ballasted compact fluorescent lamps and its derivatives, up to a nominal mains voltage of 240 V (RMS). It provides all the necessary functions for proper preheat, ignition and on-state operation of the lamp. Besides the control function, the IC provides the level shift and drive function for the 2 discrete power MOSFETs.

Initial start-up

Initial start-up is achieved by charging CS9 with the current applied to pin RHV. The start-up of the circuit is such that T2 shall be conductive and T1 shall be non-conductive, in order to make sure that C_{boot} gets charged. This start-up state is reached for a supply voltage $V_{VS(reset)}$ (this is the voltage level at pin VS at which the circuit will be reset to the initial state) and maintained until the low voltage supply (V_{VS}) reaches a value of V_{start}. The circuit is reset in the start-up state.

Oscillation

If the low voltage supply (V_{VS}) has reached the value of V_{start} the circuit starts oscillating in the preheat state. The internal oscillator is a current-controlled circuit which generates a sawtooth waveform. The frequency of the sawtooth is determined by the capacitor C_{CF} and the current out of pin CF (mainly set by R_{RREF}). The sawtooth frequency is twice the frequency of the signal across the load. The IC brings alternately the transistors T1 and T2 into conduction with a duty cycle of approximately 50%. Figure 4 represents the timing of the IC. The circuit block 'non-overlap' generates a non-overlap time t_{no} when T1 and T2 are conducting. This is dependant on the reference current.

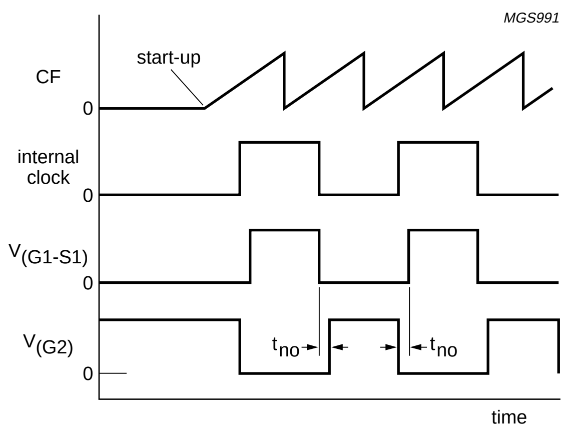
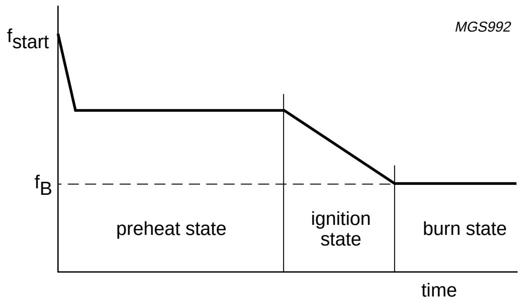


Fig.4 Oscillator timing.

Operation in the preheat mode

The circuit starts oscillating at a frequency of approximately $2.5f_B$ (108 kHz). The frequency will gradually decrease until a defined value of the current through R_{shunt} is reached (see Fig.5). The slope of the decrease in frequency is determined by the capacitor connected to pin CI. The frequency during preheating will be approximately 90 kHz. This frequency is well above the resonant frequency of the load, which means that the lamp is off; the load consists of L2, C5 and the electrode resistance only (see Fig.7). The preheat time is determined by the capacitor connected to pin CP. The circuit can be locked in the preheat state by connecting pin CP to ground. During preheating the circuit monitors the load current by measuring the voltage drop over external resistor R_{shunt} at the end of conduction of T2 with decision level V_{shunt}. The frequency is decreased as long as $V_{RS} > V_{shunt}$. The frequency is increased for $V_{RS} < V_{shunt}$.



For calculations refer to Chapter “Design equations”.

Fig.5 Operation in the preheat mode.

Ignition state

The RS monitoring function changes from V_{shunt} regulation to capacitive mode protection at the end of the preheat time. Normally this results in a further frequency decrease down to the bottom frequency f_B (approximately 43 kHz). The frequency change per ms is lowered with respect to the frequency change in the preheat mode. During the downward frequency sweep the circuit sweeps through the resonant frequency of the load. A high voltage will then appear across the lamp. This voltage will normally ignite the lamp.

Failure to ignite

Excessive current levels may occur when the lamp fails to ignite. The IC does not limit these currents in any manner.

Transition to the burn state

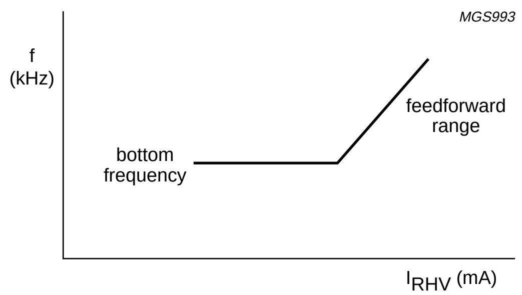
Assuming that the lamp has ignited during the downward frequency sweep, the frequency normally decreases to the bottom frequency. The IC can transit to the burn state in two ways:

1. In the event that the bottom frequency is not reached, the transition is made after reaching the ignition time t_{ign}.
2. As soon as the bottom frequency is reached.

The bottom frequency is determined by R_{RREF} and C_{CF}.

Feedforward frequency

Above a defined voltage level the oscillation frequency also depends on the supply voltage of the half-bridge (see Fig.6). The current for the current-controlled oscillator is in this feedforward range and is derived from the current through R_{RHV}. The feedforward frequency will be proportional to the average value of the current through R_{RHV} within the operating range of I_{RHV}, given the lower limit set by f_B. For currents beyond the operating range (i.e. between 1.0 and 1.6 mA) the feedforward frequency is clamped. In order to prevent feedforward of the ripple of the V_{in} voltage, the ripple is filtered out. The capacitor connected to pin CP is used for this purpose. This pin is also used in the preheat state and the ignition state for timing (t_{ph} and t_{ign}).



For calculations refer to Chapter “Design equations”.

Fig.6 Feedforward frequency.

Capacitive mode protection

When the preheat mode is completed, the IC will protect the power circuit against losing the zero voltage switching condition and getting too close to the capacitive mode of operation. This is detected by monitoring the voltage across R_{shunt}. If the voltage at pin RS is below $V_{RS(cap)}$ at the time of turn-on of T2, then capacitive mode operation is assumed. Consequently, the frequency will be increased as long as the capacitive mode is detected. The frequency decreases down to the feedforward frequency if no capacitive mode is detected. Frequency modulation is achieved via pin CI.

IC supply

Initially, the IC is supplied from V_{in} by the current through R_{RHV}. This current charges the supply capacitor CS9 via an internal diode. As soon as VS exceeds V_{start}, the circuit starts oscillating. After the preheat phase is finished, pin RHV is connected to an internal resistor (R_{RHV}); prior to this the pin is internally connected to pin VS. The voltage level at pin RHV thus drops from ($VS + V_d$) to $I_{RHV} \times R_{RHV}$. The capacitor CS9 at pin VS will now be charged via the snubber capacitor CS7. Excess charge is drained by an internal clamp that turns on at voltage VS_{clamp}.

Minimum gate-source voltage of T1 and T2

The high side driver is supplied via capacitor C_{boot}. C_{boot} is charged via the bootstrap switch during the on-periods of T2. The IC stops oscillating at a voltage level V_{stop}. Given a maximum charge consumption on the load at pin G1 of 1 nC/V, this safeguards the minimum drive voltages $V_{(G1-S1)}$ for the high side driver; see Table 1.

Table 1 Minimum gate-source voltages

FREQUENCY	VOLTAGE
<75 kHz	8 V (min.)
75 kHz to 85 kHz	7 V (min.)
≥85 kHz	6 V (min.)

The drive voltage at G2 will exceed the drive voltage of the high side driver.

Frequency and change in frequency

At any point in time during oscillation, the circuit will operate between f_B and f_{start}. Any change in frequency will be gradual, no steps in frequency will occur. Changes in frequency caused by a change in voltage at pin CI, show a rather constant dF/dt over the entire frequency range. The following rates are realised (at a frequency of 85 kHz and a 100 nF connected to pin CI):

- For any increase in frequency the dF/dt will be between 15 and 37.5 kHz/ms
- During preheat and normal operation: the dF/dt for a decrease in frequency is between –6 and –15 kHz/ms
- During the ignition phase: the dF/dt for a decrease in frequency is between –150 and –375 Hz/ms.

Ground pins

Pin PGND is the ground reference of the IC with respect to the application. As an exception, pin SGND provides a local ground reference for the components connected to pins CP, CI, RREF and CF. For this purpose pins PGND and SGND are short-circuited internally. External connection to pins PGND and SGND is not preferred. The sum of currents flowing out of the pins CP, CI, RREF, CF and SGND must remain zero at any time.

Charge coupling

Due to parasitic capacitive coupling to the high voltage circuitry, all pins are burdened with a repetitive charge injection. Given the typical application in Fig.7 the pins RREF and CF are sensitive to this charge injection. For the rating Q_{coup} a safe functional operation of the IC is guaranteed, independent of the current level. Charge coupling at current levels below 50 µA will not interfere with the accuracy of the $V_{RS(cap)}$ and V_{shunt} levels. Charge coupling at current levels below 20 µA will not interfere with the accuracy of any parameter.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); all voltages referenced to ground.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{FS}	high side floating supply voltage	operating	–	570	V
		during 0.5 s	–	630	V
I_{clamp}	clamp current	during 0.5 s	–	35	mA
$V_{i(RS)}$	input voltage pin RS		–2.5	+2.5	V
		transient of 50 ns	–1.5	+2.5	V
SR	slew rate at pins S1, G1 and FS (with respect to ground)		–4	+4	V/ns
P	power dissipation		–	500	mW
T_{amb}	ambient temperature		–40	+150	°C
T_j	junction temperature		–40	+150	°C
T_{stg}	storage temperature		–55	+150	°C
Q_{coup}	charge coupling at pins RREF and CF	operating	–8	+8	pC
V_{es}	electrostatic handling	human body model	–	1000	V
		machine model	–	125	V

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
	SO14		100	K/W
	DIP14		60	K/W
$R_{th(j-pin)}$	thermal resistance from junction to pcb	in free air		
	SO14		50	K/W
	DIP14		30	K/W

QUALITY SPECIFICATION

In accordance with *“SNW-FQ-611-E”.*

CHARACTERISTICS

V_{VS} = 11 V; V_{FS} – V_{S1} = 11 V; T_{amb} = 25 °C; all voltages referenced to ground; see Fig.7; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
High voltage supply						
I_L	leakage current on high voltage pins	V_{FS}, V_{G1} and V_{S1} = 630 V	–	–	15	μA
Start-up state						
V_{rst}	reset voltage	T1 off; T2 on	4.0	5.5	6.5	V
V_{start}	oscillator start voltage		11.35	11.95	12.55	V
V_{stop}	oscillator stop voltage		9.55	10.15	10.75	V
V_{hys}	supply voltage hysteresis		1.5	1.8	2.0	V
$I_{stb(VS)}$	standby supply current at pin VS	note 1; V_{VS} = 11 V	150	200	250	μA
$\Delta V_{(RHV-VS)}$	voltage difference between pins RHV and VS	I_{RHV} = 1.0 mA	0.7	0.8	1.0	V
$V_{clamp(start)}$	clamp margin to V_{start}	note 2	0.2	0.3	0.4	V
I_{clamp}	clamp current	V_{VS} < 17 V	–	14	35	mA
Preheat mode						
f_{start}	starting frequency	V_{CI} = 0 V	98	108	118	kHz
t_g	conducting time T1 and T2	f_{start} = 108 kHz	–	3.2	–	μs
$I_{ch(CI)}$	charge current at pin CI	V_{CI} = 0 V; V_{RS} = –0.3 V	38	44	50	μA
$I_{dch(CI)}$	discharge current at pin CI	V_{CI} = 0 V; V_{RS} = –0.9 V	79	93	107	μA
t_{ph}	preheat time		599	666	733	ms
$I_{ch(CP)}$	charge current at pin CP	V_{CP} = 1 V	–	6.0	–	μA
$I_{dch(CP)}$	discharge current at pin CP	V_{CP} = 1 V	–	5.95	–	μA
$V_{diff(M)(CP)}$	peak voltage difference at pin CP	when timing	–	2.5	–	V
$V_{ctrl(RS)}$	control voltage at pin RS	note 3	–636	–600	–564	mV
Frequency sweep to ignition						
$I_{ch(CI)}$	charge current at pin CI	V_{CI} = 1.5 V; f ≈ 85 kHz	0.8	1.0	1.2	μA
f_B	bottom frequency	V_{CI} at clamp level	–	42.9	–	kHz
t_{ign}	ignition time		–	625	–	ms
Normal operation						
f_B	bottom frequency		42.21	42.90	44.59	kHz
t_g	conducting time T1 and T2	f_B = 43 kHz	–	10.2	–	μs
g_{no}	non-overlap conductance time		1.05	1.4	1.75	μs
I_{tot}	total supply current	f_B = 43 kHz; note 4	0.85	1.0	1.1	mA
$V_{ctrl(cap)}$	capacitive mode control voltage	note 5	0	20	40	mV
V_{ref}	reference voltage	note 6	2.425	2.5	2.575	V
$V_{on(G1)}$	on voltage at pin G1	I_o = 1 mA; note 7	10.5	–	–	V
$V_{off(G1)}$	off voltage at pin G1	I_o = 1 mA; note 7	–	–	0.3	V
$V_{on(G2)}$	on voltage at pin G2	I_o = 1 mA; note 7	10.5	–	–	V
$V_{off(G2)}$	off voltage at pin G2	I_o = 1 mA; note 7	–	–	0.3	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{on(FS)}$	high side on resistance	$V_{(G1-S1)}$ = 3 V; notes 7 and 8	100	126	152	Ω
$R_{off(FS)}$	high side off resistance	$V_{(G1-S1)}$ = 3 V; notes 7 and 8	60	75	90	Ω
$R_{on(VS)}$	low side on resistance	V_{G2} = 3 V; note 8	100	126	152	Ω
$R_{off(VS)}$	low side off resistance	V_{G2} = 3 V; note 8	60	75	90	Ω
V_{drop}	voltage drop at bootstrap switch	I_{FS} = 5 mA	0.6	1.0	1.4	V
Feedforward						
$R_{i(RHV)}$	input resistance at pin RHV		1.54	2.2	2.86	kΩ
$I_{i(op)(RHV)}$	operating range of the input current at pin RHV	note 9	0	–	1000	μA
f_{ff}	feedforward frequency	I_{RHV} = 0.75 mA	60.4	63.6	66.15	kHz
		I_{RHV} = 1 mA	80.3	84.5	88.2	kHz
SYM_{ff}	symmetry	I_{RHV} = 1 mA; note 10	0.9	1.0	1.1	μA
RR	ripple rejection	f_{Vin} = 100 Hz	–	6	–	dB
$R_{s(CP)}$	CP switch series resistance	I_{CP} = 100 μA	0.75	1.5	2.25	kΩ
R_{AV}	averaging resistor	I_{CP} = 10 μA	22.4	32	41.6	kΩ

Notes

1. The start-up supply current is specified in a temperature (T_{vj}) range of 0 to 125 °C. For T_{vj} <0 and T_{vj} >125 °C the start-up supply current is <350 μA.
2. The clamp margin is defined as the voltage difference between turn-on of the clamp and start of oscillation. The clamp is in the off-state at start of oscillation.
3. Data sampling of $V_{RS(cap)}$ is performed at the end of conduction of T2.
4. The total supply current is specified in a temperature (T_{vj}) range of –20 to +125 °C. For T_{vj} < –20 and T_{vj} > 125 °C the total supply current is <1.5 mA.
5. Data sampling of $V_{RS(cap)}$ is performed at the start of conduction of T2.
6. Within the allowed range of R_{ref}, defined as 30 kΩ ±10%.
7. For $V_{(FS-S1)}$ = 11 V.
8. Typical values for the on and off resistances at T_{vj} = 87.5 °C are: $R_{on(VS)}$ and $R_{on(FS)}$ = 164 Ω, $R_{off(VS)}$ and $R_{off(FS)}$ = 100 Ω.
9. The input current at pin RHV may increase to 1600 μA during voltage transient at V_{in}. Only for currents I_{RHV} beyond approximately 550 μA is the oscillator frequency proportional to I_{RHV}.
10. The symmetry SYM_{ff} is calculated from the quotient $SYM_{ff} = T1_{tot}/T2_{tot}$, with $T1_{tot}$ the time between turn-off of G2 and turn-off of G1, and $T2_{tot}$ the time between turn-off of G1 and turn-off of G2.

DESIGN EQUATIONS

- Bottom frequency: $f_B = \frac{1}{2 \times [(C_f + C_{par}) \times (X1 \times R_{ref} - R_{int})] + \tau}$ (Hz)
- Feedforward frequency: $f_{ff} = \frac{1}{2 \times \left[(C_f + C_{par}) \times \left(\frac{X2 \times V_{ref}}{I_{RHV}} - R_{int}\right)\right] + \tau}$ (Hz)

  Where:
  - $X1 = 3.68$
  - $X2 = 22.28$
  - $\tau = 0.4\ \mu s$
  - $R_{int} = 3\ k\Omega$
  - $C_{par} = 4.7\ pF$.
- Operating frequency = $f_{B(max)}$, $f_{ff(max)}$ and $f_{cm(max)}$

  Where:
  - f_B = bottom frequency
  - $f_{ff(max)}$ = maximum feedforward frequency
  - $f_{cm(max)}$ = maximum frequency due to capacitive mode detection.
- Preheat time: $t_{ph} = \frac{C_{par}}{150\ nF} \times \frac{R_{ref}}{30\ k\Omega}$ (s)
- Ignition time: $t_{ign} = \frac{15}{16} \times t_{ph}$ (s)
- Non-overlap time: $t_{no} = 1.4\ \mu s \times \frac{R_{ref}}{30\ k\Omega}$

APPLICATION INFORMATION

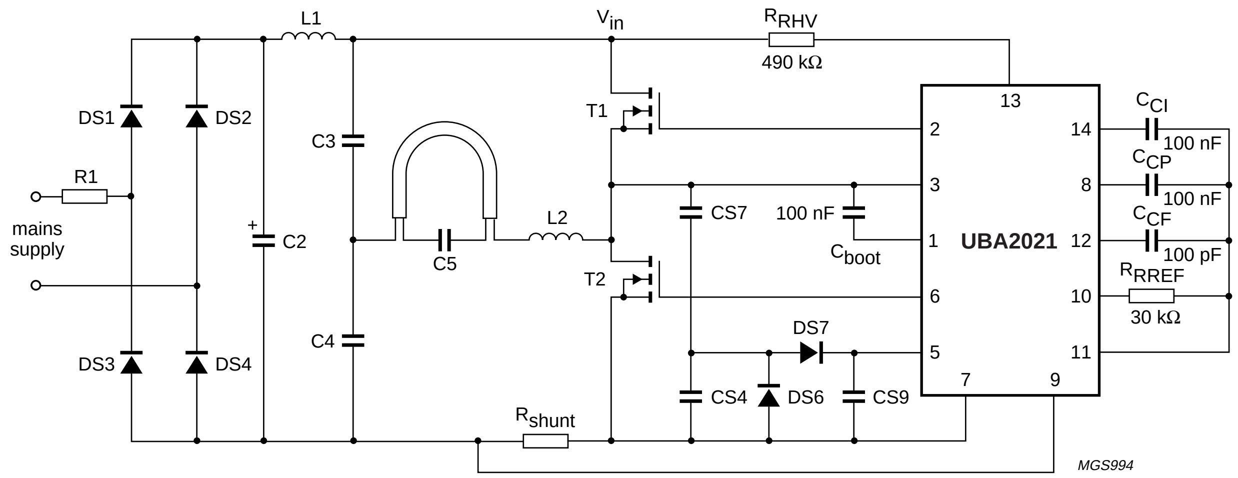
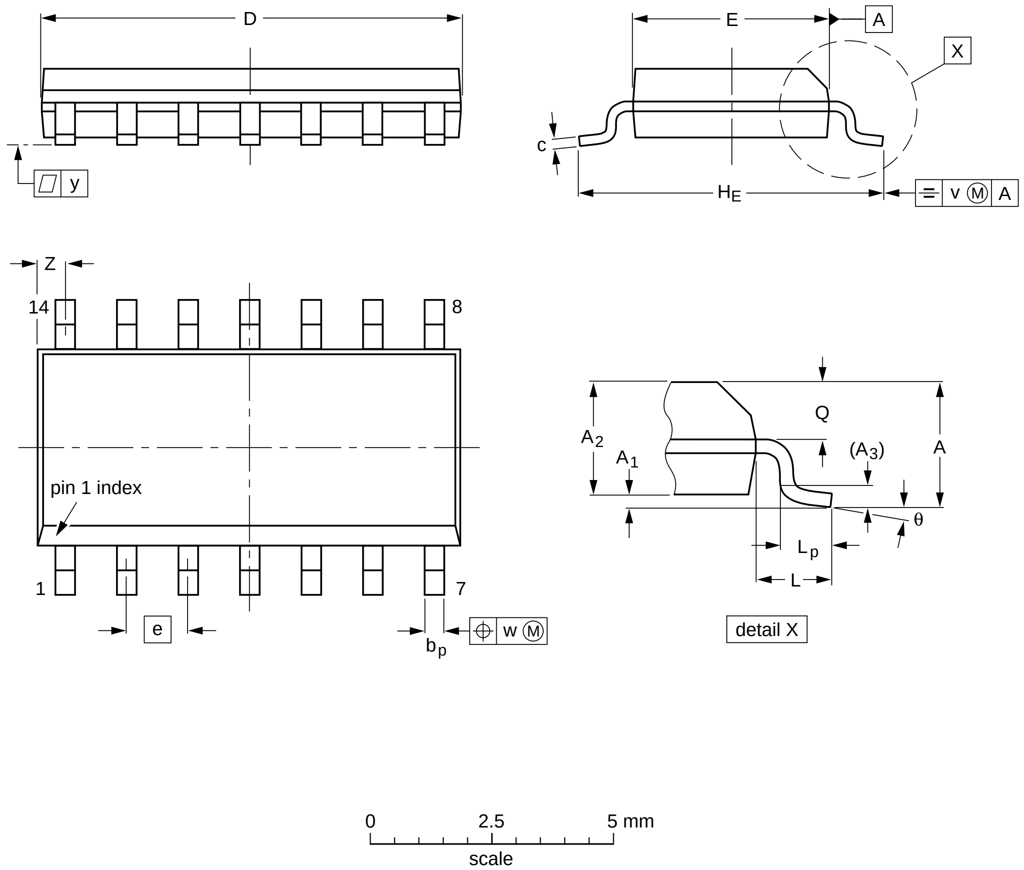


Fig.7 Application diagram.

PACKAGE OUTLINES

SO14: plastic small outline package; 14 leads; body width 3.9 mm SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

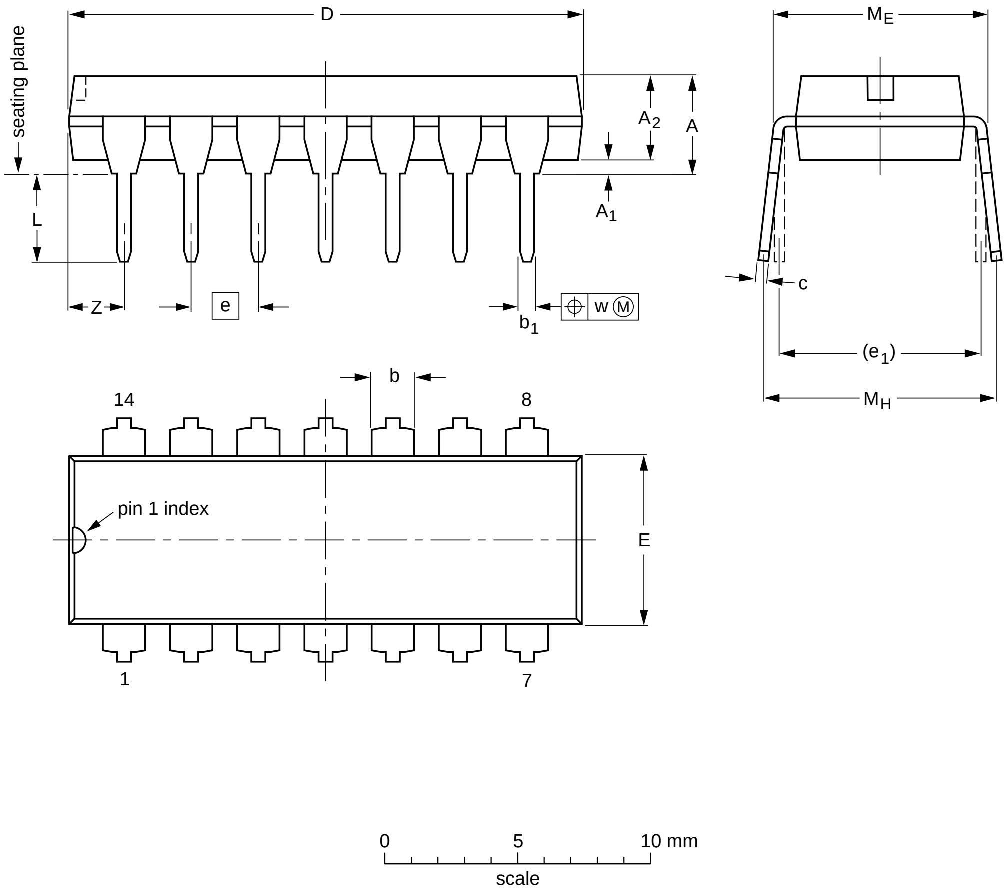
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06	MS-012				~~97-05-22~~ 99-12-27

DIP14: plastic dual in-line package; 14 leads (300 mil) SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001	SC-501-14			~~95-03-11~~ 99-12-27

SOLDERING

Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Through-hole mount packages

SOLDERING BY DIPPING OR BY SOLDER WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

MANUAL SOLDERING

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Surface mount packages

REFLOW SOLDERING

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

WAVE SOLDERING

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

MANUAL SOLDERING

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of IC packages for wave, reflow and dipping soldering methods

MOUNTING	PACKAGE	SOLDERING METHOD		
		WAVE	REFLOW(1)	DIPPING
Through-hole mount	DBS, DIP, HDIP, SDIP, SIL	suitable(2)	–	suitable
Surface mount	BGA, LFBGA, SQFP, TFBGA	not suitable	suitable	–
	HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(3)	suitable	–
	PLCC(4), SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended(4)(5)	suitable	–
	SSOP, TSSOP, VSO	not recommended(6)	suitable	–

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *“Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”*.
2. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
3. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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