2 GHz image rejecting front-end UAA2077BM

FEATURES

- Low-noise, wide dynamic range amplifier
- Very low noise figure
- Dual balanced mixer for over 25 dB on-chip image rejection
- IF I/Q combiner at 188 MHz
- On-chip quadrature network
- Down-conversion mixer for closed-loop transmitters
- Independent TX/RX fast ON/OFF power-down modes
- Very small outline packaging
- Very small application (no image filter).

APPLICATIONS

- 1800 MHz front-end for DCS1800 hand-portable equipment
- Compact digital mobile communication equipment
- TDMA receivers e.g. PCS, RF-LANS.

GENERAL DESCRIPTION

UAA2077BM contains both a receiver front-end and a high frequency transmit mixer intended to be used in mobile telephones. Designed in an advanced BiCMOS process it combines high performance with low power consumption and a high degree of integration, thus reducing external component costs and total front-end size.

The main advantage of the UAA2077BM is its ability to provide over 25 dB of image rejection. Consequently, the image filter between the LNA and the mixer is suppressed.

Image rejection is achieved in the internal architecture by two RF mixers in quadrature and two all-pass filters in I and Q IF channels that phase shift the IF by 45° and 135° respectively. The two phase shifted IFs are recombined and buffered to furnish the IF output signal.

For instance, signals presented at the RF input at LO + IF frequency are rejected through this signal processing while signals at LO – IF frequency can form the IF signal. An internal switch allows the use of infradyne (LO < RF) or supradyne (LO > RF) reception.

The receiver section consists of a low-noise amplifier that drives a quadrature mixer pair. The IF amplifier has on-chip 45° and 135° phase shifting and a combining network for image rejection. The IF driver has differential open-collector type outputs.

The LO part consists of an internal all-pass type phase shifter to provide quadrature LO signals to the receive mixers.The centre frequency of the phase shifter is adjustable for maximum image rejection in a given band. The all-pass filters outputs are buffered before being fed to the receive mixers.

The transmit section consists of a low-noise amplifier, and a down-conversion mixer. In the transmit mode an internal LO buffer is used to drive the transmit IF down-conversion mixer.

All RF and IF inputs or outputs are balanced.

Pins RXON, TXON and SXON allow a selection of whether to reject the upper or lower image frequency and control of the different power-down modes. Special care has been taken for fast power-up switching.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	3.6	4.0	5.3	V
I_{CCRX}	receive supply current	22	27	33	mA
I_{CCTX}	transmit supply current	11	14	17	mA
I_{CCPD}	supply current in power-down	–	–	50	µA
T_{amb}	operating ambient temperature	–30	+25	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA2077BM	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

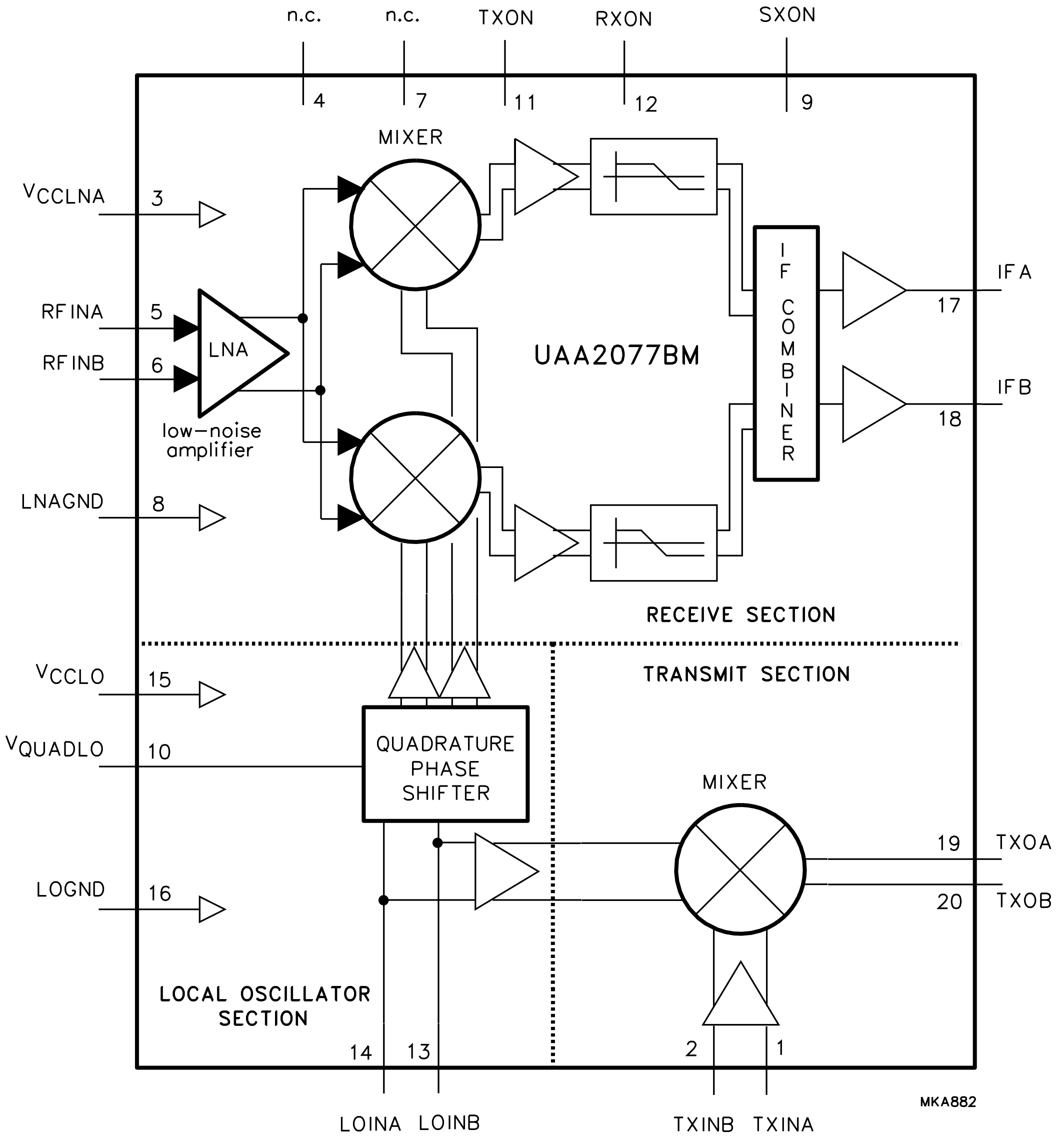

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
TXINA	1	transmit mixer input A (balanced)
TXINB	2	transmit mixer input B (balanced)
V_{CCLNA}	3	supply voltage for LNA, IF parts and TX mixer
n.c.	4	not connected
RFINA	5	RF input A (balanced)
RFINB	6	RF input B (balanced)
n.c.	7	not connected
LNAGND	8	ground for LNA and IF parts
SXON	9	synthesizer-ON mode enable
V_{QUADLO}	10	input voltage for LO quadrature trimming
TXON	11	transmit mode enable
RXON	12	receive mode enable
LOINB	13	LO input B (balanced)
LOINA	14	LO input A (balanced)
V_{CCLO}	15	supply voltage for LO parts
LOGND	16	ground for LO parts
IFA	17	IF output A (balanced)
IFB	18	IF output B (balanced)
TXOA	19	transmit mixer IF output A (balanced)
TXOB	20	transmit mixer IF output B (balanced)

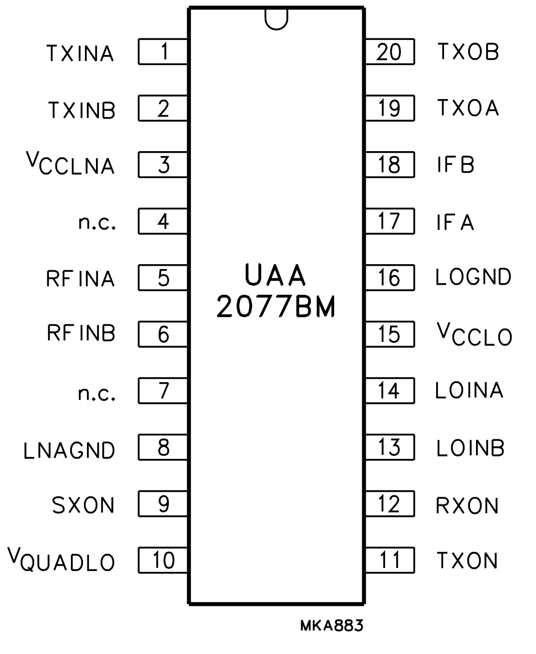

Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Receive section

The circuit contains a low-noise amplifier followed by two high dynamic range mixers. These mixers are of the Gilbert-cell type, the whole internal architecture is fully differential.

The local oscillator, shifted in phase to 45° and 135°, mixes the amplified RF to create I and Q channels. The two I and Q channels are buffered, phase shifted by 45° and 135° respectively, amplified and recombined internally to realize the image rejection.

Balanced signal interfaces are used for minimizing crosstalk due to package parasitics. The RF differential input impedance is 35 Ω (real part).

The IF output is differential and of the open-collector type. Typical application will load the output with a differential 1 kΩ load; i.e. a 1 kΩ resistor load at each IF output, plus a 2 kΩ to x Ω narrow band matching network (x Ω being the input impedance of the IF filter). The path to V_{CC} for the DC current is achieved via tuning inductors. The output voltage is limited to V_{CC} + $3V_{be}$ or 3 diode forward voltage drops.

Fast switching, ON/OFF, of the receive section is controlled by the hardware input RXON.

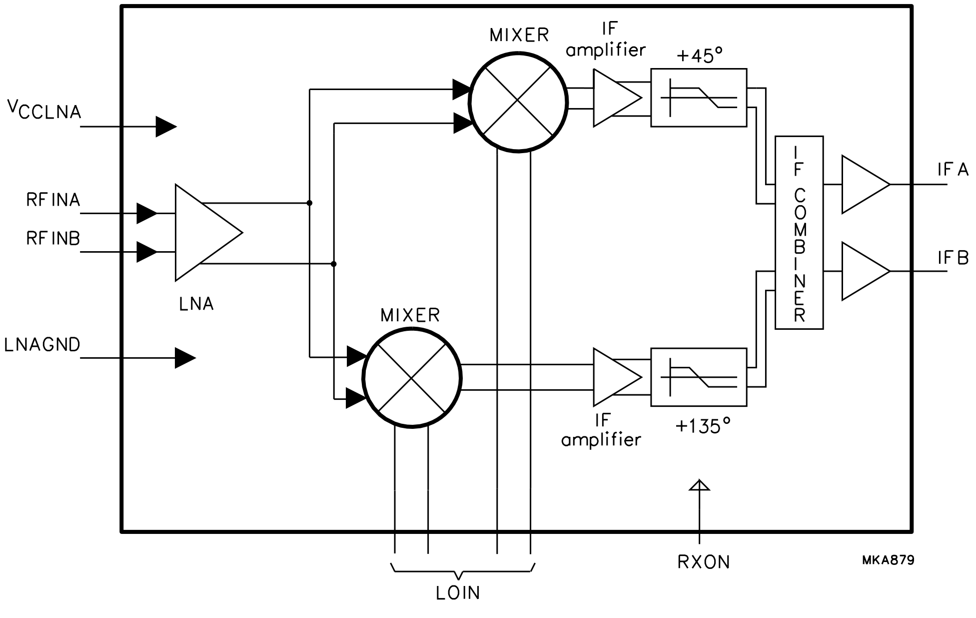

Fig.3 Block diagram, receive section.

Local oscillator section

The local oscillator (LO) input directly drives the two internal all-pass networks to provide quadrature LO to the receive mixers.

The centre frequency of the receive band is adjustable by the voltage on pin V_{QUADLO}. This should be done by connecting a resistor between V_{QUADLO} and V_{CC}. Over 25 dB of image rejection can be obtained by an optimum resistor value.

The LO differential input impedance is 35 Ω (real part). A synthesizer-ON mode is used to power-up all LO input buffers, thus minimizing the pulling effect on the external VCO when entering receive or transmit mode. This mode is active when SXON = 1.

Transmit mixer

This mixer is used for down-conversion to the transmit IF. Its inputs are coupled to the transmit RF which is down-converted to a modulated transmit IF frequency, phase locked with the baseband modulation.

The transmit mixer provides a differential input at 40 Ω and a differential HIGH impedance output. The IF outputs are HIGH impedance (open-collector type); i.e. a 500 Ω resistor load at each IF output, plus a 1 kΩ to x Ω narrow band matching network (x Ω being the input impedance of the IF filter). The mixer can also be used for frequency up-conversion.

Fast switching, ON/OFF, of the transmit section is controlled by the hardware input TXON.

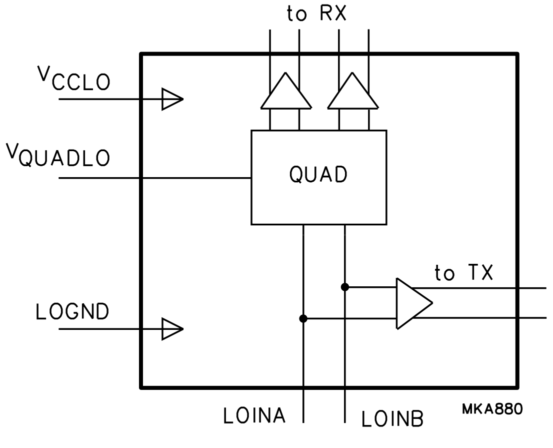

Fig.4 Block diagram, LO section.

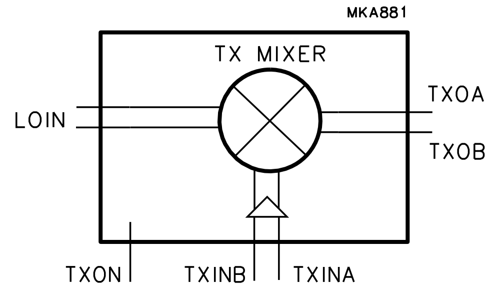

Fig.5 Block diagram, transmit mixer.

Table 1 Control of power status

EXTERNAL PIN LEVEL			CIRCUIT MODE OF OPERATION
TXON	RXON	SXON	
LOW	LOW	LOW	power-down mode
LOW	HIGH	LOW	receive section on, infradyne reception
HIGH	LOW	LOW	transmit section on
LOW	LOW	HIGH	synthesizer-ON mode (only LO buffers enabled)
LOW	HIGH	HIGH	receive section on and synthesizer-ON mode active, infradyne reception
HIGH	LOW	HIGH	transmit section on and synthesizer-ON mode active
HIGH	HIGH	LOW	receive section on, supradyne reception
HIGH	HIGH	HIGH	receive section on and synthesizer-ON mode active, supradyne reception

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–	9	V
ΔGND	difference in ground supply voltage applied between LOGND and LNAGND	–	0.6	V
$P_{I(max)}$	maximum power input	–	+20	dBm
$T_{j(max)}$	maximum operating junction temperature	–	+150	°C
$P_{dis(max)}$	maximum power dissipation in quiet air	–	250	mW
T_{stg}	storage temperature	–65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

HANDLING

Every pin withstands 1500 V ESD Human Model and 200 V Machine Model; refer to MIL-STD-883C class 2 (method 3015.5).

DC CHARACTERISTICS

V_{CC} = 4 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins: V_{CCLNA}, V_{CCLO}						
V_{CC}	supply voltage	over full temperature range	3.6	4.0	5.3	V
$I_{CC(RX)}$	supply current	receive mode active; DC tested	22	27	33	mA
$I_{CC(TX)}$	supply current	transmit mode active; DC tested	11	14	17	mA
$I_{CC(PD)}$	supply current in power-down mode	DC tested	–	–	50	μA
$I_{CC(SX)}$	supply current	synthesizer-ON mode only	6	7.5	9	mA
$I_{CC(SRX)}$	supply current	receive and synthesizer-ON mode active	–	29	–	mA
$I_{CC(STX)}$	supply current	transmit and synthesizer-ON mode active	–	18	–	mA
Pins: RXON, TXON and SXON						
V_{th}	CMOS threshold voltage	note 1	–	1.25	–	V
V_{IH}	HIGH level input voltage		$0.7V_{CC}$	–	V_{CC}	V
V_{IL}	LOW level input voltage		–0.3	–	0.8	V
I_{IH}	HIGH level static input current	pins at V_{CC} – 0.4 V	–1	–	+1	μA
I_{IL}	LOW level static input current	pins at 0.4 V	–1	–	+1	μA
Pins: RFINA and RFINB						
V_I	DC input voltage level	receive mode enabled	–	2.0	–	V
Pins: IFA and IFB						
I_O	DC output current	receive mode enabled	–	2.5	–	mA
Pins: TXINA and TXINB						
V_I	DC input voltage level	transmit section enabled	–	2.0	–	V
Pins: TXOA and TXOB						
I_O	DC output current	transmit section enabled	–	0.9	–	mA
Pins: LOINA and LOINB						
V_{LOIN}	DC input voltage level	RXON, TXON or SXON HIGH	–	3.3	–	V

Note

1. The referenced inputs should be connected to a valid CMOS input level.

AC CHARACTERISTICS

V_{CC} = 4 V; T_{amb} = –30 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receive section (receive section enabled)						
Z_{RFI}	RF input impedance (real part)	balanced; at 1850 MHz	–	35	–	Ω
f_{RFI}	RF input frequency		1800	–	2000	MHz
RL_{RF}	return loss on matched RF input	balanced; note 1	11	15	–	dB
G_{CP}	conversion power gain	differential RF inputs to differential IF outputs loaded to 1 kΩ differential	17	20	23	dB
G_{rip}	gain ripple as a function of RF frequency	between 1805 and 1880 MHz; note 2	–	0.1	–	dB
ΔG/T	gain variation with temperature	note 2	–15	–10	–5	mdB/K
$CP1_{RX}$	1 dB compression point	differential RF inputs to differential IF outputs; note 1	–26	–23	–	dBm
DES3	3 dB desensitisation point	interferer frequency offset: 3 MHz; differential RF inputs to differential IF outputs; note 1	–	–30	–	dBm
		interferer frequency offset: 20 MHz; differential RF inputs to differential IF outputs; note 1	–	–27	–	dBm
$IP2D_{RX}$	2nd order intercept point	differential RF inputs to differential IF outputs; note 2	+15	+22	–	dBm
$IP3_{RX}$	3rd order intercept point	differential RF inputs to differential IF outputs; note 2	–23	–17	–	dBm
NF_{RX}	overall noise figure	differential RF inputs to differential IF outputs; notes 2 and 3	–	4.3	5.0	dB
$Z_{L(IF)}$	typical application IF output load impedance	balanced	–	1	–	kΩ
RL_{IF}	return loss on matched IF input	balanced; note 1	11	15	–	dB
f_{IF}	IF frequency range		170	188	210	MHz
IR	rejection of image frequency	V_{QUADLO} tuned	20	–	–	dB
		infradyne; f_{IF} = 188 MHz; note 4	25	32	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Local oscillator section (receive section enabled)						
f_{LO}	LO input frequency		1600	–	2200	MHz
Z_{LO}	LO input impedance (real part)	balanced	–	35	–	Ω
RL_{LO}	return loss on matched input (including standby mode)	note 1	9	12	–	dB
ΔRL_{LO}	return loss variation between SX, SRX and STX modes	linear S_{11} variation; note 1	–		–	mU
$P_{i(LO)}$	LO input power level		–6	–3	+3	dBm
RI_{LO}	reverse isolation	LOIN to RFIN at LO frequency; note 1	40	–	–	dB
R_{tune}	image rejection tuning resistor	connected between V_{QUADLO} and V_{CC}	0	1000	–	Ω
Transmit section (transmit section enabled)						
Z_L	TX IF typical load impedance		–	500	–	Ω
RL_{TXIF}	return loss on matched transmitter IF input		11	15	–	dB
$Z_{i(RF)}$	TX RF input impedance (real part)	balanced; at 1750 MHz	–	40	–	Ω
f_{TXmix}	TX mixer input frequency		1600	–	2000	MHz
RL_{TX}	return loss on matched TX input	note 1	10	15	–	dB
G_{CP}	conversion power gain	differential transmitter inputs to differential transmitter IF outputs loaded with 500 Ω differential	6	9	12	dB
$f_{o(TX)}$	TX mixer output frequency		50	–	400	MHz
$CP1_{TX}$	1 dB input compression point		–25	–22	–	dBm
$IP2_{TX}$	2nd order intercept point		–	+22	–	dBm
$IP3_{TX}$	3rd order intercept point		–19	–16	–	dBm
NF_{TX}	noise figure	double sideband; notes 2 and 3	–	6	9	dB
I_{TX}	isolation	LOIN to TXIN; note 1	40	–	–	dB
RI_{TX}	reverse isolation	TXIN to LOIN; note 1	40	–	–	dB
Timing						
t_{stu}	start-up time of each block		1	5	20	µs

Notes

1. Measured and guaranteed only on UAA2077BM demonstration board at T_{amb} = +25 °C.
2. Measured and guaranteed only on UAA2077BM demonstration board.
3. This value includes printed-circuit board and balun losses.
4. Measured and guaranteed only on UAA2077BM demonstration board at T_{amb} = +25 °C, with a 1 kΩ resistor between V_{QUADLO} and V_{CC}.

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APPLICATION INFORMATION

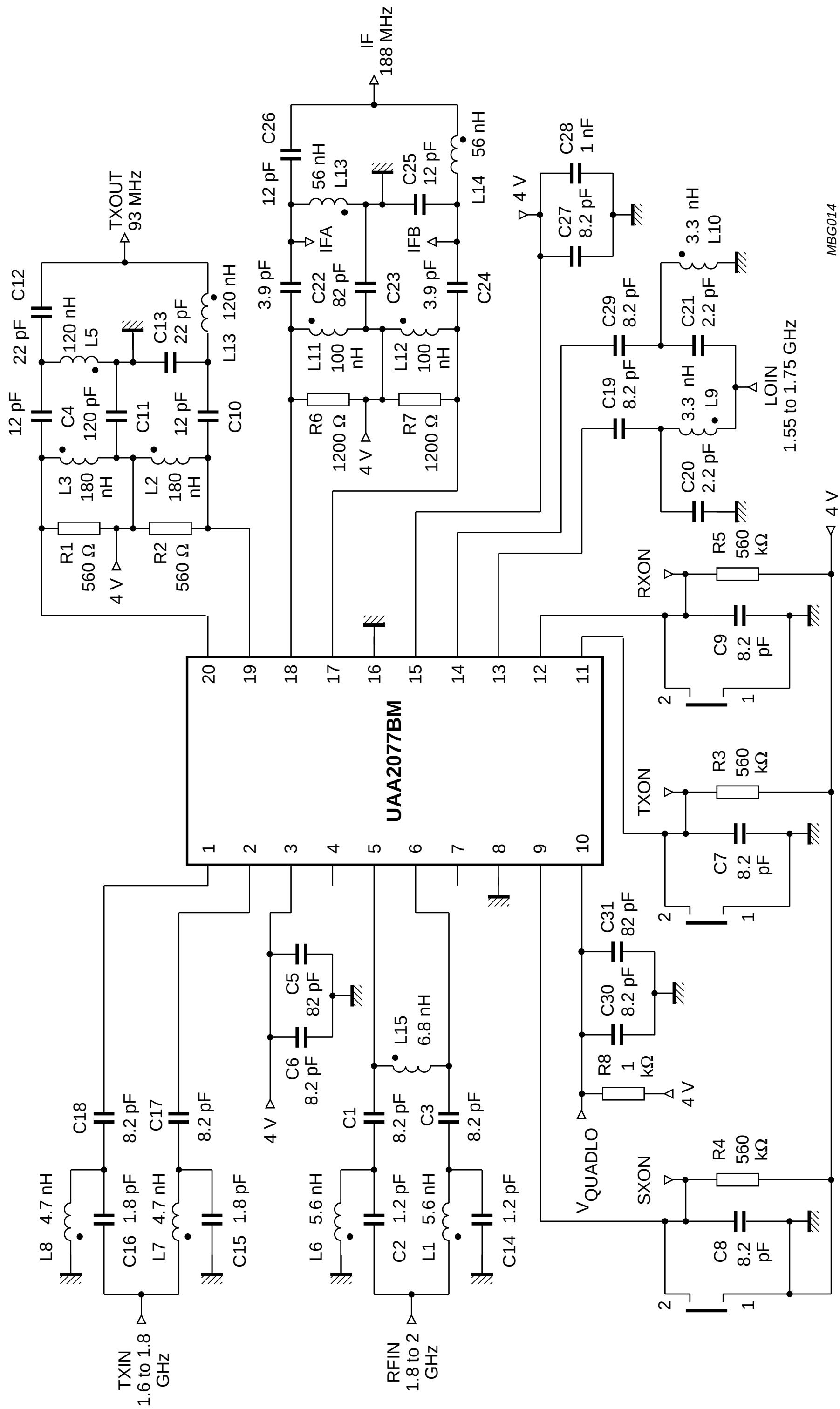

Figure 6 illustrates the electrical diagram of the UAA2077BM Philips demonstration board for DCS1800 applications.
For measurement purposes all matching is to 50 Ω. Different values will be used in a real application.

Fig.6 Application diagram.