Image reject 1800 MHz transceiver for DECT applications

UAA2067G

FEATURES

- Receiver with:
  - low noise amplifier
  - dual quadrature mixers for image rejection (lower sideband)
  - I and Q combining networks at a fixed IF
- Both high-frequency and low-frequency VCOs including buffers with good isolation for low pulling
- Transmitter with:
  - dual quadrature mixers for image rejection (lower sideband)
  - amplitude ramping circuit
  - amplifier with high output power.

APPLICATIONS

- 1800 MHz transceiver for DECT hand-portable equipment
- TDMA systems.

GENERAL DESCRIPTION

The UAA2067G is a low-power transceiver intended for use in portable and base station transceivers complying with the DECT system. The IC performs in accordance with specifications in the –30 to +85°C temperature range.

The UAA2067G contains a front-end receiver for the 1800 to 1900 MHz frequency range, a high-frequency VCO for the 1700 to 1800 MHz range, a low-frequency VCO for the 110 to 140 MHz frequency range and a transmitter with a high-output power amplifier driver stage for the 1800 to 1900 MHz frequency range. Designed in an advanced BiCMOS process, it combines high performance with low-power consumption and a high degree of integration, thus reducing external component costs and total radio size.

Its first advantage is to provide typically 34 dB of image rejection in the receiver path. Thus, the image filter between the LNA and the mixer is redundant and consequently can be removed. The receiver section consists of a low-noise amplifier that drives a quadrature mixer pair. Image rejection is achieved by this RF mixer pair and the two phase shifters in the I and Q channels that phase shift the IF by 45° and 135° respectively. The two phase shifted IFs are recombined and buffered to furnish the IF output signal.

Signals presented at the RF input at LO − IF frequency are rejected through this signal processing while signals at LO + IF frequency can form the IF signal.

Its second advantage is to provide a good buffered high-frequency VCO signal to the RX and TX mixers and to the synthesizer-prescaler. Switching the receiver or transmitter section **on** gives a very small change in VCO frequency.

Its third advantage is to provide a good buffered low-frequency VCO signal to the TX mixers, to the synthesizer-prescaler and the second down conversion mixer in a double conversion receiver. Switching the transmitter section **on** gives a very small change in VCO frequency.

The frequency of each VCO is determined by a resonator network that is external to the IC. Each VCO has a regulated power supply voltage that has been designed specifically for minimizing a change in frequency due to changes in the power supply voltage, which may be caused for instance by switching **on** the power amplifier.

Its fourth advantage is to provide typically 33 dBc of image rejection in the single-sideband up-conversion mixer. Thus the image filter between the preamplifier and the antenna is redundant and may consequently be removed. Image rejection is achieved in the internal architecture by two RF mixers in quadrature and two phase shifters in the low-frequency VCO signal that shifts the phase to 0° and 90°. The output signals of the mixers are summed to form the single-upper-sideband output signal.

The output stage is a high-level output buffer with an output power of approximately 4 dBm. The output level is sufficient to drive a three-stage bipolar preamplifier for DECT.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA2067G	LQFP32	plastic low profile quad flat package; 32 leads; body 5 × 5 × 1.4 mm	SOT401-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	3.0	3.6	5.5	V
$I_{CC(RX)}$	receive supply current	–	24	–	mA
$I_{CC(TX)}$	transmit supply current	–	42	–	mA
$I_{CC(RFLO)}$	RF oscillator supply current	–	15	–	mA
$I_{CC(IFLO)}$	IF oscillator supply current	–	7	–	mA
NF_{RX}	receive noise figure	–	–	7.0	dB
G_{CP}	conversion power gain	–	30	–	dB
IR_{RX}	receive image frequency rejection	–	34	–	dB
f_{RFLO}	RFLO frequency range	1.7	–	1.8	GHz
f_{IFLO}	IFLO frequency range	110	–	140	MHz
P_{out}	output transmit power	–	4	–	dBm
IR_{TX}	transmit image frequency rejection	–	33	–	dBc
T_{amb}	operating ambient temperature	–30	+25	+85	°C

BLOCK DIAGRAM

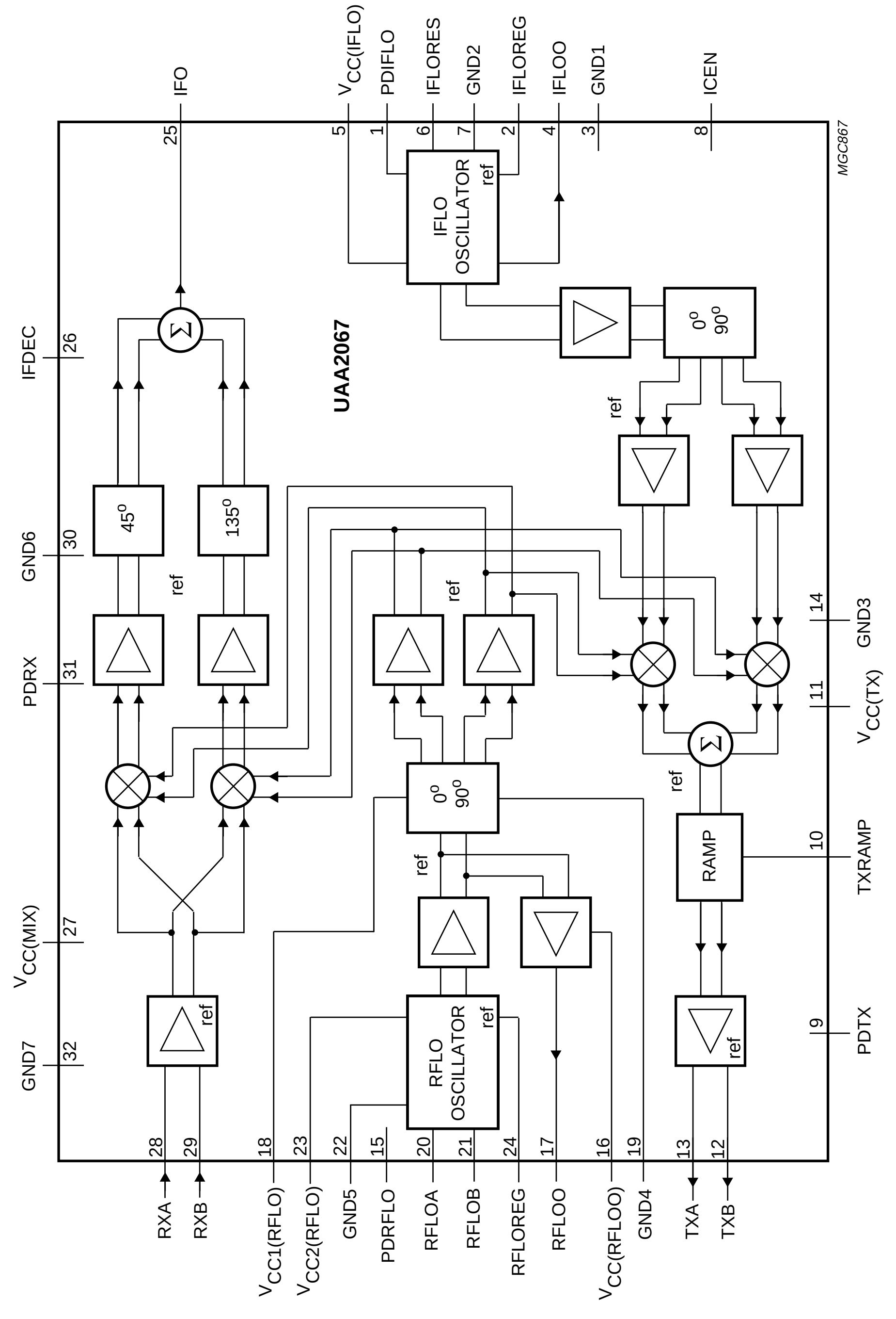

Fig.1 Block diagram

PINNING

SYMBOL	PIN	DESCRIPTION
PDIFLO	1	power-down for IFLO
IFLOREG	2	regulator decoupling for IFLO
GND1	3	ground for IFLO; note 1
IFLOO	4	IFLO output
$V_{CC(IFLO)}$	5	supply voltage for IFLO
IFLORES	6	IFLO resonator
GND2	7	ground for IFLO resonator; note 1
ICEN	8	IC enable
PDTX	9	power-down for transmitter
TXRAMP	10	power ramping transmitter
$V_{CC(TX)}$	11	supply voltage for transmitter output stage
TXB	12	transmitter RF output B
TXA	13	transmitter RF output A
GND3	14	ground for transmitter output stage
PDRFLO	15	power-down for RFLO
$V_{CC(RFLOO)}$	16	supply voltage for RFLO output
RFLOO	17	RFLO output
$V_{CC1(RFLO)}$	18	supply voltage for RFLO oscillator; note 2
GND4	19	ground for RFLO oscillator; note 3
RFLOA	20	RFLO resonator
RFLOB	21	RFLO resonator
GND5	22	ground for RFLO oscillator; note 3
$V_{CC2(RFLO)}$	23	supply voltage for RFLO oscillator; note 2
RFLOREG	24	regulator decoupling for RFLO
IFO	25	receiver IF output
IFDEC	26	IF decoupling
$V_{CC(MIX)}$	27	supply voltage for receiver and transmit mixers
RXA	28	receiver RF input A
RXB	29	receiver RF input B
GND6	30	ground for receiver and transmit mixers
PDRX	31	power-down for receiver
GND7	32	die-pad ground

Notes

1. Pins 3 and 7 are internally connected.
2. Pins 18 and 23 are internally connected.
3. Pins 19 and 22 are internally connected.

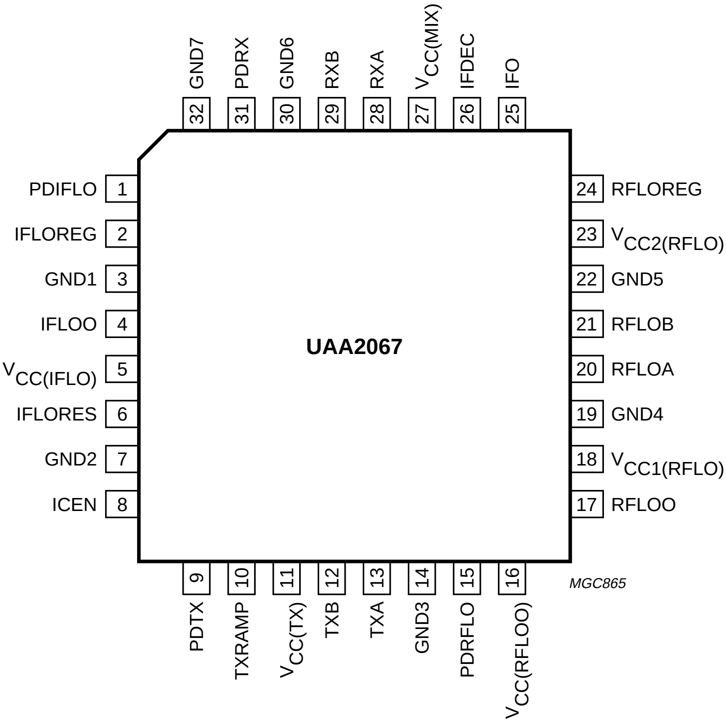

Fig.2 Pin configuration

FUNCTIONAL DESCRIPTION

Receive section

The circuit contains a balanced low-noise amplifier followed by two high dynamic range mixers. The local oscillator signals, shifted in phase to 0 and 90° mix the amplified RF signal to the I and Q channels.These two channels are buffered, phase shifted by 45° and 135° respectively, amplified and recombined internally to realize the image rejection. Signals at the RF input at RFLO – IF frequencies are rejected through the signal processing while signals at the RFLO + IF frequencies form the IF signals.

An image rejection of typically 34 dB is obtained for an IF between 100 and 120 MHz.

Balanced signals are used for minimizing crosstalk due to package parasitics. The IF output is single-ended. The typical load is 50 Ω.

Fast switching, **on/off** of the receive section is controlled by the hardware input PDRX.

RFLO section

The high-frequency oscillator (RFLO oscillator) supplies the local oscillator signal for the down-conversion (receive) and up-conversion (transmit) mixers. This VCO uses an on-chip regulator for a power-supply voltage-independent output frequency. The buffered VCO signal is fed into a phase shifter and an off-chip prescaler-synthesizer. The output signal of the phase-shifter is used for driving the RX and TX mixers. Due to the good isolation in the buffer stages, a very small change in VCO frequency is obtained when switching the RX and TX mixers **on**.

Fast switching, **on/off** of the oscillator section is controlled by the hardware input PDRFLO.

IFLO section

The low-frequency oscillator (IFLO oscillator) internally supplies the local oscillator signal to the single-sideband transmit mixer. The buffered VCO signal is fed into a phase shifter. The output signal of the phase-shifter is used for driving the TX mixers and the off-chip prescaler-synthesizer and second down-conversion mixer.

Due to the good isolation in the buffer stages, a very small change in VCO frequency is obtained when switching the TX mixer **on**.

Fast switching **on/off** of the oscillator section is controlled by the hardware input PDIFLO input.

Transmit mixer

The circuit contains two balanced mixers, each of which is driven by the RFLO and IFLO signals. The output signal of the two mixers is summed and buffered to obtain the single upper-sideband signal at frequency RFLO + IFLO.

With the use of an off-chip time constant, the ramping circuit defines the power ramp-up and ramp-down of the pre-amplifier output signal.

Balanced signals are used for minimizing crosstalk due to package parasitics.

Fast switching, **on/off**, of the transmit section is controlled by the hardware input PDTX.

The power supply voltage of the transmit mixers, the adding circuit and ramping circuit is taken from the $V_{CC(MIX)}$ and GND6 for maximum isolation from the preamplifier output stage.

OPERATING MODES

To use the IC, **all** V_{CC} pins must be connected to the supply voltage.

For transceiving a DECT signal, the RFLO and IFLO sections should be powered-on. After a stable frequency has been reached (mainly determined by the synthesizer design), the receiver or transmitter can be powered-on.

GMSK data modulation can be supplied in two different ways: the data is directly modulated on IFLO or RFLO.

The ramping of the power level can be set with a time constant that is external to the IC.

Table 1 gives the definition of the polarity of the switching signals on the receiver, the RFLO, the IFLO and the transmitter sections.

Table 1 Switching signals on the receiver

SIGNAL	SECTION	LEVEL	on/off
PDRX	receiver section powered-on	LOW	on(1)
	receiver section powered-off	HIGH	off
PDRFLO	RFLO section powered-on	LOW	on(1)
	RFLO section powered-off	HIGH	off
PDIFLO	IFLO section powered-on	LOW	on(1)
	IFLO section powered-off	HIGH	off
PDTX	transmitter section powered-on	LOW	on(1)
	transmitter section powered-off	HIGH	off
ICEN	all sections disabled	LOW	off
	all sections enabled	HIGH	on

Note

1. Active when ICEN is enabled.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–	6	V
ΔGND	difference in ground supply voltage applied between all grounds	–	0.6	V
$P_{I(max)}$	maximum power input	–	+20	dBm
$T_{j(max)}$	maximum operating junction temperature	–	+150	°C
$P_{dis(max)}$	maximum power dissipation in stagnant air at 25°C	–	500	mW
T_{stg}	storage temperature	–65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	90	K/W

HANDLING

Every pin withstands the ESD test in accordance with *“MIL-STD-883C class 2 (method 3015.5)”*.

DC CHARACTERISTICS

V_{CC} = 3.6 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins: $V_{CC(MIX)}$, $V_{CC(TX)}$, $V_{CC(IFLO)}$, $V_{CC1(RFLO)}$, $V_{CC2(RFLO)}$ and $V_{CC(RFLOO)}$						
V_{CC}	supply voltage	over full temperature range	3.0	3.6	5.5	V
$I_{CC(RX)}$	supply current	receiver section **on**; DC tested	18	24	30	mA
$I_{CC(RFLO)}$	supply current RFLO	RFLO section **on**; DC tested	11	15	20	mA
$I_{CC(IFLO)}$	supply current IFLO	IFLO section **on**; DC tested	5	7	9	mA
$I_{CC(TX)}$	supply current	transmitter section **on**; DC tested	34	42	54	mA
$I_{CC(PD)}$	supply current	power-down mode; DC tested	–	2	50	μA
Pins: PDRX, PDTX, PDRFLO, PDIFLO and ICEN						
V_{IH}	HIGH level input voltage		2.1	–	V_{CC} + 0.3	V
V_{IL}	LOW level input voltage		–0.3	–	0.8	V
I_{IH}	HIGH level static input current	pin at V_{CC} – 0.4 V	–1	–	+1	μA
I_{IL}	LOW level static input current	pin at 0.4 V	–1	–	+1	μA
Pins: RXA, RXB, IFO and IFDEC						
$V_{RXA,B}$	DC input voltage level	receiver section **on**	2.1	2.4	2.7	V
V_{IFO}	DC output voltage level	receiver section **on**	0.9	1.1	1.3	V
V_{IFDEC}	DC level	receiver section **on**	2.45	2.65	2.85	V
Pins: RFLOA, RFLOB, RFLOREG and RFLOO						
$I_{RFLOA,B}$	DC current	RFLO section **on**	1	2	3	mA
$V_{RFLOREG}$	DC level	RFLO section **on**	2.45	2.65	2.85	V
V_{RFLOO}	DC output voltage level	RFLO section **on**	2.8	3.1	3.4	V
Pins: IFLORES, IFLOREG and IFLOO						
$V_{IFLORES}$	DC level	IFLO section **on**	1.85	2.1	2.3	V
$V_{IFLOREG}$	DC level	IFLO section **on**	2.35	2.55	2.8	V
V_{IFLOO}	DC output voltage level	IFLO section **on**	2.2	2.45	2.7	V
Pins: TXA, TXB and TXRAMP						
$I_{TXA,B}$	DC output current	transmitter section **on**	2	10	18	mA
I_{TXRAMP}	DC input current	V_{TXRAMP} = 3 V; transmitter section **on**	–	–	200	μA

AC CHARACTERISTICS

V_{CC} = 3.0 to 5.5 V; T_{amb} = –30 to +85°C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receive mode (receiver and RFLO sections powered-on)						
f_{RFI}	RF input frequency		1800	–	1900	MHz
Z_{RFI}	RF input impedance	note1	–	50	–	Ω
RL_{RF}	return loss on matched RF input	note 1	–	–20	–15	dB
$PRFLO_{RX}$	RFLO level at input to RX balun	note 1	–	–70	–40	dBm
$DES3_{RX}$	RF interference for 3 dB desensitization	interference frequency offset 6 MHz; note 1	–39	–35	–	dBm
G_{CP}	conversion power gain	RF input to IF output (typical load)	24	30	36	dB
$CP1_{RX}$	1 dB input compression point	referenced to RF input; note 1	–36	–33	–	dBm
$P_{o(RX)}$	IF power for $CP1_{RX} < P_{in} <$ +8 dBm	referenced to IF power at $CP1_{RX}$; note 1	–6	–	+6	dB
t_{rec}	recovery time for P_{in} = +12 dBm	note 1	–	2	30	µs
$IP2\text{-}2_{RX}$	mixer 2-2 spurious intercept point	referenced to the RF input; note 1	–6	+2	–	dBm
$IP3_{RX}$	3rd order intercept point	referenced to the RF input; note 1	–30	–26	–	dBm
NF_{RX}	overall noise figure	RF input to differential IF output; note 1	–	6.3	7	dB
f_{IF}	IF frequency range		100	110	120	MHz
$Z_{L(IF)}$	typical application IF output load impedance		–	50	–	Ω
RL_{IF}	return loss on matched IF output impedance	note 1	–	–20	–15	dB
IR_{RX}	image frequency rejection		20	34	–	dB
PSRR	power supply rejection ratio	note 1; typical load; at 110 MHz	35	–	–	dB
RF local oscillator (RFLO section powered-on)						
f_{RFLO}	oscillator frequency		1700	–	1800	MHz
$Z_{i(RFLO)}$	oscillator input impedance	balanced; at 1.77 GHz	–	–250	–	Ω
$V_{o(RFLO)}$	local oscillator output level; RMS value	note 2	50	75	–	mV
$Z_{o(RFLO)}$	local oscillator output impedance	at 1.77 GHz	–	30 – 60j	–	Ω
$R_{L(RFLO)}$	typical load resistance		–	300	–	Ω
$C_{L(RFLO)}$	typical load capacitance		–	2	–	pF
$HAR_{(RFLO)}$	harmonic levels at RFLO output	note 1	–	–	–20	dBc

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IF local oscillator (IFLO section powered-on)						
f_{IFLO}	oscillator frequency		110	120	140	MHz
$Z_{i(IFLO)}$	oscillator input impedance (real part)		–	–480	–	Ω
$V_{o\ IFLO}$	IF local oscillator output level; RMS value		100	160	–	mV
$Z_{o(IFLO)}$	local oscillator output impedance (real part)		–	–	100	Ω
$R_{L(IFLO)}$	typical load resistance		–	5	–	kΩ
$C_{L(IFLO)}$	typical load capacitance		–	7	–	pF
$HAR_{(IFLO)}$	harmonic levels at IFLO output	note 1	–	–	–15	dBc
Transmit mode (transmitter, RFLO and IFLO sections powered-on)						
f_{TX}	RF output frequency		1800	–	1900	MHz
$Z_{o(TX)}$	RF output impedance	balanced	–	50	–	Ω
RL_{TX}	return loss on matched RF output impedance	note 1	–	–20	–15	dB
$FTRFLO_{TX}$	RFLO feedthrough at the TX output	referenced to the desired frequency; T_{amb} = 25 °C	–	–25	–23	dBc
Pout	output transmit power	V_{TXRAMP} = 0 V; T_{amb} = 25 °C	1	4	7	dBm
IR_{TX}	image frequency rejection	referenced to the desired frequency	20	33	–	dBc
$Z_{inTXRAMP}$	input impedance at pin TXRAMP		10	–	–	kΩ
$C_{inTXRAMP}$	input capacitance at pin TXRAMP		–	–	10	pF
$V_{TXRAMP(max)}$	ramp voltage for $P_{out} = P_{max}$		–	0		V
$V_{TXRAMP(min)}$	ramp voltage for $P_{out} = P_{max} - 30$ dB		–	3.0	–	V
CNR_{TX}	carrier-to-noise ratio at TX output	Δf = 4320 kHz; T_{amb} = 25 °C; note 1	+127	+131	–	dBc/Hz

Notes

1. Measured and guaranteed only on the Philips demonstration board, including PCB and balun.
2. The imaginary part of the load impedance has been tuned out.

APPLICATION INFORMATION

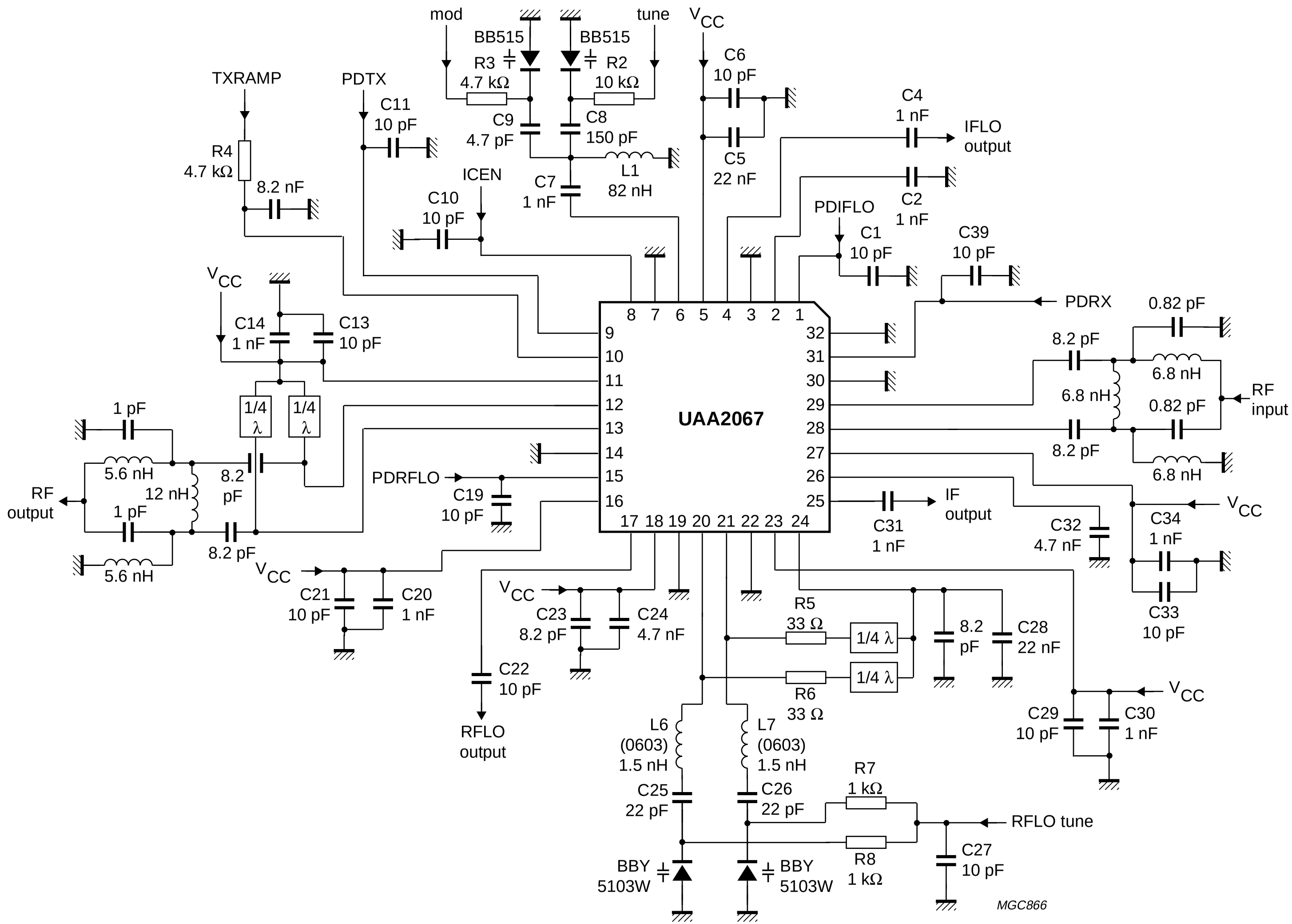

Figure 3 illustrates the electrical diagram of the UAA2067G Philips demonstration board for DECT applications. All matching is to 50 Ω for measurement purposes. Different values will be used in a real application.

Fig.3 Demonstration board diagram.

Application-indicative values

Measured on the Philips demonstration board, including PCB and balun at T_{amb} = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RF local oscillator (RFLO section powered-on)						
CNR_{RFLO}	carrier-to-noise ratio	Δf = 864 kHz	–	117	–	dBc/Hz
		Δf = 2500 kHz	–	128	–	dBc/Hz
		Δf = 4320 kHz	–	132	–	dBc/Hz
$PULL_{RFLO}$	pulling due to enabling RX or TX	V_{TXRAMP} = 3 V	–	5	–	kHz
$SHIFT_{RFLO}$	frequency shift due to 200 mV V_{CC} change		–	5	–	kHz
IF local oscillator (IFLO section powered-on)						
CNR_{IFLO}	carrier-to-noise ratio	Δf = 4320 kHz	–	140	–	dBc/Hz
$SPUR_{IFLO}$	spurious signal modulation due to 0.5 mV (RMS value) on the power supply	Δf = 4320 kHz	–	–60	–	dBc
$PULL_{IFLO}$	pulling due to enabling TX		–	1	–	kHz
$SHIFT_{IFLO}$	frequency shift due to 200 mV V_{CC} change		–	2.5	–	kHz
Transmit mode (transmitter, RFLO and IFLO sections powered-on)						
$PSRR_{TX}$	spurious signal modulation due to 0.5 mV (RMS value) on $V_{CC(MIX)}$, $V_{CC(TX)}$ and $V_{CC(RFLO)}$ only	Δf = 4320 kHz; note 1	–	–58	–	dBc
$SPUR_{TX}$	spurious signals	RFLO – 3IFLO	–	–40	–	dBc
		RFLO + 2IFLO	–	–35	–	dBc
		RFLO + 5IFLO	–	–51	–	dBc
N_{TX}	white noise level at the output		–	131	–	dBc/Hz

Note

1. Including PSRR of the RFLO circuitry.