DATA SHEET

TZA3013A; TZA3013B
SDH/SONET STM16/OC48 transimpedance amplifier

Objective specification
File under Integrated Circuits, IC19

2000 Jun 19

Philips Semiconductors

PHILIPS

FEATURES

- Low equivalent input noise, typically 8 pA/√Hz
- Wide dynamic range, typically 6 μA to 1.7 mA (p-p)
- Differential transimpedance of 4 kΩ
- Bandwidth from DC to 1.9 GHz
- Differential outputs
- On-chip Automatic Gain Control (AGC)
- No external components required
- Single supply voltage 3.3 V
- Bias voltage for PIN diode
- Remains linear up to 1.7 mA (p-p) input current (unclipped)
- Switched output polarity available (types A and B).

APPLICATIONS

- Digital fibre optic receiver in short, medium and long haul optical telecommunications transmission systems or in high speed data networks
- Wide-band RF gain block.

GENERAL DESCRIPTION

The TZA3013 is a transimpedance amplifier with AGC, designed to be used in STM16/OC48 fibre-optic links. It amplifies the current generated by a photo detector (PIN diode or avalanche photodiode) and converts it to a differential output voltage.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA3013AHL	LQFP32	plastic low profile quad flat package; 32 leads; body 5 × 5 × 1.4 mm	SOT401-1
TZA3013AU	–	bare die in waffle pack carriers; die dimensions 0.810 × 1.230 mm	–
TZA3013BU	–	bare die in waffle pack carriers; die dimensions 0.810 × 1.230 mm	–

BLOCK DIAGRAM

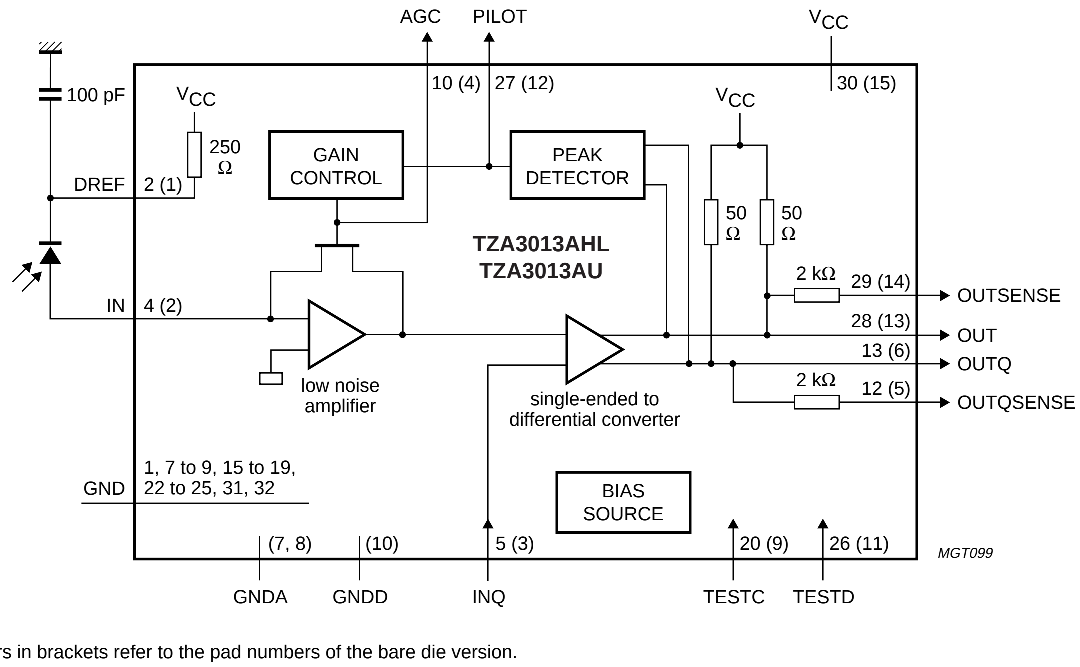


Fig.1 Block diagram of TZA3013AHL and TZA3013AU.

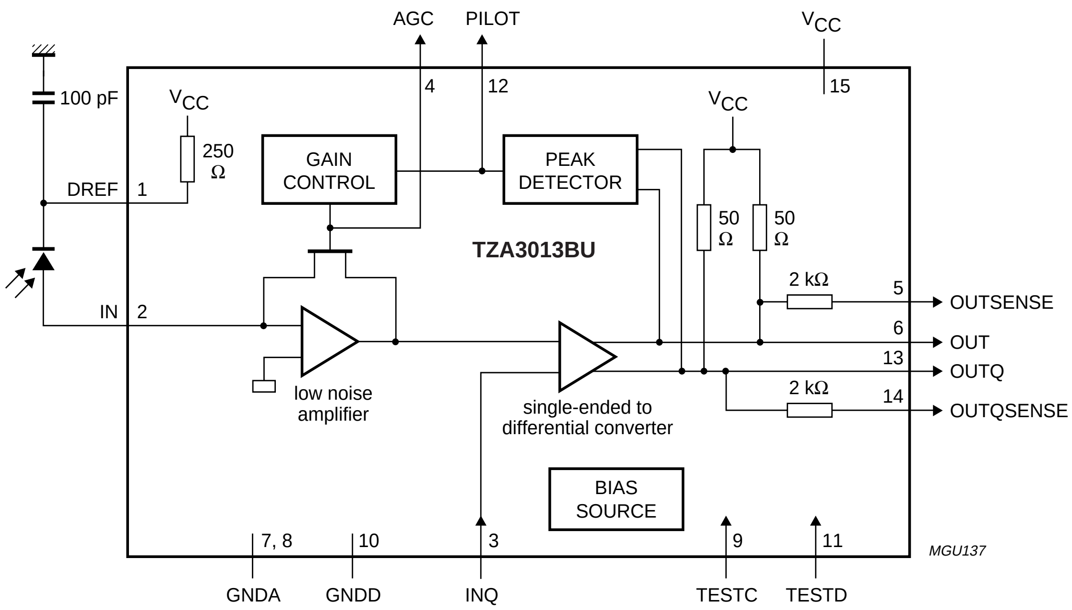


Fig.2 Block diagram of TZA3013BU (bare die only).

PINNING

SYMBOL	PIN TZA3013AHL	PAD TZA3013AU	PAD TZA3013BU	TYPE	DESCRIPTION
GND	1	–	–	ground	ground
DREF	2	1	1	analog output	bias voltage output for PIN diode; connect cathode of PIN diode to this pin
n.c.	3	–	–	n.c.	not connected
IN	4	2	2	input	current input; anode of PIN diode should be connected to this pin; note 1
INQ	5	3	3	input	decision level adjust input; note 1
n.c.	6	–	–	n.c.	not connected
GND	7	–	–	ground	ground
GND	8	–	–	ground	ground
GND	9	–	–	ground	ground
AGC	10	4	4	analog output	AGC voltage
n.c.	11	–	–	n.c.	not connected
OUTQSENSE	12	5	14	analog output	data sense output for OUTQ; for test purposes
OUTQ	13	6	13	output	data output; compliment of OUT
n.c.	14	–	–	n.c.	not connected
GND	15	–	–	ground	ground
GND	16	–	–	ground	ground
GND	17	–	–	ground	ground
GND	18	–	–	ground	ground
GND	19	–	–	ground	ground
TESTC	20	9	9	input	test input; not used in the application
n.c.	21	–	–	n.c.	not connected
GND	22	–	–	ground	ground
GND	23	–	–	ground	ground
GND	24	–	–	ground	ground
GND	25	–	–	ground	ground
TESTD	26	11	11	input	test input; not used in the application
PILOT	27	12	12	analog output	pilot tone detection current output
OUT	28	13	6	output	data output; compliment of OUTQ; note 2

SYMBOL	PIN TZA3013AHL	PAD TZA3013AU	PAD TZA3013BU	TYPE	DESCRIPTION
OUTSENSE	29	14	5	analog output	data sense output for OUT; for test purposes
V_{CC}	30	15	15	supply	supply voltage
GND	31	–	–	ground	ground
GND	32	–	–	ground	ground
GNDA	–	7	7	ground	analog ground
GNDA	–	8	8	ground	analog ground
GNDD	–	10	10	ground	digital ground

Notes

1. DC bias voltage = 0.86 V.
2. This pin goes HIGH when current flows into pin IN.

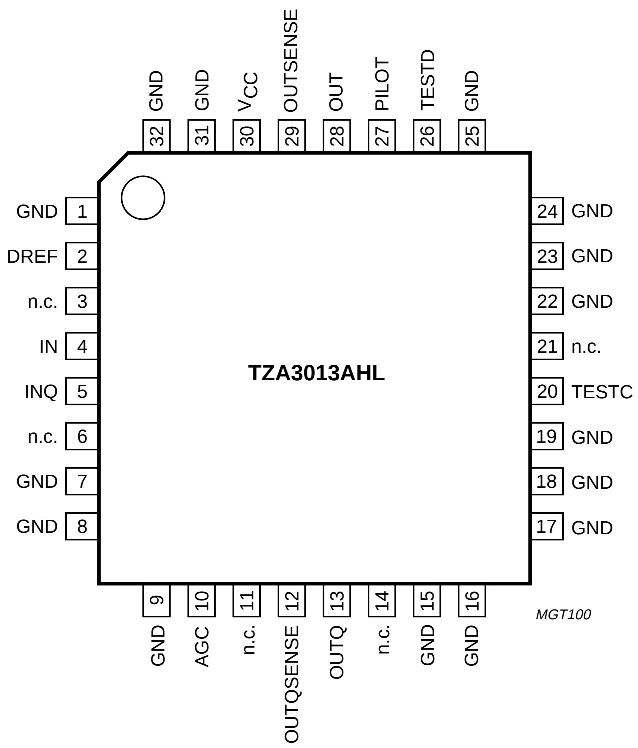


Fig.3 Pin configuration of TZA3013AHL.

FUNCTIONAL DESCRIPTION

The TZA3013 is a transimpedance amplifier intended for use in fibre optic links for signal recovery in STM16/OC48 applications. It amplifies the current generated by a photo detector (PIN diode or avalanche photodiode) and converts it to a differential output voltage.

The most important characteristics of the TZA3013 are high receiver sensitivity and wide dynamic range. High receiver sensitivity is achieved by minimizing transimpedance amplifier noise.

The TZA3013 has a wide dynamic range to handle the signal current generated by the PIN diode which can vary from 6 μA to 1.7 mA (p-p). This is implemented by an AGC loop which reduces the preamplifier feedback resistance so that the amplifier remains linear over the whole input range. The AGC loop hold capacitor is integrated on-chip, so an external capacitor is not required.

A differential amplifier converts the output of the preamplifier to a differential voltage. The data output circuit is shown in Fig.4.

The logic level symbol definitions are shown in Fig.5.

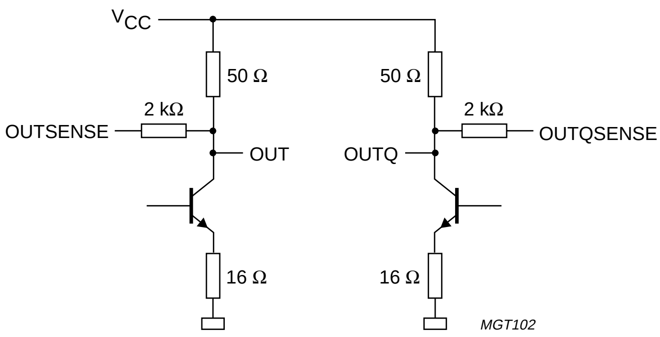


Fig.4 Data output circuit.

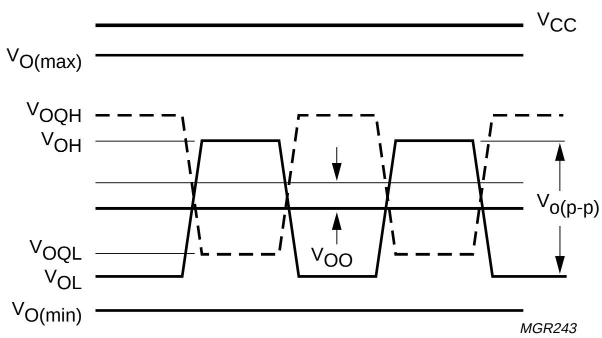


Fig.5 Logic level symbol definitions for data outputs OUT and OUTQ.

PIN diode bias voltage DREF

The performance of an optical receiver is largely determined by the combined effect of the transimpedance amplifier and the PIN diode. In particular, the method used to connect the PIN diode to the input and the layout around the input pin strongly influences the main parameters of a transimpedance amplifier, such as sensitivity, bandwidth, and PSRR. Sensitivity is most affected by the value of the total capacitance at the input pin. Therefore, to obtain the highest possible sensitivity requires the value of total capacitance to be as low as possible by reducing the capacitance of the PIN diode and the parasitics around the input pin. To minimize parasitics, the PIN diode should be placed as close as physically possible to the IC.
The capacitance of the PIN diode can be reduced by making the value of reverse voltage across it as high as possible.

The PIN diode can be connected to the input in two ways. Figure 6 shows the PIN diode connected between pins DREF and IN.

Pin DREF provides an easy bias voltage for the PIN diode. The voltage at DREF is derived from V_{CC} by a low-pass filter comprising internal resistor R1 and external capacitor C2 which decouples any supply voltage noise. The value of external capacitor C2 affects the value of PSRR and should have a minimum value of 100 pF. Increasing this value increases the value of PSRR.

For a supply voltage of 3.3 V, the reverse voltage across the PIN diode is 2.438 V (3.3 V – 0.862 V). It is preferable to connect the cathode of the PIN diode to a voltage higher than V_{CC} if there is one available on the PCB, leaving pin DREF unconnected. If a negative supply voltage is available, the configuration shown in Fig.7 can be used. It should be noted that in this configuration, the direction of the signal current is reversed to that shown in Fig.6. It is essential that the PIN diode bias voltage is correctly filtered to achieve the highest possible level of sensitivity.

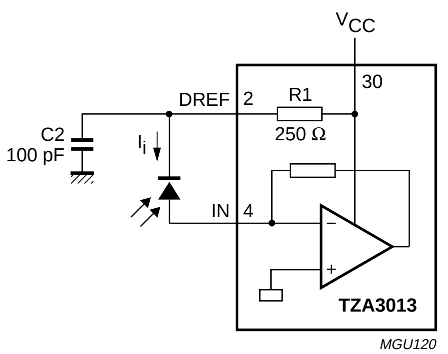


Fig.6 The PIN diode connected between the input and pin DREF.

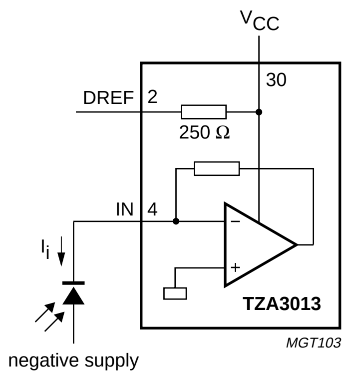


Fig.7 The PIN diode connected between the input and a negative supply voltage.

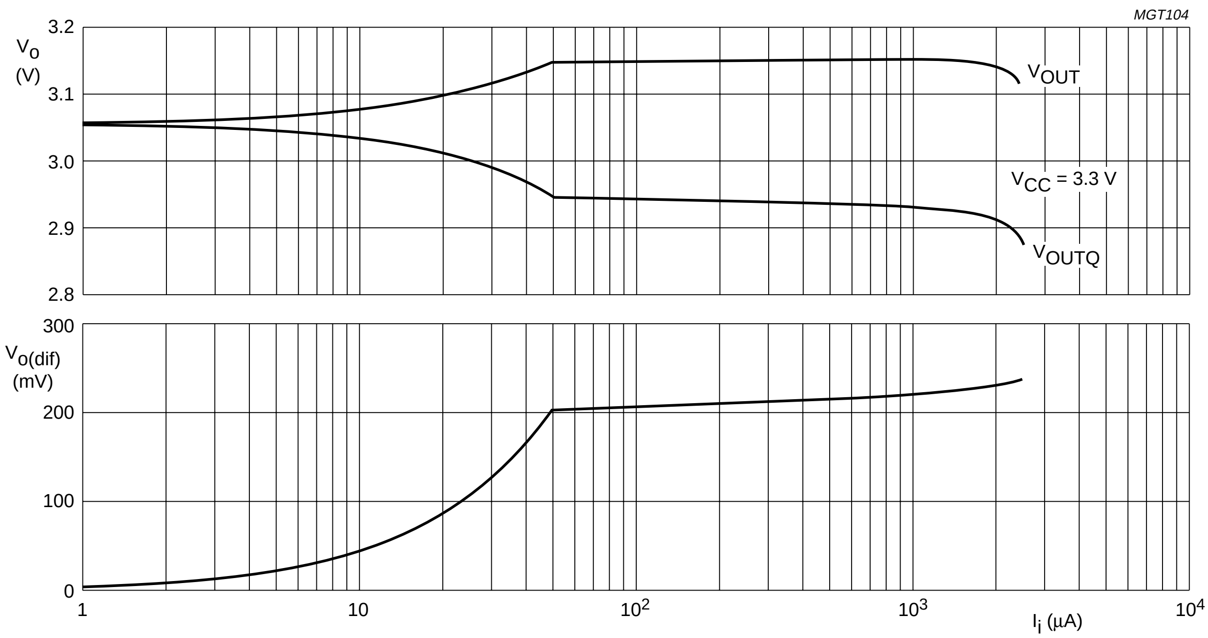
AGC

The TZA3013 transimpedance amplifier can handle input currents from 6 µA to 1.7 mA which is equivalent to a dynamic range of 49 dB. At low input currents, the transimpedance must be high to obtain enough output voltage, and the noise should be low enough to guarantee a minimum bit error rate. At high input currents however, the transimpedance should be low to avoid pulse width distortion. To achieve the wide dynamic range requires the gain of the amplifier to depend on the level of the input signal. This is achieved in the TZA3013 by an AGC loop.

The AGC loop comprises a peak detector, a hold capacitor and a gain control circuit. The peak detector detects the amplitude of the signal and the hold capacitor stores it. The hold capacitor voltage is compared to a threshold voltage which corresponds to an input current of 50 µA (p-p). The AGC is only active when the input signal level is larger than the threshold level and is inactive when the input signal is smaller than the threshold level.

When the AGC is inactive, the transimpedance is at its maximum value of 4 kΩ differential. When the AGC is active, the feedback resistor value of the transimpedance amplifier is reduced, reducing its transimpedance, to keep the output voltage constant. The transimpedance is regulated from 4 kΩ at low currents (I_i < 50 µA) to 80 Ω at high currents (I_i = 1.7mA). The AGC allows the amplifier to remain linear over the whole input current range compared to other configurations which clip the large signals, such as those using Schottky diodes, for example.

The top half of Fig.8 shows the output voltage at pins OUT and OUTQ (V_{OUT} and V_{OUTQ}) as a function of DC input current (I_I) at a supply voltage of 3.3 V. The bottom half of Fig.8 shows the difference between V_{OUT} and V_{OUTQ}. The output voltage changes linearly up to an input current of 50 µA. At this point and above, the AGC becomes active and tries to keep the differential output voltage constant, which is about 220 mV for a large range input current of <1.7 mA.



$V_{o(dif)} = V_{OUT} - V_{OUTQ}$

Fig.8 AGC characteristics.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–0.5	+3.8	V
V_n	DC voltage			
	pins/pads IN and INQ	–0.5	+2.0	V
	pins/pads OUT and OUTQ	–0.5	V_{CC} + 0.5	V
	pins/pads OUTSENSE and OUTQSENSE	–0.5	V_{CC} + 0.5	V
	pin/pad PILOT	–0.5	V_{CC} + 0.5	V
	pin/pad DREF	–0.5	V_{CC} + 0.5	V
I_n	DC current			
	pins/pads IN and INQ	–4.0	+4.0	mA
	pins/pads OUT and OUTQ	–10	+10	mA
	pin/pad PILOT	–0.2	+0.2	mA
	pin/pad DREF	–4.0	+4.0	mA
P_{tot}	total power dissipation	–	300	mW
T_{stg}	storage temperature	–65	+150	°C
T_j	junction temperature	–	150	°C
T_{amb}	ambient temperature	–40	+85	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However it is good practice to take normal precautions appropriate to handling MOS devices (see *“Handling MOS devices”*).

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th(j-s)}$	thermal resistance from junction to solder point	15	K/W

CHARACTERISTICS

Typical values at T_j = 25 °C and V_{CC} = 3.3 V; minimum and maximum values are valid over the entire ambient temperature range and supply range; all voltages are measured with respect to ground; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		3.0	3.3	3.6	V
I_{CC}	supply current	AC coupled; R_L = 50 Ω; without input signal	–	26	37	mA
P_{tot}	total power dissipation	V_{CC} = 3.3 V	–	85.8	134	mW
T_j	junction temperature		–40	–	+125	°C
T_{amb}	ambient temperature		–40	+25	+85	°C
R_{tr}	small-signal transresistance of the receiver	measured differentially; AC coupled				
		$R_L = \infty$	6.6	8.4	10	kΩ
		R_L = 50 Ω	3.3	4.2	5.0	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$f_{-3dB(h)}$	high frequency –3 dB point	C_i = 0.5 pF	1.7	1.9	–	GHz
$I_{n(tot)(rms)}$	total integrated RMS noise current over bandwidth	referenced to input; Δf_i = 1.8 GHz third-order Bessel filter; note 1	–	425	–	nA
PSRR	power supply rejection ratio	measured differentially; note 2				
		f_i = 100 kHz to 100 MHz	–	–	–	μA/V
		f_i = 3 GHz	–	–	–	μA/V
Automatic gain control loop: pin AGC						
t_{att}	AGC attack time		–	10	–	μs
t_{decay}	AGC decay time		–	10	–	μs
$I_{th(AGC)(p-p)}$	AGC threshold current (peak-to-peak value)	referenced to input	–	50	–	μA
Input: pin IN						
$I_{i(p-p)}$	input current (peak-to-peak value)		–1700	–	+1700	μA
$V_{I(bias)}$	input bias voltage		–	862	–	mV
R_i	small-signal input resistance	tested at 1 MHz; I_i < 20 μA (p-p)	–	53	–	Ω
Data outputs: pins OUT and OUTQ						
$V_{o(cm)}$	common mode output voltage	AC coupled; R_L = 50 Ω	–	V_{CC} – 0.243	–	V
$V_{o(se)(p-p)}$	single-ended load output voltage (peak-to-peak value)	AC coupled; R_L = 50 Ω; I_i = 100 μA (p-p)	–	110	–	mV
V_{OO}	differential output offset voltage		–100	0	+100	mV
R_o	output resistance	single-ended; DC tested	40	53	65	Ω
t_r	rise time	20% to 80%	–	tbf	–	ps
t_f	fall time	80% to 20%	–	tbf	–	ps

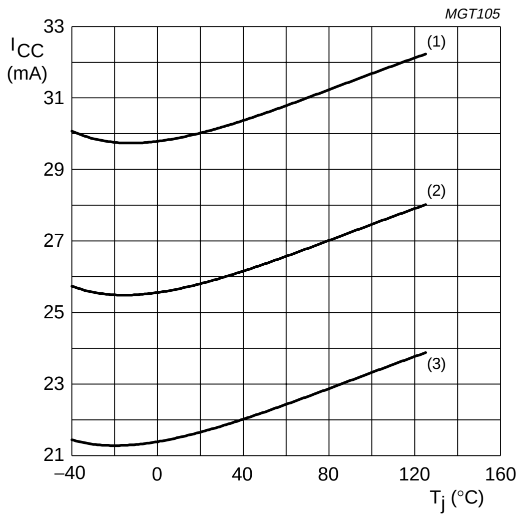
Notes

1. Measurement performed with C_i = 0.5 pF comprising 0.4 pF (photodiode) and 0.1 pF (allowed for PCB layout).
2. PSRR is defined as the ratio of change in input current (ΔI_i) corresponding to change in supply voltage (ΔV_{CC}):

$$PSRR = \frac{\Delta I_i}{\Delta V_{CC}}$$

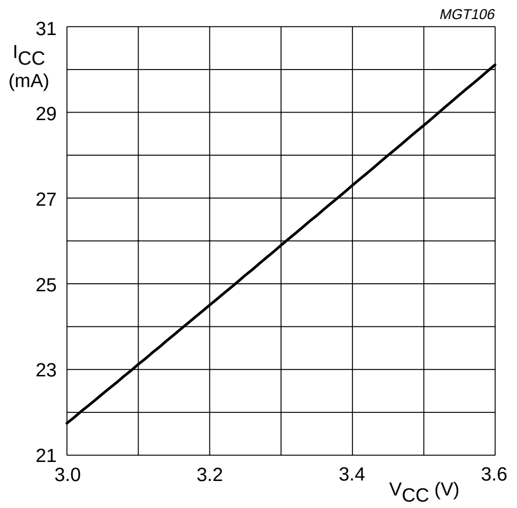
For example, a +4 mV disturbance on V_{CC} at 10 MHz will typically add an extra tbf nA to I_i (photodiode output current). The value of the external capacitor connected between pins DREF and GND has a significant effect on the value of PSRR. The specification is valid with an external capacitor of 1 nF.

TYPICAL PERFORMANCE CHARACTERISTICS



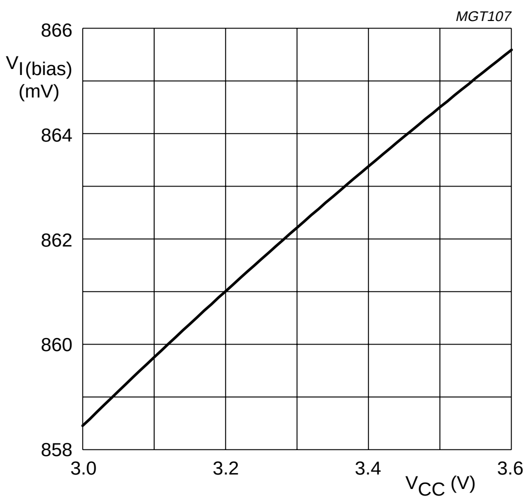
(1) V_{CC} = 3.6 V.
(2) V_{CC} = 3.3 V.
(3) V_{CC} = 3.0 V.

Fig.9 Supply current as a function of the junction temperature.



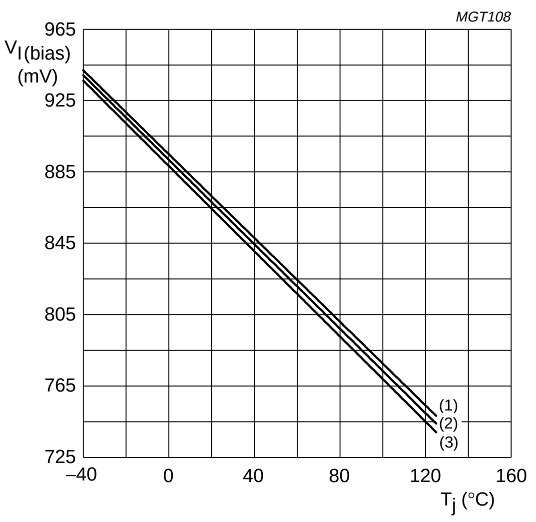
T_j = 25 °C.

Fig.10 Supply current as a function of the supply voltage.



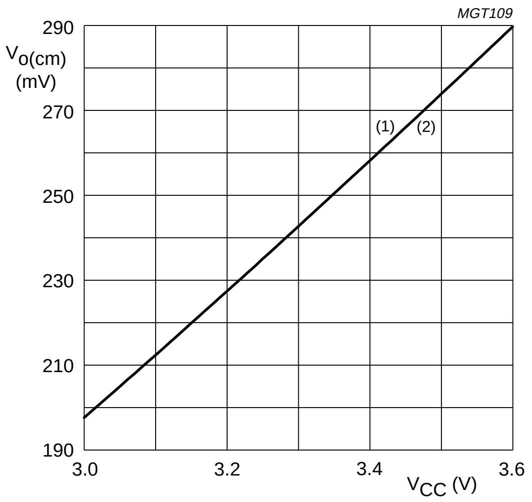
T_j = 25 °C.

Fig.11 Input bias voltage as a function of the supply voltage.



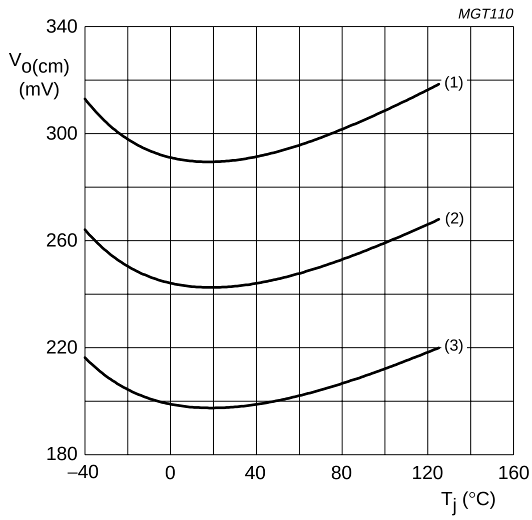
(1) V_{CC} = 3.6 V.
(2) V_{CC} = 3.3 V.
(3) V_{CC} = 3.0 V.

Fig.12 Input bias voltage as a function of the junction temperature.



T_j = 25 °C.
(1) $V_{CC} - V_{OUT}$.
(2) $V_{CC} - V_{OUTQ}$.

Fig.13 Common mode output voltage as a function of the supply voltage referenced to V_{CC}.



(1) V_{CC} = 3.6 V.
(2) V_{CC} = 3.3 V.
(3) V_{CC} = 3.0 V.

Fig.14 Common mode output voltage as a function of the junction temperature referenced to V_{CC}.

APPLICATION AND TEST INFORMATION

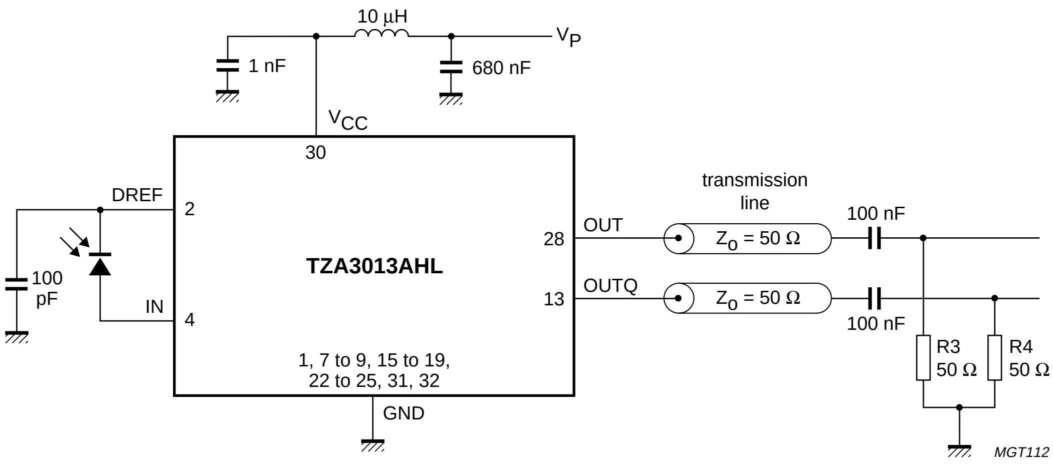
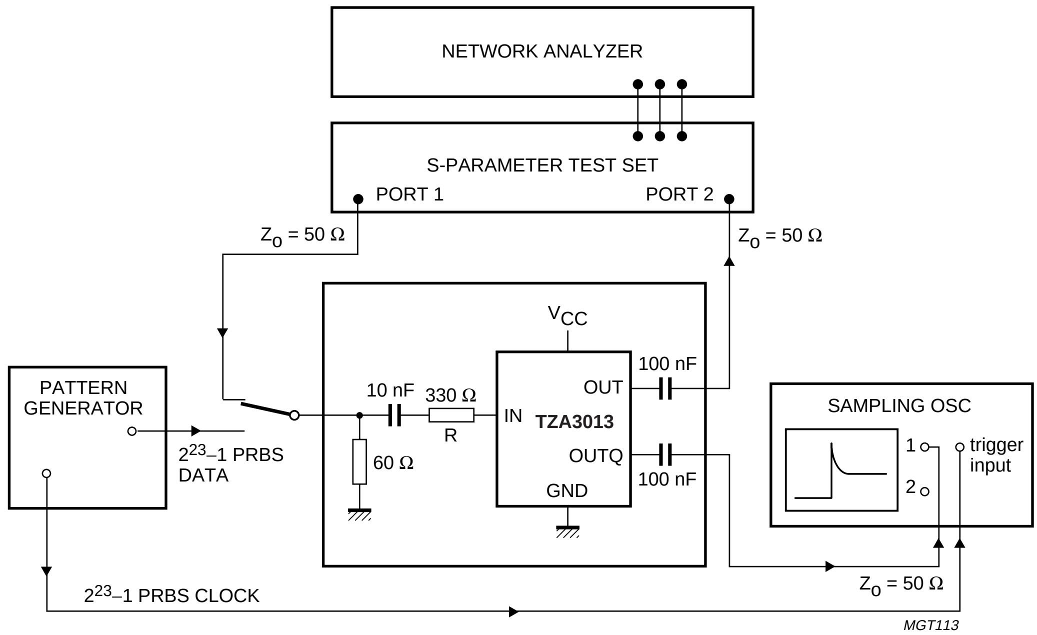


Fig.15 Application diagram.



Total impedance of the test circuit = Z_T and is calculated by the equation $Z_T = s_{21} \times (R + Z_{IN}) \times 2$

where s_{21} is the insertion loss of ports 1 and 2.

Typical values: R = 330 Ω, Z_{IN} = 73 Ω.

Fig.16 Test circuit.

BONDING PAD LOCATIONS

SYMBOL	PAD TZA3013AU	PAD TZA3013BU	COORDINATES[1]	
			x	y
DREF	1	1	–440	+155
IN	2	2	–440	+10
INQ	3	3	–440	–157
AGC	4	4	–266	–255
OUTQSENSE	5	–	–40	–255
	–	14	–40	+255
OUTQ	6	–	+116	–255
	–	13	+110	+255
GNDA	7	7	+256	–255
GNDA	8	8	+398	–255
TESTC	9	9	+448	–79
GNDD	10	10	+448	+70
TESTD	11	11	+410	+255
PILOT	12	12	+260	+255
OUT	13	–	+110	+255
	–	6	+116	–255
OUTSENSE	14	–	–40	+255
	–	5	–40	–255
V_{CC}	15	15	–266	+255

Note

1. All coordinates are referenced, in µm, to the centre of the die.

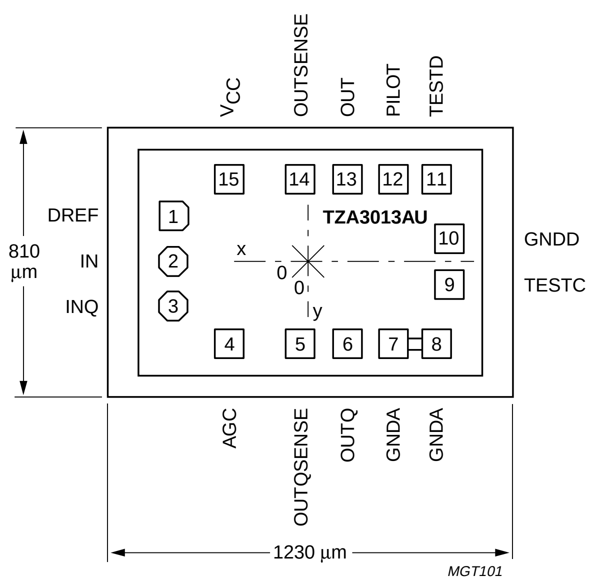


Fig.17 Bonding pad locations of the TZA3013AU.

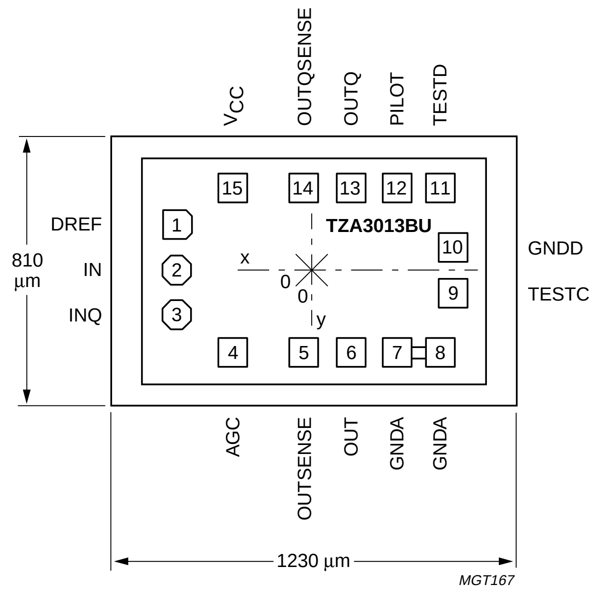


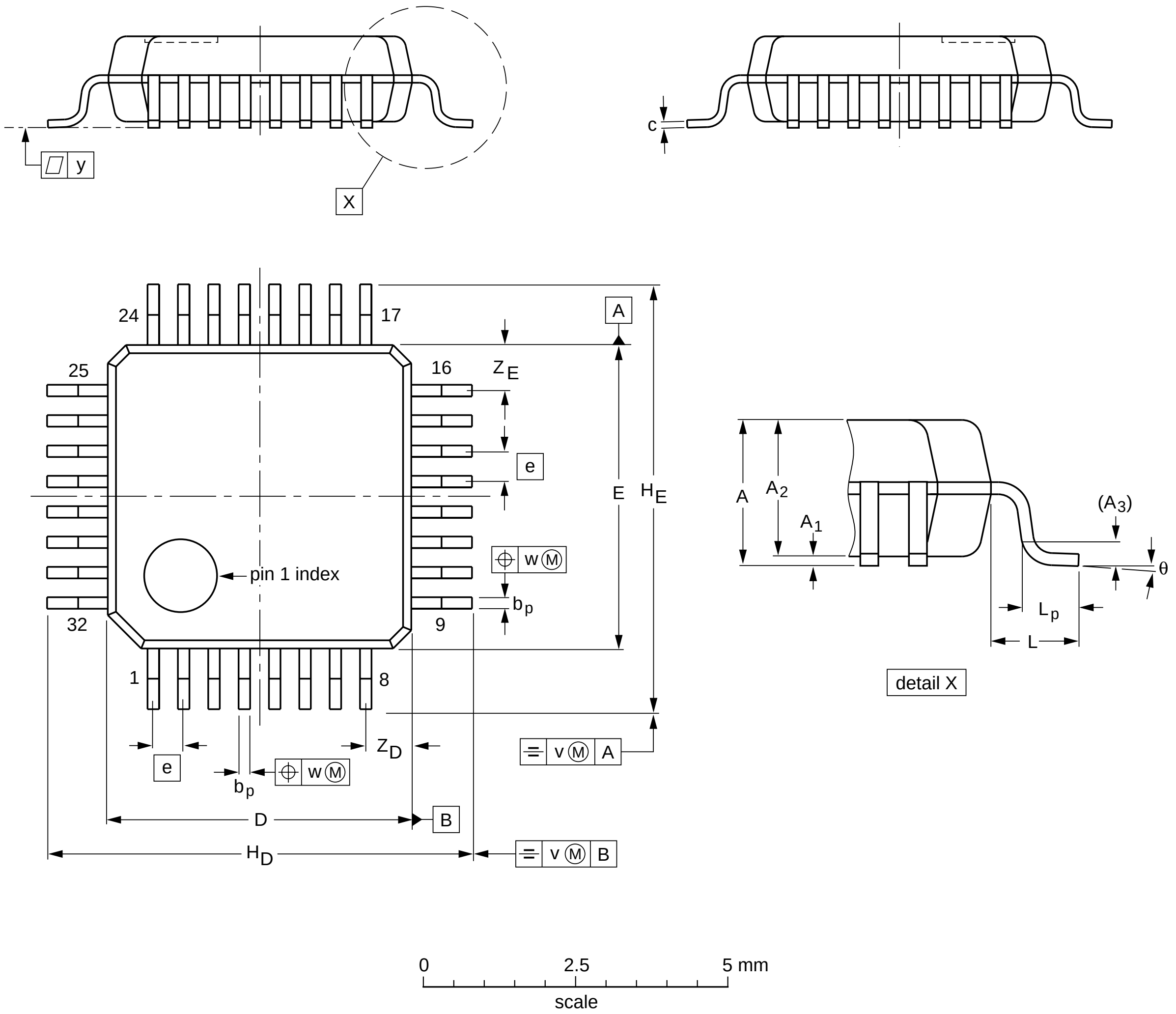
Fig.18 Bonding pad locations of the TZA3013BU.

Physical characteristics of the bare die

PARAMETER	VALUE
Glass passivation	0.3 µm PSG (PhosphoSilicate Glass) on top of 0.8 µm silicon nitride
Bonding pad dimension	minimum dimension of exposed metallization is 90 × 90 µm (pad size = 100 × 100 µm) except pads 2 and 3 which have exposed metallization of 80 × 80 µm (pad size = 90 × 90 µm)
Metallization	2.8 µm AlCu
Thickness	380 µm nominal
Size	0.810 × 1.230 mm (0.996 mm^2)
Backing	silicon; electrically connected to GND potential through substrate contacts
Attach temperature	<440 °C; recommended die attach is glue
Attach time	<15 s

PACKAGE OUTLINE

LQFP32: plastic low profile quad flat package; 32 leads; body 5 x 5 x 1.4 mm **SOT401-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_D	H_E	L	L_p	v	w	y	Z_D(1)	Z_E(1)	θ
mm	1.60	0.15 0.05	1.5 1.3	0.25	0.27 0.17	0.18 0.12	5.1 4.9	5.1 4.9	0.5	7.15 6.85	7.15 6.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT401-1	136E01	MS-026				~~99-12-27~~ 00-01-19

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW[1]
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS [(1)]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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