SIEMENS

Components
for Entertainment Electronics

2 Band TV Tuner

TUA 6026

Mixer-Oscillator-PLL
with Unbalanced IF-Amplifier

Preliminary Data Sheet 1998-09-01

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Data Classification

Maximum Ratings

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Recommended Operating Conditions

Under this conditions the functions given in the circuit description are fulfilled. Nominal conditions specify mean values expected over the production spread and are the proposed values for interface and application. If not stated otherwise, nominal values will apply at T_A=25°C and the nominal supply voltage.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit.

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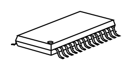
TUA 6026

Preliminary Data **BIPOLAR**

1 Overview



P-TSSOP-28-1

1.1 Features

General

- Suitable for NTSC and PAL tuners
- Full ESD protection

Mixer/Oscillator

- High impedance mixer input for VHF
- Low impedance mixer input for UHF
- 4 pin oscillator for VHF
- 4 pin oscillator for UHF

IF-Amplifier

- Unbalanced SAW preamplifier
- Low output impedance

PLL

- PLL with short lock-in time;
  no asynchronous divider stage
- High voltage VCO tuning output
- Fast I^2C Bus
- 4 NPN bandswitch buffers
- Internal VHF/UHF switch
- Lock-in flag
- Power-down reset
- Programmable reference divider ratio (64, 80, 128)
- Programmable charge pump current

Type	Ordering Code	Package
TUA 6026-K	Q67037-A1053	P-TSSOP-28-1
TUA 6026-S	Q67037-A1058	P-TSSOP-28-1

1.2 Functional Description

The TUA 6026 device combines a digitally programmable phase locked loop (PLL), with a mixer-oscillator block including two balanced mixers and oscillators for use in TV tuners.

The PLL block with four hard-switched chip addresses forms a digitally programmable phase locked loop. With a 4 MHz quartz crystal, the PLL permits precise setting of the frequency of the tuner oscillator up to 900 MHz in increments of 62.5 kHz. The tuning process is controlled by a microprocessor via an I^2C Bus. The device has four output ports, two of them (P0 and P1) can also be used as TTL input ports. A flag is set when the loop is locked. The input ports and lock flag can be read by the processor via the I^2C Bus.

The mixer-oscillator block includes two balanced mixers (one mixer with high-impedance input and one mixer with a balanced low-impedance input), two frequency and amplitude-stable balanced oscillators for VHF, HYPER and UHF, a low-noise reference voltage source and a band switch.

1.3 Application

The IC is suitable for NTSC and PAL tuners in TV- and VCR-sets or cable set-top receivers for analog TV and Digital Video Broadcasting.

1.4 Pin Configuration

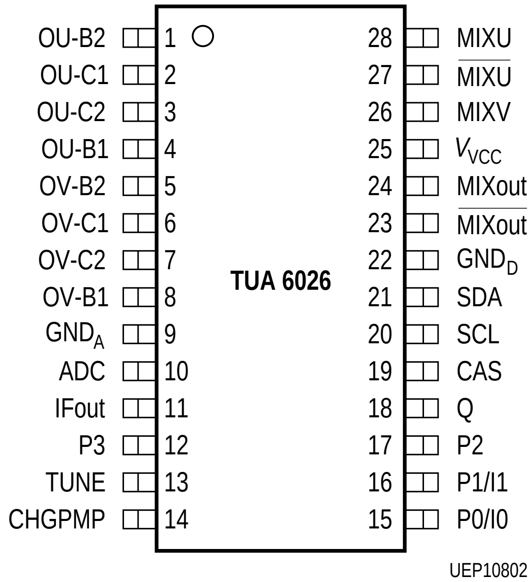


Figure 1

1.5 Pin Definitions and Functions

Pin No.	Symbol	Function
1	OU-B2	UHF oscillator amplifier, high-impedance base input, symmetrical to OU-B1
2	OU-C1	UHF oscillator amplifier, high-impedance collector output, symmetrical to OU-C2
3	OU-C2	UHF oscillator amplifier, high-impedance collector output, symmetrical to OU-C1
4	OU-B1	UHF oscillator amplifier, high-impedance base input, symmetrical to OU-B2
5	OV-B2	HYPER oscillator amplifier, high-impedance base input, symmetrical to OV-B1
6	OV-C1	HYPER oscillator amplifier, high-impedance collector output, symmetrical to OV-C2
7	OV-C2	HYPER oscillator amplifier, high-impedance collector output, symmetrical to OV-C1

1.5 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Function
8	OV-B1	HYPER oscillator amplifier, high-impedance base input, symmetrical to OV-B2
9	GND_A	Analog Ground
10	ADC	ADC input
11	IFout	IF output
12	P3	Port output
13	TUNE	VCO tuning voltage output
14	CHGPMP	Charge pump output/loop filter
15	P0/I0	Port output/TTL input
16	P1/I1	Port output/TTL input
17	P2	Port output
18	Q	4 MHz low-impedance crystal oscillator input
19	CAS	Chip address select
20	SCL	Clock input for the I^2C Bus
21	SDA	Data input/output for the I^2C Bus
22	GND_D	Digital Ground
23	$\overline{\text{MIXout}}$	Inverse Mixer output, symmetrical to MIXout
24	MIXout	Mixer output, symmetrical to $\overline{\text{MIXout}}$
25	V_{VCC}	Analog supply voltage
26	MIXV	VHF mixer input, high-impedance
27	$\overline{\text{MIXU}}$	UHF mixer input, low-impedance, symmetrical to MIXU
28	MIXU	UHF mixer input, low-impedance, symmetrical to $\overline{\text{MIXU}}$

1.6 Block Diagram

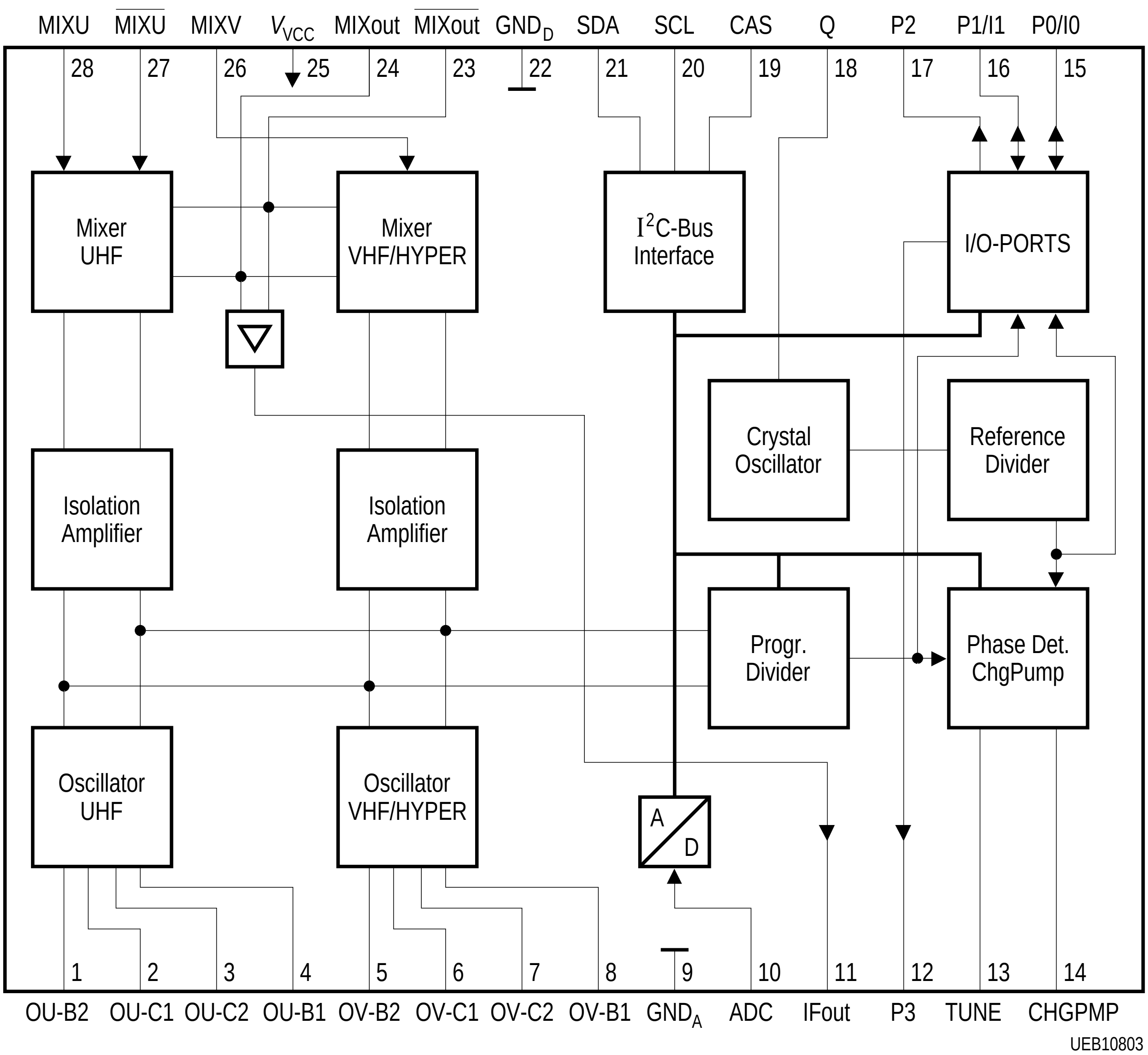


Figure 2

2 Circuit Description

2.1 Mixer-Oscillator Block

The mixer oscillator section includes two balanced mixers (double balanced mixer), two balanced oscillators for VHF low and/or HYPER band and UHF, a reference voltage source and a band switch.

Filters between tuner input and IC separate the TV frequency signals into two bands. The band switching in the tuner front-end is done by using two or three port outputs. In the selected band the signal passes a tuner input stage with MOSFET amplifier, a double-tuned bandpass filter and is then fed to the balanced mixer input of the IC which has in case of VHF/Hyperband a high-impedance input and in case of UHF a low-impedance input.

The input signal is mixed there with the signal from the activated on chip oscillator to the IF frequency which is filtered out at the balanced high-impedance output pair by means of a parallel tuned circuit. The following SAW preamplifier has a low output impedance to drive a 75 Ω load directly.

2.2 PLL Block

The mixer-oscillator signal VCO/$\overline{\text{VCO}}$ is internally DC-coupled as a differential signal at the programmable divider inputs. The signal subsequently passes through a programmable divider with ratio N = 256 through 32767 and is then compared in a digital frequency/phase detector to a reference frequency f_{ref} = 62.5 kHz. This frequency is derived from a unbalanced, low-impedance 4 MHz crystal oscillator (pin Q) divided by Q = 64.

The phase detector has two outputs UP and DOWN that drive two current sources I+ and I- of a charge pump. If the negative edge of the divided VCO signal appears prior to the negative edge of the reference signal, the I+ current source pulses for the duration of the phase difference. In the reverse case the I- current source pulses. If the two signals are in phase, the charge pump output (CHGPMP) goes into the high-impedance state (PLL is locked). An active low-pass filter integrates the current pulses to generate the tuning voltage for the VCO (internal amplifier, external pullup resistor at TUNE and external RC circuitry). The charge pump output is also switched into the high-impedance state when the control bit T0 = 1. Here it should be noted, however, that the tuning voltage can alter over a long period in the high-impedance state as a result of self-discharge in the peripheral circuity. TUNE may be switched off by the control bit OS to allow external adjustments.

If the VCO is not working the PLL locks to a tuning voltage of 33 V.

By means of control bit 5I the pump current can be switched between two values by software. This programmability permits alteration of the control response of the PLL in the locked-in state. In this way different VCO gains can be compensated, for example.

The software-switched ports P0, P1, and P2 are general-purpose open-collector outputs. The test bit T1 = 1, switches the test signals f_{ref} (4 MHz / 64) and C_y (divided input signal) to P0 and P1 respectively. P0, P1 are bidirectional.

The lock detector resets the lock flag FL when the width of the charge pump current pulses is greater than the period of the crystal oscillator (i.e. 250 ns). Hence, when FL = 1, the maximum deviation of the input frequency from the programmed frequency is given by

$$\Delta f = \pm I_P \, (K_{VCO} / f_Q) \, (C_1 + C_2) / (C_1 C_2)$$

where I_P is the charge pump current, K_{VCO} the VCO gain, f_Q the crystal oscillator frequency and C_1, C_2 the capacitances in the loop filter (see ”Application Circuits” on page 26). As the charge pump pulses at 62.5 kHz (= f_{ref}), it takes a maximum of 16 µs for FL to be reset after the loop has lost lock state.

Once FL has been reset, it is set only if the charge pump pulse width is less than 250 ns for eight consecutive f_{ref} periods. Therefore it takes between 128 and 144 µs for FL to be set after the loop regains lock.

2.3 I^2C-Bus Interface

Data is exchanged between the processor and the PLL via the I^2C Bus. The clock is generated by the processor (input SCL), while pin SDA functions as an input or output depending on the direction of the data (open collector, external pull-up resistor). Both inputs have hysteresis and a low-pass characteristic, which enhance the noise immunity of the I^2C Bus.

The data from the processor pass through an I^2C-Bus controller. Depending on their function the data are subsequently stored in registers. If the bus is free, both lines will be in the marking state (SDA, SCL are HIGH). Each telegram begins with the start condition and ends with the stop condition. Start condition: SDA goes LOW, while SCL remains HIGH. Stop condition: SDA goes HIGH while SCL remains HIGH. All further information transfer takes place during SCL = LOW, and the data is forwarded to the control logic on the positive clock edge.

The table ”Bit Allocation” (see ”Bit Allocation Read/Write” on page 12) should be referred to the following description. All telegrams are transmitted byte-by-byte, followed by a ninth clock pulse, during which the control logic returns the SDA line to LOW (acknowledge condition). The first byte is comprised of seven address bits. These are used by the processor to select the PLL from several peripheral components (chip select). The LSB bit (R/W) determines whether data are written into (R/W = 0) or read from (R/W = 1) the PLL.

In the data portion of the telegram during a WRITE operation, the MSB bit of the first or third data byte determines whether a divider ratio or control information is to follow. In each case the second byte of the same data type has to follow the first byte. If the address byte indicates a READ operation, the PLL generates an acknowledge and then shifts out the status byte onto the SDA line. If the processor generates an acknowledge, a further status byte is output; otherwise the data line is released to allow the processor to generate a stop condition. The status word consists of two bits from the TTL input ports, three bits from the A/D converter, the lock flag and the power-on flag.

Four different chip addresses can be set by appropriate DC level at pin CAS (see ”Address Selection” on page 14).

When the supply voltage is applied, a power-on reset circuit prevents the PLL from setting the SDA line to LOW, which would block the bus. The power-on reset flag POR is set at power-on and if V_{VCC} falls below 3.2 V. It will be reset at the end of a READ operation.

2.3.1 Bit Allocation Read/Write

Byte	MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB	Ack	Remarks
Write Data										
Address byte	1	1	0	0	0	MA1	MA0	0	A	
Progr. divider byte 1	0	n14	n13	n12	n11	n10	n9	n8	A	
Progr. divider byte 2	n7	n6	n5	n4	n3	n2	n1	n0	A	
Control byte 1	1	5I	T1	T0	1	RSA	RSB	OS	A	
Control byte 2	x	x	x	x	P3	P2	P1	P0	A	
Read Data										
Address byte	1	1	0	0	0	MA1	MA0	1	A	
Status byte	POR	FL	x	I1	I0	A2	A1	A0	A	

2.3.2 Description of Symbols

Symbol	Description
MA0, MA1	Address selection bits (see ”Address Selection” on page 14)
n14 to n0	Programmable divider bits: $N = 2^{14} * n14 + 2^{13} * n13 + ... + 2^3 * n3 + 2^2 * n2 + 2^1 * n1 + n0$
5I	Charge pump current: Bit = 0 : Charge pump current = 50 µA Bit = 1 : Charge pump current = 220 µA
T1, T0	Test bits (see ”Test Modes” on page 14)
RSA, RSB	Reference divider bits (see ”Reference Divider Ratio” on page 14)
OS	Tuning amplifier control bit: Bit = 0 : Enable V_{TUNE} Bit = 1 : Disable V_{TUNE}
PO, P1, P2, P3	NPN ports control bits Bit = 0 : NPN open-collector output is inactive, TTL inputs at P0, P1 Bit = 1 : NPN open-collector output is active UHF/VHF bandswitch (see ”UHF/VHF Bandswitch” on page 13)
A0, A1, A2	ADC bits (see ”A/D Converter Levels” on page 14)
I0, I1	Input data from P0/I0, P1/I1
FL	PLL lock flag Bit = 1 : Loop is locked
POR	Power-on reset flag Flag is set at power-on and reset at the end of READ operation
x	don‘t care

2.3.3 UHF/VHF Bandswitch

IC is in UHF Mode	Ports Pn			
	P0	P1	P2	P3
TUA 6026-K	x	x	1	x
TUA 6026-S	x	x	x	1

2.3.4 Address Selection

Voltage at CAS	MA1	MA0
(0...0.1) * V_{VCC}	0	0
Open circuit	0	1
(0.4...0.6) * V_{VCC}	1	0
(0.9...1) * V_{VCC}	1	1

2.3.5 Test Modes

Test Mode	T1	T0
Normal operation	0	0
Charge pump output, CHGPMP is in high-impedance state	0	1
P1 = C_y output, P0 = f_{ref} output	1	0
TTL-inputs I1/I0 are C_y / f_{ref} inputs of phase detector	1	1

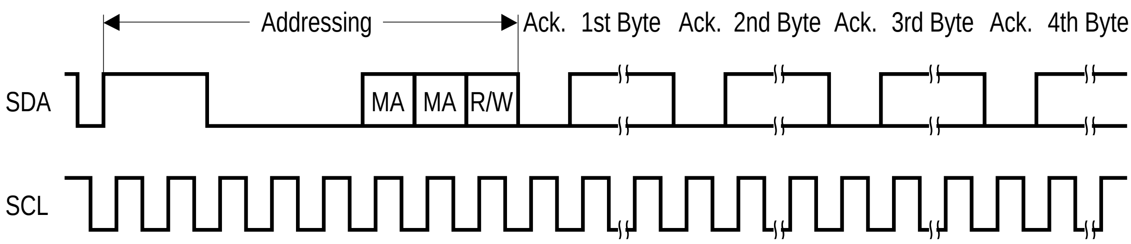
2.3.6 Reference Divider Ratio

Reference Divider Ratio	RSA	RSB
80	x	0
128	0	1
64	1	1

2.3.7 A/D Converter Levels

Voltage at ADC	A2	A1	A0
(0...0.15) * V_{VCC}	0	0	0
(0.15...0.3) * V_{VCC}	0	0	1
(0.3...0.45) * V_{VCC}	0	1	0
(0.45...0.6) * V_{VCC}	0	1	1
(0.6...1) * V_{VCC}	1	0	0

2.3.8 I²C-Bus Timing Diagram



Telegram examples:
Start-Addr-DR1-DR2-CW1-CW2-Stop
Start-Addr-CW1-CW2-DR1-DR2-Stop
Start-Addr-DR1-DR2-Stop
Start-Addr-CW1-CW2-Stop

Abbreviations:
Start = Start Condition
Addr = Address Byte
DR1 = Prog. Divider Byte 1
DR2 = Prog. Divider Byte 2
CW1 = Control Byte 1
CW2 = Control Byte 2
Stop = Stop Condition

UED10804

Figure 3

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Parameter [1)]	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
Supply voltage	V_{VCC}	- 0.3	6	V	
Junction temperature	T_J		150	°C	
Storage temperature	T_{Stg}	- 40	125	°C	
Thermal resistance (junction to ambient)	R_{thSA}		120	K/W	
PLL					
CHGPMP	V_{CHGPMP}	- 0.3	3	V	
	I_{CHGPMP}		1	mA	
Crystal oscillator pins Q	V_Q		V_{VCC}	V	
	I_Q	- 5		mA	
Bus input/output SDA	V_{SDA}	- 0.3	V_{VCC}	V	
Bus output current SDA	$I_{SDA(L)}$		5	mA	Open collector
Bus input SCL	V_{SCL}	- 0.3	V_{VCC}	V	
Chip address switch CAS	V_{CAS}	- 0.3	V_{VCC}	V	
VCO tuning output (loop filter)	V_{TUNE}	- 0.3	35	V	
Port outputs P0...P3	V_P	- 0.3	V_{VCC}	V	
	$I_{P(L)}$	- 1	15	mA	t_{max} = 0.1 s at 5.5 V
Total port output current	$\Sigma I_{P(L)}$		40	mA	t_{max} = 0.1 s at 5.5 V
Mixer-Oscillator					
Mix inputs VHF/HYPER	V_{MIXV}	- 0.3	3	V	
Mix inputs UHF	V_{MIXU}		2	V	
	I_{MIXU}	- 5	6	mA	
VCO base voltage	V_B	- 0.3	3	V	
VCO collector voltage	V_C		V_{VCC}	V	

3.1 Absolute Maximum Ratings (cont'd)

Parameter [1]	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
ESD-Protection [2]					
All pins	V_{ESD}		1	kV	

[1] All values are referred to ground (pin), unless stated otherwise.
Currents with a positive sign flows into the pin and currents with a negative sign flows out of pin.

[2] According to MIL STD 883D, method 3015.7 and EOS/ESD assn. standard S5.1 - 1993

Ambient Temperature under bias: T_A = -20 to 85 °C.

Note: The maximal ratings may not be exceeded under any circumstances, not even momentary and individual, as permanent damage to the IC will result.

3.2 Operating Range

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
Supply voltage	V_{VCC}	4.5	5.5	V	
Programmable divider factor	N	256	32767		
VHF mixer input frequency range	f_{MIXV}	40	500	MHz	
UHF mixer input frequency range	f_{MIXU}	350	90	MHz	
VHF oscillator frequency range	f_{OH}	75	560	MHz	
UHF oscillator frequency range	f_{OU}	380	950	MHz	
Ambient temperature	T_{amb}	- 20	85	°C	

Note: Within the operational range the IC operates as described in the circuit description. The AC/DC characteristic limits are not guaranteed..

3.3 AC/DC Characteristics

Parameter T_A = 25 °C, V_{VCC}	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Supply						
Supply voltage	V_{VCC}	4.5	5	5.5	V	
Current consumption	I_{VCC}	66	70	84	mA	
Digital Unit						
PLL						
Crystal Oscillator Connections Q						
Crystal frequency	f_Q	3.2	4.0	4.8	MHz	Series resonance
Crystal resistance	R_Q	10		100	Ω	Series resonance
Oscillation frequency	f_Q	3.99975	4.000	4.00025	MHz	f_Q = 4 MHz
Input impedance	Z_Q	- 500	- 700	- 900	Ω	f_Q = 4 MHz
Charge Pump Output CHGPMP						
HIGH output current	I_{CPH}	± 90	± 220	± 300	µA	5I = 1, V_{CP} = 2 V
LOW output current	I_{CPL}	± 22	± 50	± 75	µA	5I = 0, V_{CP} = 2 V
Tristate current	I_{CPZ}		1		nA	T0 = 1, V_{CP} = 2 V
Output voltage	V_{CP}	1.0		2.5	V	Locked
Drive Output TUNE (open collector)						
HIGH output current	I_{TH}			10	µA	V_{TH} = 33 V, T0 = 1
LOW output voltage	V_{TL}			0.4	V	I_{TL} = 1.0 mA
I^2C-Bus						
Bus Inputs SCL, SDA						
HIGH input voltage	V_{IH}	3		5.5	V	
LOW input voltage	V_{IL}	0		1.5	V	
HIGH input current	I_{IH}			10	µA	V_{IH} = V_S
LOW input current	I_{IL}	- 10			µA	V_{IL} = 0 V
Bus Output SDA (open collector)						
HIGH output current	I_{OH}			10	µA	V_{OH} = 5.5 V
LOW output voltage	V_{OL}			0.4	V	I_{OL} = 3 mA

3.3 AC/DC Characteristics (cont'd)

Parameter T_A = 25 °C, V_{VCC}	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Edge Speed SCL, SDA						
Rise time	t_r			300	ns	
Fall time	t_f			300	ns	
Clock Timing SCL						
Frequency	f_{SCL}	0		400	kHz	
HIGH pulse width	t_H	0.6			µs	
LOW pulse width	t_L	1.3			µs	
Start Condition						
Set-up time	t_{susta}	0.6			µs	
Hold time	t_{hsta}	0.6			µs	
Stop Condition						
Set-up time	t_{susto}	0.6			µs	
Bus free	t_{buf}	1.3			µs	
Data Transfer						
Set-up time	t_{sudat}	0.1			µs	
Hold time	t_{hdat}	0			µs	
Input hysteresis SCL,SDA	V_{hys}		200		mV	
Pulse width of spikes which are suppressed	t_{sp}	0		50	ns	
Capacitive load for each bus line	C_L			400	pF	
Port Outputs P0, P1, P2, P3 (open collector)						
HIGH output current	I_{POH}			1	µA	V_{POH} = 5 V
LOW output voltage	V_{POL}			0.5	V	I_{POL} = 15 mA
TTL Port Inputs P0, P1						
HIGH input voltage	V_{PIH}	2.7			V	
LOW input voltage	V_{PIL}			0.8	V	
HIGH input current	I_{PIH}			10	µA	V_{PIH} = 5.5 V
LOW input current	I_{PIL}	- 10			µA	V_{PIL} = 0 V

3.3 AC/DC Characteristics (cont'd)

Parameter T_A = 25 °C, V_{VCC}	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
ADC Port Input						
HIGH input current	I_{ADCH}			10	µA	
LOW input current	I_{ADCL}	- 10			µA	
Address Selection Input CAS						
HIGH input current	I_{CASH}			50	µA	V_{CASH} = 5 V
LOW input current	I_{CASL}	- 50			µA	V_{CASL} = 0 V
Analog Unit						
VHF Low and VHF High Band Section (including IF amplifier)						
Voltage gain	G_{MIXV}	20	23	26	dB	f_{RF} = 43.25 to 463.25 MHz, f_{IF} = 33.4 to 58.75 MHz
Mixer noise figure	F_{MIXV}		9	11	dB	f_{RF} = 43.25 to 463.25 MHz
Mixer input impedance	R_{MIXV}	1	2	3	kΩ	Serial equivalent circuit, f_{MIXV} = 100 MHz
	C_{MIXV}		2	3	pF	Serial equivalent circuit, f_{MIXV} = 100 MHz
Oscillator drift, PLL unlocked	Δf_{OscV}			400	kHz	V_S = 5 V ±10%
				500	kHz	ΔT = 25 °C
				100	kHz	t = 5 s up to 15 min after switching on
Oscillator pulling, PLL unlocked	V_{MIXV}	100	108		dBµV	Δf = 10 kHz f_{RF} = 48.25 MHz
		80	88		dBµV	Δf = 10 kHz f_{RF} = 399.25 MHz

3.3 AC/DC Characteristics (cont'd)

Parameter T_A = 25 °C, V_{VCC}	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
N + 5 pulling, PLL unlocked	V_{MIXU}	- 50			dBc	f_{RF} = 48.25 MHz, f_{RF1} = 82.25 MHz, P_{RF} = P_{RF1} = 80 dBµV
	V_{MIXU}	- 50			dBc	f_{RF} = 399.25 MHz, f_{RF1} = 437.25 MHz, P_{RF} = P_{RF1} = 80 dBµV
Oscillator phase noise	$L(f_M)_{VHF}$	- 80	- 86		dBc/ Hz	f_M = 10 kHz, application circuit
IF suppression	a_{IF}	15	20		dB	V_{MIXB} = 80 dBµV
UHF Band Section (including IF amplifier)						
Voltage gain	G_{MIXU}	31	34	37	dB	f_{RF} = 367.25 to 863.25 MHz, f_{IF} = 33.4 to 58.75 MHz
Mixer noise figure	F_{MIXU}		6	9	dB	f_{RF} = 367.25 to 615.25 MHz
			7	10	dB	f_{RF} = 623.25 to 863.25 MHz
Mixer input impedance	R_{MIXU}	14	20	26	Ω	Serial equivalent circuit, f_{MIXU} = 600 MHz
	L_{MIXU}	6	10	14	nH	Serial equivalent circuit, f_{MIXU} = 600 MHz
Oscillator drift, PLL unlocked	Δf_{OscU}			400	kHz	V_S = 5 V ±10%
				800	kHz	ΔT = 25 °C
				100	kHz	t = 5 s up to 15 min after switching on
Oscillator pulling, PLL unlocked	V_{MIXU}	100	108		dBµV	Δf = 10 kHz f_{RF} = 375.25 MHz
		100	108		dBµV	Δf = 10 kHz f_{RF} = 847.25 MHz

3.3 AC/DC Characteristics (cont'd)

Parameter T_A = 25 °C, V_{VCC}	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
N + 5 pulling, PLL unlocked	V_{MIXU}	- 50			dBc	f_{RF} = 471.25 MHz, f_{RF1} = 510.25 MHz, $P_{RF} = P_{RF1}$ = 80 dBµV
	V_{MIXU}	- 50			dBc	f_{RF} = 847.25 MHz, f_{RF1} = 886.25 MHz, $P_{RF} = P_{RF1}$ = 80 dBµV
Oscillator phase noise	$L(f_M)_{UHF}$	- 80	- 86		dBc/Hz	f_M = 10 kHz, application circuit
IF suppression	a_{IF}	15	20		dB	V_{MIXB} = 80 dBµV
SAW Preamplifier						
IF output impedance	R_{IFout}			80	Ω	Serial equivalent circuit, f_{IF} = 38.9 MHz
	L_{IFout}		tbf		nH	
Rejection at the IF Output						
Channel 6 beat	INT_{CH6}	tbf	tbf		dBc	$V_{RFpix} = V_{RFsnd}$ = 80 dBµV [1]
Channel A-5 beat	INT_{CHA-5}	tbf	tbf		dBc	V_{RFpix} = 80 dBµV [2]

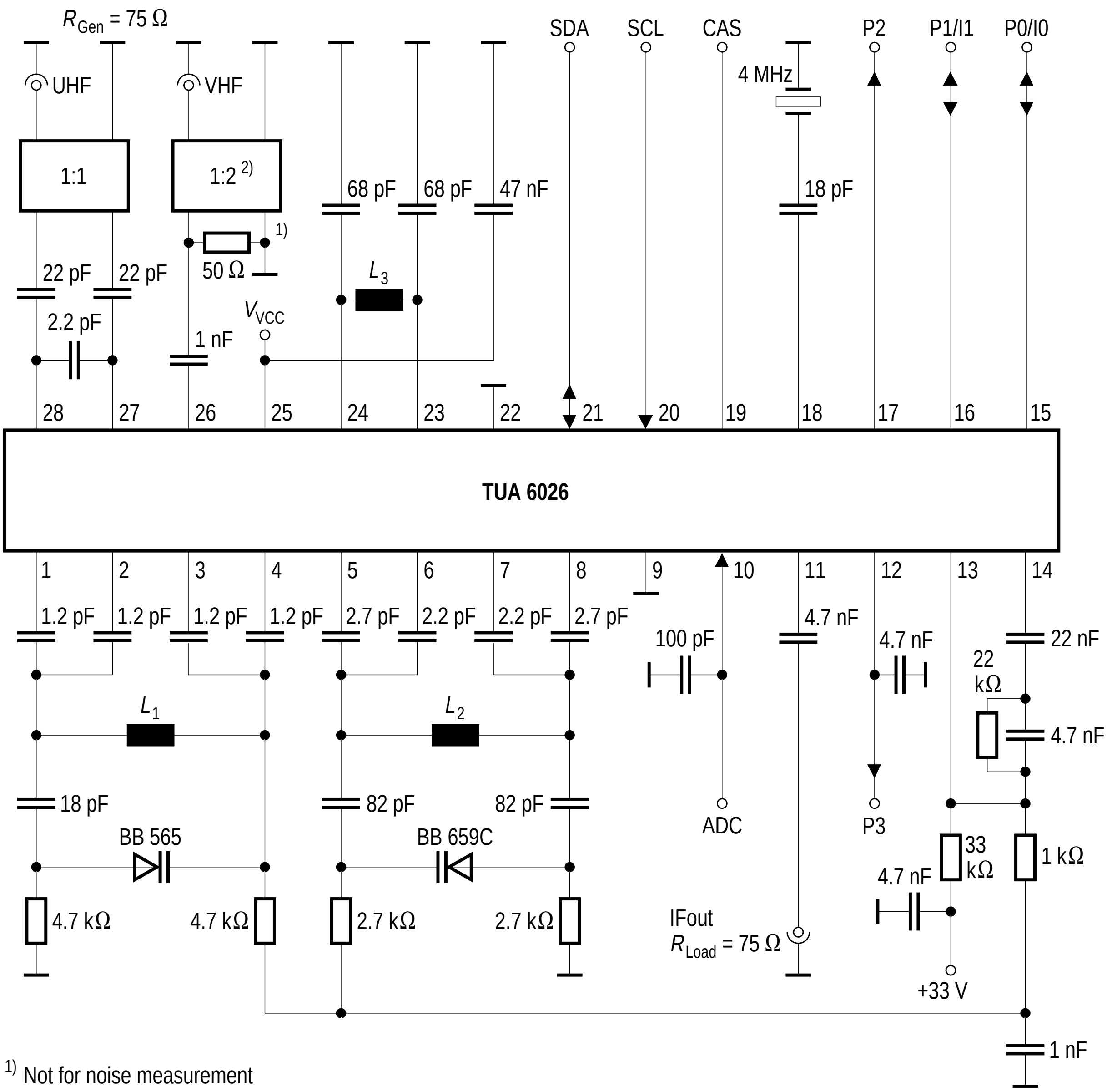
[1] Channel 6 beat is the interfering product of f_{RFpix}, f_{RFsnd} - f_{OSC} of channel 6 at 42 MHz.

[2] Channel A-5 beat is the interfering product of $f_{RFpix} + f_{RFsnd} - f_{OSC}$ of channel A-5, f_{BEAT} = 45.5 MHz.
The possible mechanisms are: $f_{OSC} - 2 \star f_{IF}$ or $2 \star f_{RFpix} - f_{OSC}$. For the measurement V_{RF} = 80 dBµV.

Note: AC/DC characteristics involve the spread of values guaranteed in the specified supply voltage and ambient temperature range. Typical characteristics are the median of the production.

4 Test Circuit

4.1 DC and RF Parameter Measurement



1) Not for noise measurement

2) 1:2 transformer for noise measurement

Figure 4

4.2 Measurement of Crystal Oscillator Frequency

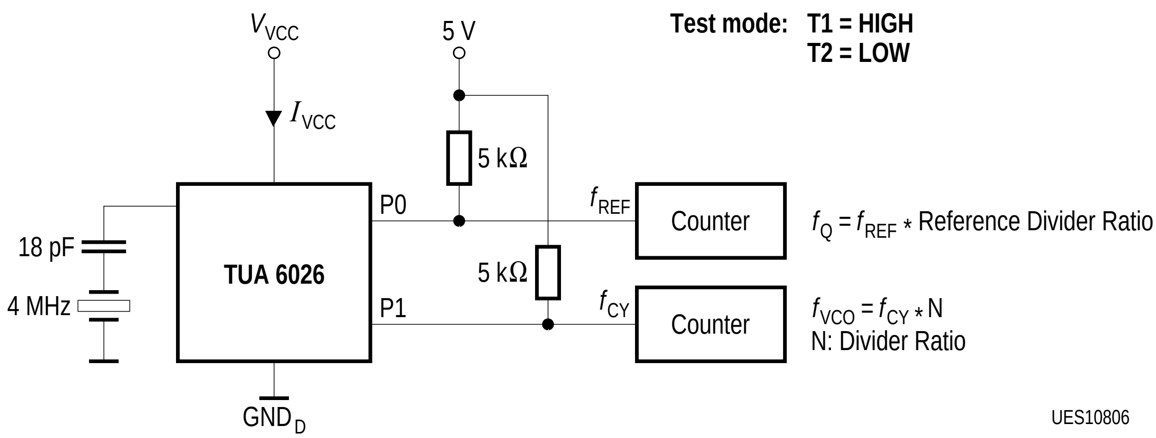
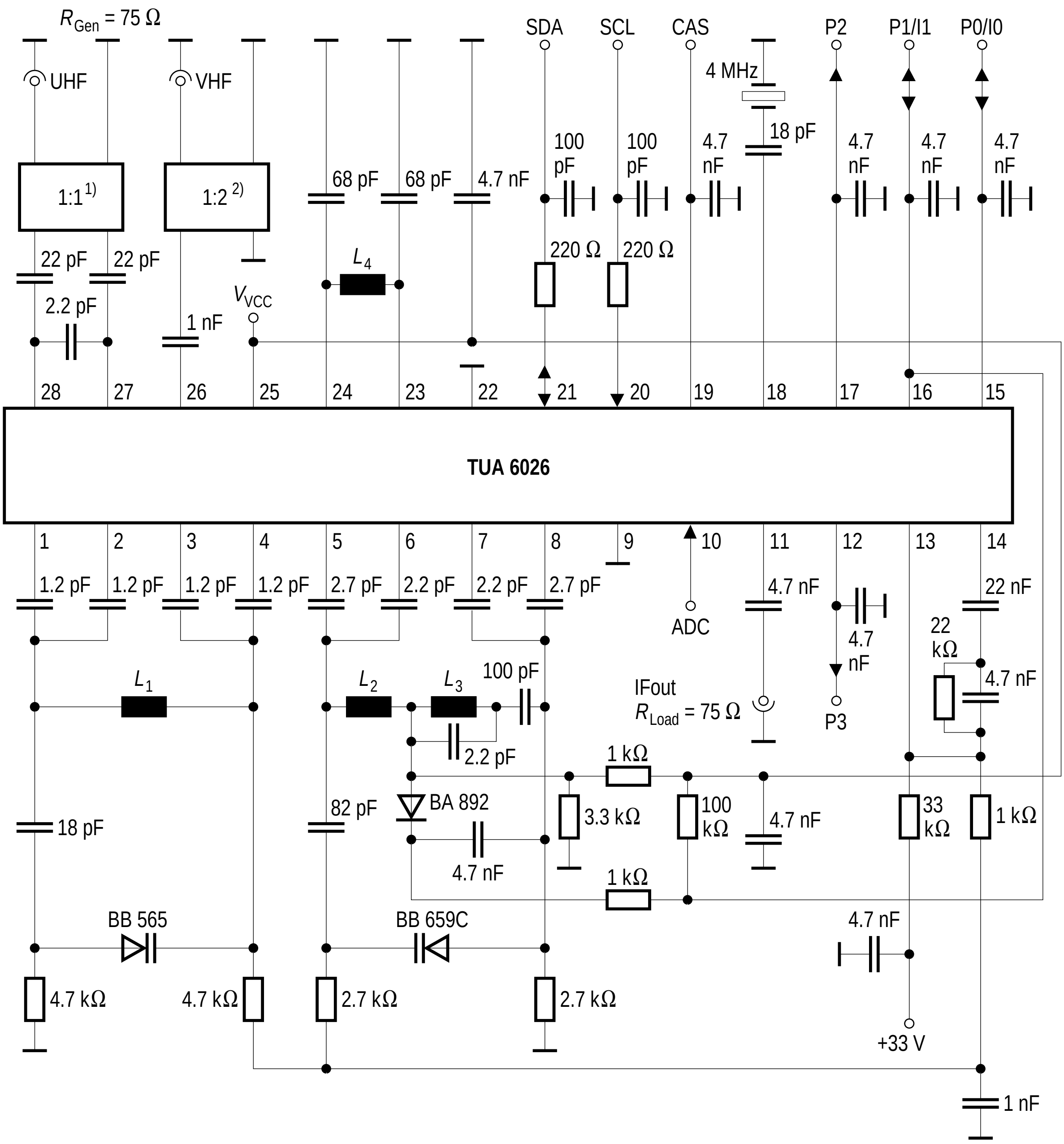


Figure 5

5 Application Circuits

5.1 Application Circuit 1, PAL (evaluation board)



Transformers:
1) TOKO B4F Type 617DB-1023
2) TOKO B4F Type 617PT-1026
3) TOKO 7KL 291GCS-1499F

RF-Bands:
43.25 to 126.25 MHz
133.25 to 423.25 MHz
423.25 to 863.25 MHz

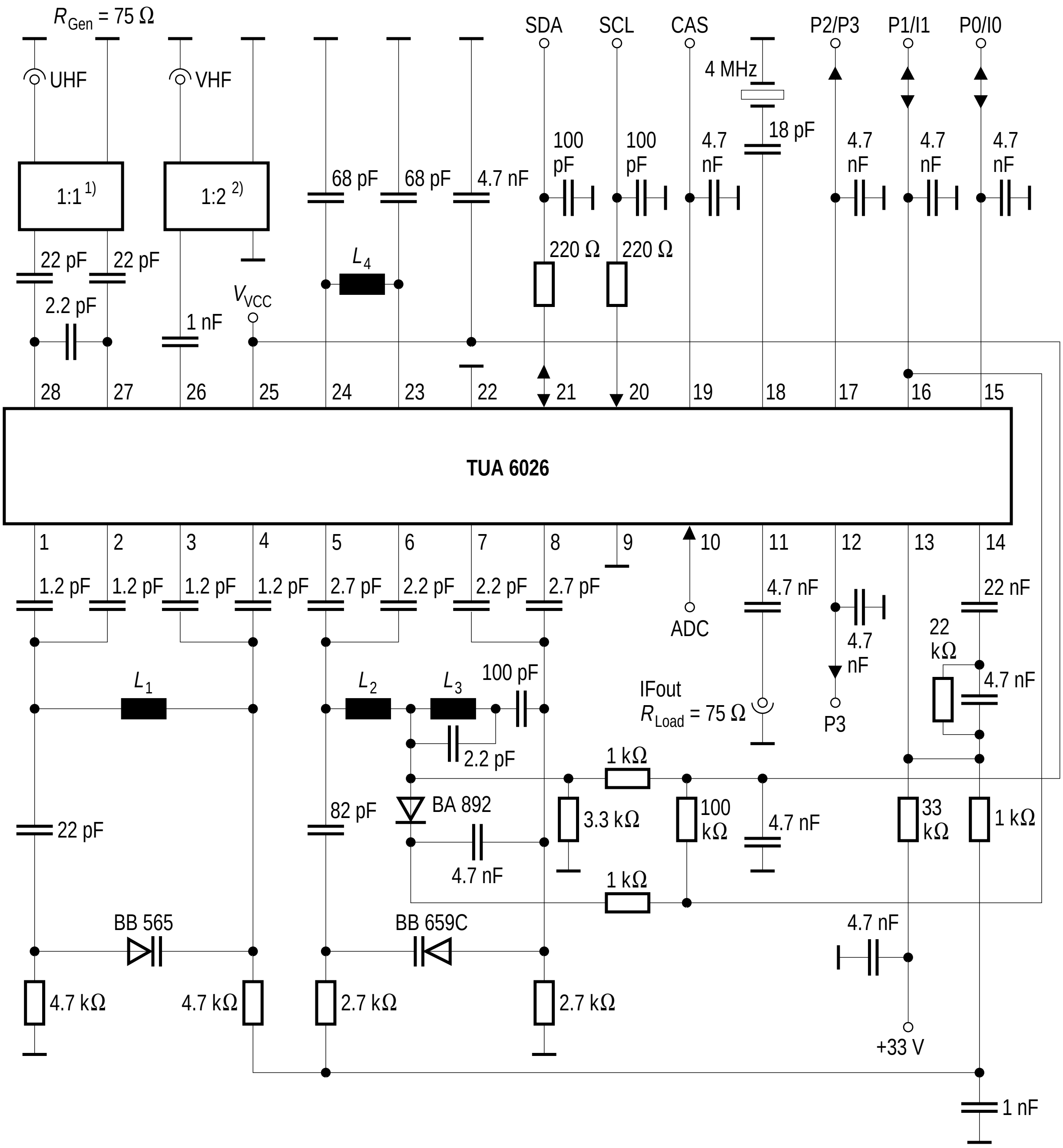
Coils:

Coil	Turns	Wire Size [mm]	Coil Diameter [mm]
L_1	1.5	0.4	2
L_2	2.5	0.5	3
L_3	8.5	0.5	3
L_4	14.5	0.3	4

UES10807

Figure 6

5.2 Application Circuit 2, NTSC (evaluation board)



Transformers:

1) TOKO B4F Type 617DB-1023
2) TOKO B4F Type 617PT-1026
3) TOKO 7KL 291GCS-1499F

RF-Bands:

55.25 to 126.25 MHz
139.25 to 423.25 MHz
367.25 to 801.25 MHz

Coils:

Coil	Turns	Wire Size [mm]	Coil Diameter [mm]
L_1	1.5	0.4	2
L_2	2.5	0.5	3
L_3	8.5	0.5	3
L_4	12	0.3	3.5

UES10808

Figure 7

6 Electrical Diagrams

6.1 Input Admittance VHF Mixer Input Y_0 = 20 ms (single ended)

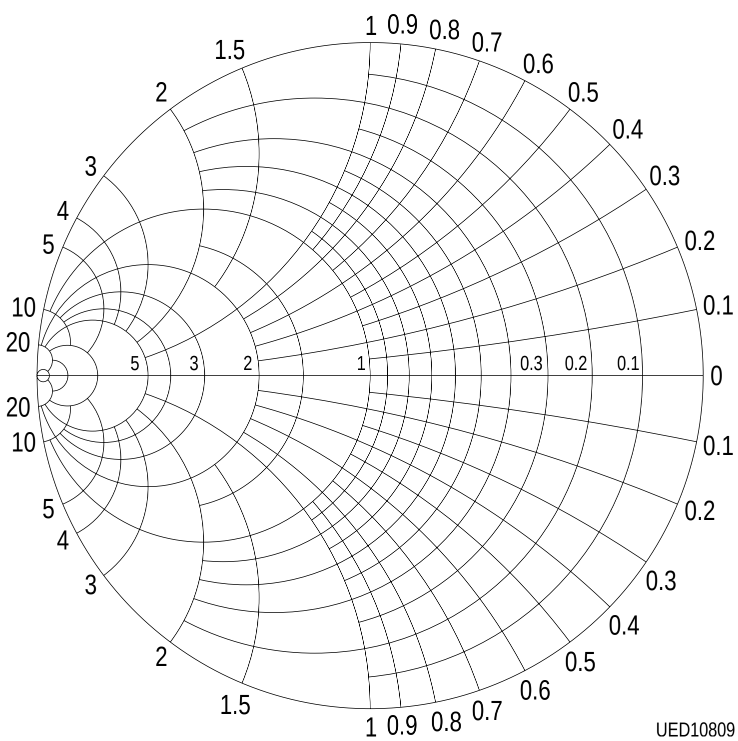


Figure 8

6.2 Input Impedance UHF Mixer Input Z_0 = 50 Ω (symmetrical)

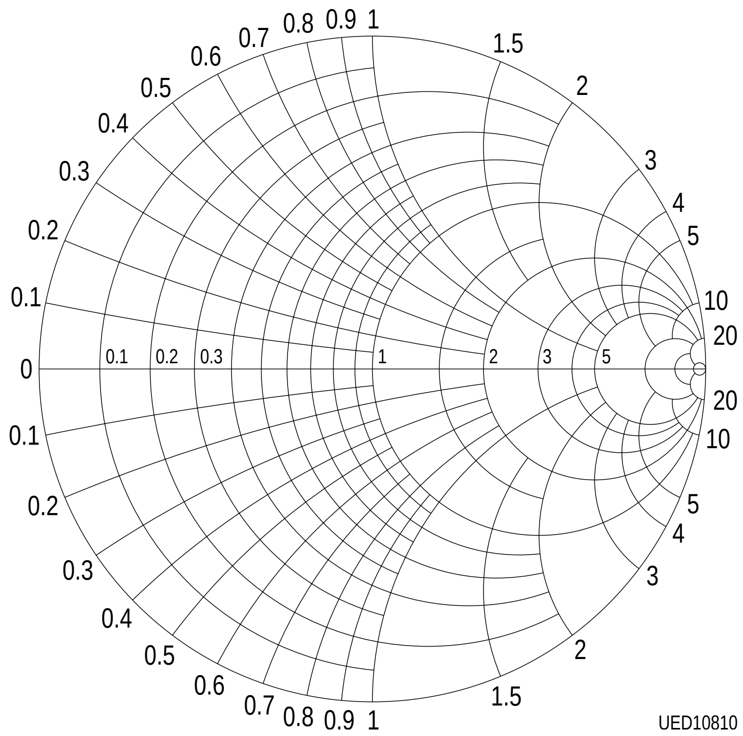


Figure 9

6.3 Output Impedance IF Output Y_0 = 20 ms (single ended)

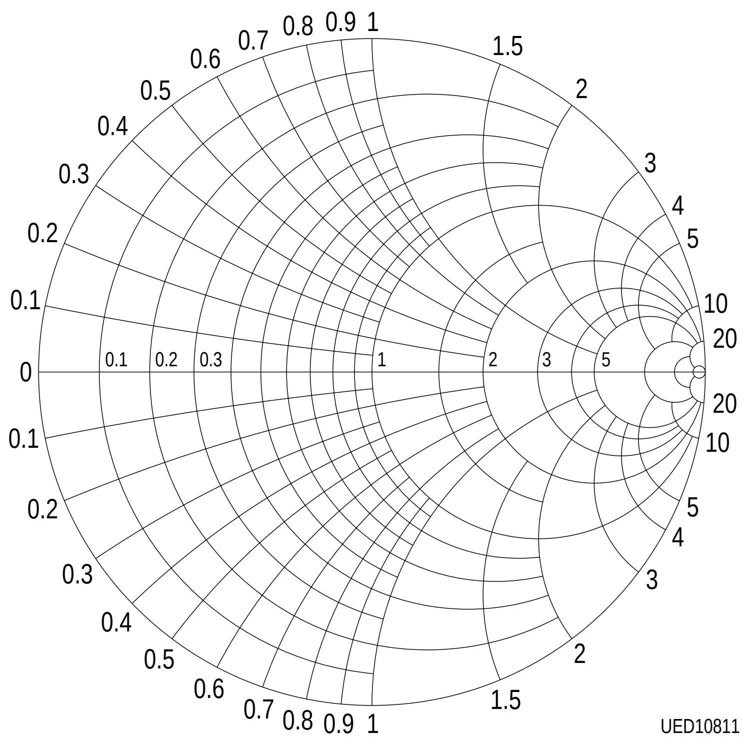
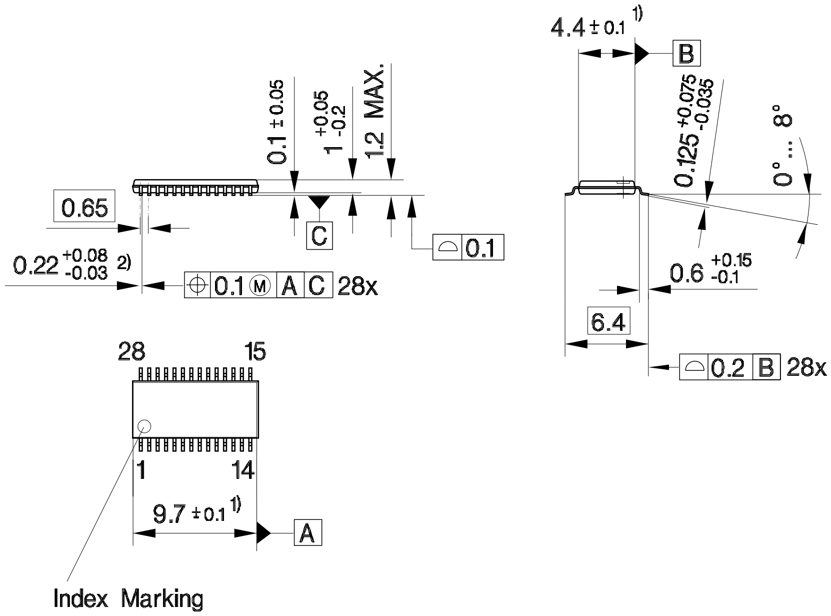


Figure 10

7 Package Outlines

P-TSSOP-28-1
(Plastic Thin Shrink Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion

GPS05867

Figure 11