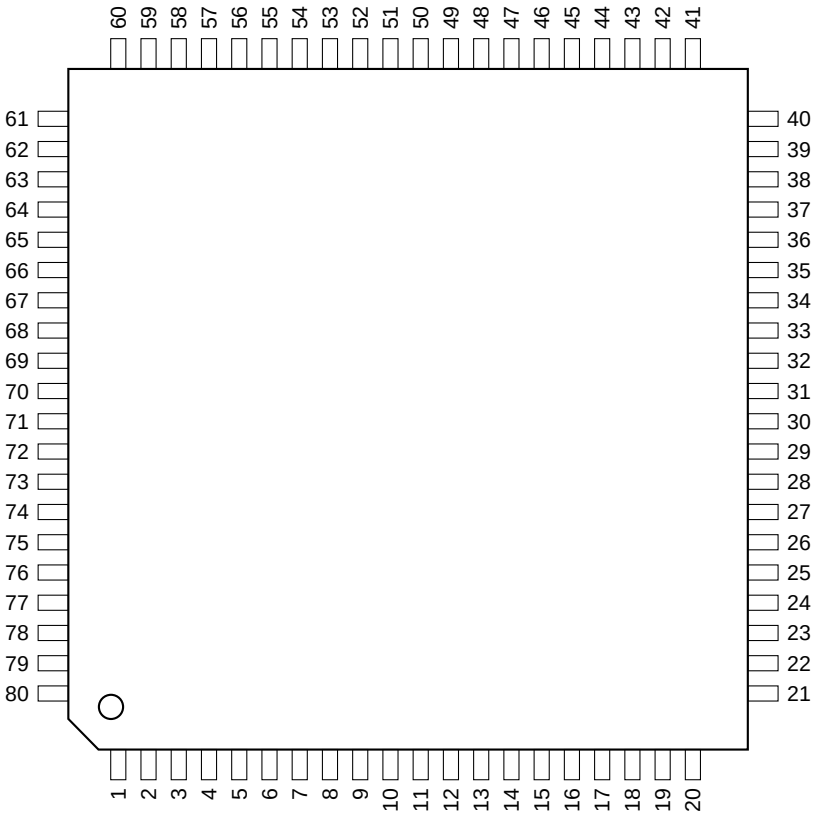
# TRIPLE CABLE TRANSCEIVER/ARBITER

—TOP VIEW—




| PIN NO. | I/O | SIGNAL | PIN NO. | I/O | SIGNAL | PIN NO. | I/O | SIGNAL | PIN NO. | I/O | SIGNAL |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | I | LREQ | 21 | — | DGND | 41 | — | AGND | 61 | — | AGND |
| 2 | O | SYSCLK | 22 | I/O | C/LKON | 42 | I/O | TPB0− | 62 | — | AVCC |
| 3 | — | DGND | 23 | I | PC0 | 43 | I/O | TPB0+ | 63 | — | AVCC |
| 4 | I/O | CTL0 | 24 | I | PC1 | 44 | I/O | TPA0− | 64 | — | AGND |
| 5 | I/O | CTL1 | 25 | I | PC2 | 45 | I/O | TPA0+ | 65 | — | AGND |
| 6 | — | DVCC | 26 | I | $\overline{\text{ISO}}$ | 46 | O | TPBIAS0 | 66 | I | R0 |
| 7 | I/O | D0 | 27 | I | CPS | 47 | — | AVCC | 67 | I | R1 |
| 8 | I/O | D1 | 28 | — | DGND | 48 | — | AVCC | 68 | — | DVCC |
| 9 | — | VCC | 29 | — | DVCC | 49 | I/O | TPB1− | 69 | — | DVCC |
| 10 | I/O | D2 | 30 | — | DVCC | 50 | I/O | TPB1+ | 70 | — | DGND |
| 11 | I/O | D3 | 31 | I | TESTM | 51 | I/O | TPA1− | 71 | I/O | FILTER0 |
| 12 | I/O | D4 | 32 | I | SE | 52 | I/O | TPA1+ | 72 | I/O | FILTER1 |
| 13 | I/O | D5 | 33 | I | SM | 53 | O | TPBIAS1 | 73 | — | PLLVCC |
| 14 | I/O | D6 | 34 | — | AVCC | 54 | — | AVCC | 74 | — | PLLGND |
| 15 | I/O | D7 | 35 | — | AVCC | 55 | I/O | TPB2− | 75 | — | PLLGND |
| 16 | — | DGND | 36 | — | AGND | 56 | I/O | TPB2+ | 76 | I | XI |
| 17 | O | CNA | 37 | — | AGND | 57 | I/O | TPA2− | 77 | O | XO |
| 18 | I | PD | 38 | — | AGND | 58 | I/O | TPA2+ | 78 | I | $\overline{\text{RESET}}$ |
| 19 | I | LPS | 39 | — | AGND | 59 | O | TPBIAS2 | 79 | — | DVCC |
| 20 | — | DGND | 40 | — | AGND | 60 | — | AGND | 80 | — | DGND |

**INPUTS**

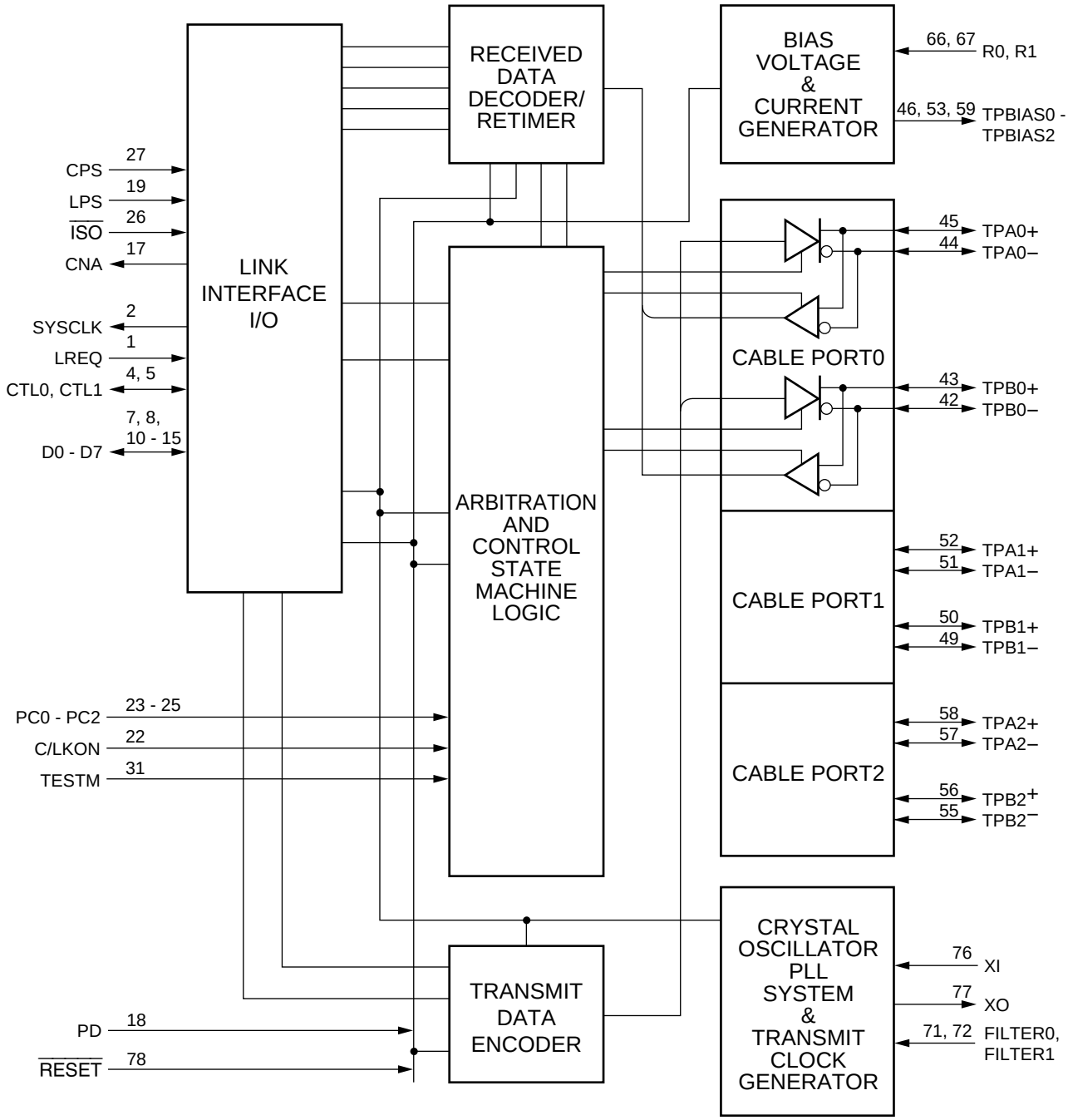
| | | |
|---|---|---|
| CPS | : | CABLE POWER STATUS |
| $\overline{\text{ISO}}$ | : | LINK INTERFACE ISOLATION CONTROL |
| LPS | : | LINK POWER STATUS |
| LREQ | : | LINK REQUEST |
| PC0 - PC2 | : | POWER CLASS |
| PD | : | POWER DOWN |
| R0, R1 | : | CURRENT SETTING RESISTOR |
| $\overline{\text{RESET}}$ | : | LOGIC RESET |
| SE | : | TEST CONTROL |
| SM | : | TEST CONTROL |
| TESTM | : | TEST MODE CONTROL |
| XI | : | CRYSTAL OSCILLATOR |

**OUTPUTS**

| | | |
|---|---|---|
| CNA | : | CABLE NOT ACTIVE |
| SYSCLK | : | SYSTEM CLOCK |
| TPBIAS0 - TPBIAS2 | : | PORT N, TWISTED PAIR BIAS |
| XO | : | CRYSTAL OSCILLATOR |

**INPUTS/OUTPUTS**

| | | |
|---|---|---|
| C/LKON | : | BUS MANAGER CONTENDER PROGRAMMING/LINK ON |
| CTL0, CTL1 | : | CONTROL |
| FILTER | : | PLL FILTER |
| D0 - D7 | : | DATA |
| TPA0+ - TPA2+ | : | PORT N, TWISTED PAIR CABLE A POSITIVE SIGNAL |
| TPA0– - TPA2– | : | PORT N, TWISTED PAIR CABLE A NAGATIVE SIGNAL |
| TPB0+ - TPB2+ | : | PORT N, TWISTED PAIR CABLE B POSITIVE SIGNAL |
| TPB0– - TPB2– | : | PORT N, TWISTED PAIR CABLE B NAGATIVE SIGNAL |


RECEIVED DATA DECODER/ RETIMER
BIAS VOLTAGE & CURRENT GENERATOR
66, 67
R0, R1
46, 53, 59
TPBIAS0 - TPBIAS2
LINK INTERFACE I/O
CPS
27
LPS
19
ISO
26
CNA
17
SYSCLK
2
LREQ
1
CTL0, CTL1
4, 5
D0 - D7
7, 8, 10 - 15
ARBITRATION AND CONTROL STATE MACHINE LOGIC
CABLE PORT0
45
TPA0+
44
TPA0–
43
TPB0+
42
TPB0–
CABLE PORT1
52
TPA1+
51
TPA1–
50
TPB1+
49
TPB1–
CABLE PORT2
58
TPA2+
57
TPA2–
56
TPB2+
55
TPB2–
PC0 - PC2
23 - 25
C/LKON
22
TESTM
31
CRYSTAL OSCILLATOR PLL SYSTEM & TRANSMIT CLOCK GENERATOR
76
XI
77
XO
71, 72
FILTER0, FILTER1
TRANSMIT DATA ENCODER
PD
18
RESET
78