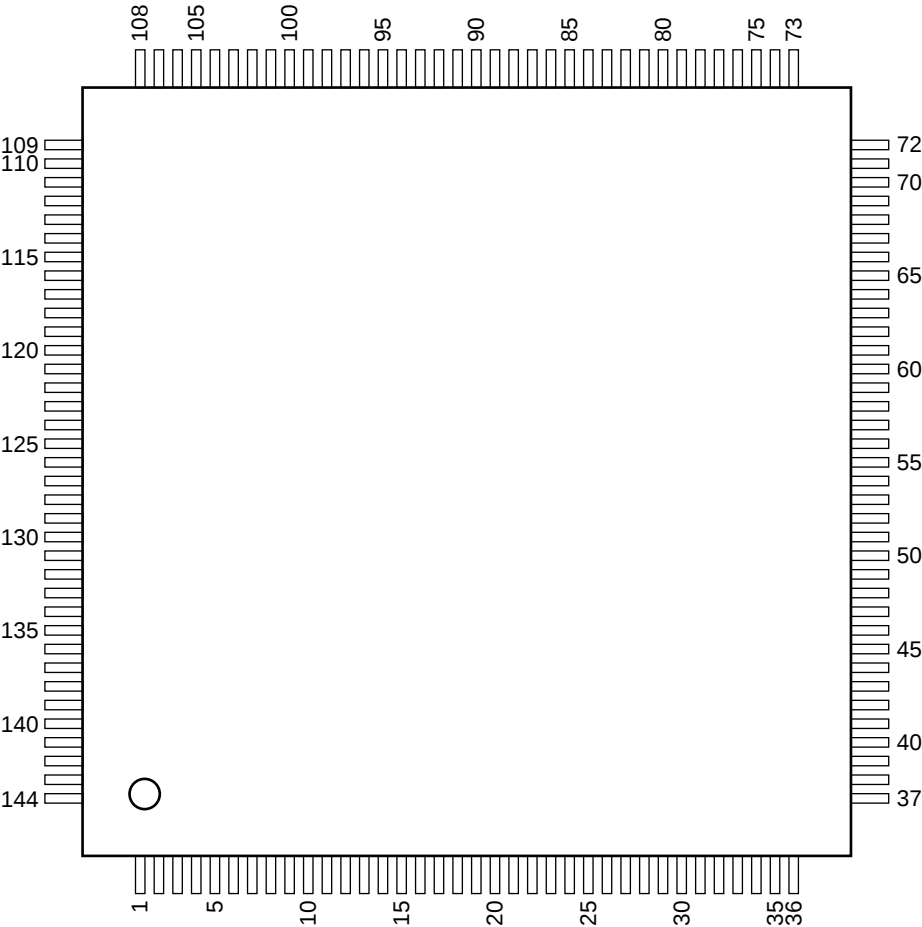


IEEE1394 SERIAL BUS LINK LAYER

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	GND	37	O	FMSWCK	73	—	GND	109	O	MCCLK
2	I	DSPYIN0	38	O	FMRSTW	74	I/O	PHD7	110	I	MCB8B16
3	I	DSPYIN1	39	O	FMWEEV	75	I/O	PHD6	111	I/O	MCDATA0
4	I	DSPYIN2	40	O	FMWEOD	76	I/O	PHD5	112	I/O	MCDATA1
5	I	DSPYIN3	41	—	Vcc	77	I/O	PHD4	113	I/O	MCDATA2
6	—	Vcc	42	I	FMQEV0	78	—	Vcc	114	I/O	MCDATA3
7	I	DSPYIN4	43	I	FMQEV1	79	I/O	PHD3	115	—	GND
8	I	DSPYIN5	44	I	FMQEV2	80	I/O	PHD2	116	I/O	MCDATA4
9	I	DSPYIN6	45	I	FMQEV3	81	I/O	PHD1	117	I/O	MCDATA5
10	I	DSPYIN7	46	—	Vcc	82	I/O	PHD0	118	I/O	MCDATA6
11	—	GND	47	I	FMQEV4	83	—	GND	119	I/O	MCDATA7
12	I	DSPCIN0	48	I	FMQEV5	84	I/O	PHCTL1	120	—	Vcc
13	I	DSPCIN1	49	I	FMQEV6	85	I/O	PHCTL0	121	I/O	MCDATA8
14	I	DSPCIN2	50	I	FMQEV7	86	—	VCC	122	I/O	MCDATA9
15	I	DSPCIN3	51	—	GND	87	I	PHSCLK	123	I/O	MCDATA10
16	—	Vcc	52	I	FMQOD0	88	—	GND	124	I/O	MCDATA11
17	I	DSPCIN4	53	I	FMQOD1	89	O	PHLREQ	125	—	Vcc
18	I	DSPCIN5	54	I	FMQOD2	90	—	GND	126	I/O	MCDATA12
19	I	DSPCIN6	55	I	FMQOD3	91	I	DSPDCKEN	127	I/O	MCDATA13
20	I	DSPCIN7	56	—	Vcc	92	—	GND	128	I/O	MCDATA14
21	—	GND	57	I	FMQOD4	93	I	MSNTBIHIZ	129	I/O	MCDATA15
22	I	DSPHD	58	I	FMQOD5	94	O	MSNTOUT	130	—	Vcc
23	I	DSPVD	59	I	FMQOD6	95	I	DSPDCK	131	I	MCCS
24	I	DSPFLD	60	I	FMQOD7	96	—	Vcc	132	O	MCCA
25	I	DSPCK	61	—	GND	97	O	CYST	133	I	MCWR
26	—	Vcc	62	O	FMSRCK	98	I	MCADD0	134	O	MCINT
27	O	FMD0	63	O	FMRSTR	99	I	MCADD1	135	—	GND
28	O	FMD1	64	O	FMREEV	100	I	MCADD2	136	O	MCARXD
29	O	FMD2	65	O	MSRSV	101	I	MCADD3	137	O	MCPREARXD
30	O	FMD3	66	O	FMREOD	102	—	GND	138	I	MCBUSY
31	—	Vcc	67	—	Vcc	103	I	MCADD4	139	I	MCDMAEN
32	O	FMD4	68	O	GRFEMP	104	I	MCADD5	140	—	Vcc
33	O	FMD5	69	O	POWERON	105	I	MCADD6	141	O	MCISOACT
34	O	FMD6	70	O	MSCYLOUT	106	I	MCADD7	142	O	CYDNE
35	O	FMD7	71	I	MSCYLIN	107	—	Vcc	143	I	MSDMARST
36	—	GND	72	I	MSRAMEZ	108	I	MCBCLK	144	I	RESET

INPUTS

DSPCIN0 - DSPCIN7	: VIDEO DATA
DSPCK	: DSP OUTPUT SYNCHRONIZATION CLOCK
DSPDCK	: 2 × DSPCK
DSPDCKEN	: WDMA WRITE I/F CLOCK
DSPFLD	: ODD/EVEN FIELD INDICATOR
DSPHD	: HORIZONTAL SYNC
DSPVD	: VERTICAL SYNC
DSPYIN0 - DSPYIN7	: VIDEO DATA
FMQEV0 - FMQEV7	: EVEN FIELD MEMORY FIFO DATA
FMQOD0 - FMQOD7	: ODD FIELD MEMORY FIFO DATA
MCADD0 - MCADD7	: ADDRESS BUS
MCB8B16	: DATA BUS WIDTH SELECTOR
MCBCLK	: HOST BUS CLOCK
MCBUSY	: BUSY
MCCS	: CYCLE START
MCDMAEN	: DMA ENABLE
MCWR	: WRITE/READ
MSCYLIN	: CYCLE
MSDMARST	: SYNCHRONOUS RESET
MSNTBIHIZ	: NAND TREE BIDIRECTIONAL 3-STATE
MSRAMEZ	: RAM 3-STATE ENABLE
PHSCLK	: SYSTEM CLOCK
RESET	: ASYNCHRONOUS RESET

OUTPUTS

CYDNE	: ISO CYCLE DONE
CYST	: ISO CYCLE START
FMD0 - FMD7	: FIELD MEMORY FIFO DATA
FMREEV	: INCREMENTS FIELD MEMORY READ ADDRESS POINTER FOR EVEN FIELD
FMREOD	: INCREMENTS FIELD MEMORY READ ADDRESS POINTER FOR ODD FIELD
FMRSTR	: RESET FIELD MEMORY READ ADDRESS POINTER
FMRSTW	: RESET FIELD MEMORY WRITE ADDRESS POINTER
FMSRCK	: MEMORY READ CLOCK
FMSWCK	: MEMORY 1/2 WRITE CLOCK
FMWEEV	: FIFO EVEN FIELD WRITE ENABLE
FMWEOD	: FIFO ODD FIELD WRITE ENABLE
GRFEMP	: GRF EMPTY
MCARXD	: ASYNC PACKET
MCCA	: CYCLE ACKNOWLEDGE
MCCLK	: MICROCONTROLLER CLOCK
MCINT	: INTERRUPT
MCISOACT	: DMA STATUS
MCPREARXD	: PRE ASYNC PACKET
MSCYLOUT	: CYCLE
MSNTOUT	: NAND TREE
MSRSV	: (RESERVED)
PHLREQ	: LINK REQUEST
POWERON	: LINK POWER ON

INPUTS/OUTPUTS

MCDATA0 - MCDATA15	: DATA
PHCTL0, PHCTL1	: CONTROL
PHD0 - PHD7	: DATA BUS

