SIEMENS

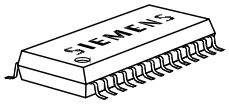
CAN-LDO

TLE 6263 G

Target Data

Features

- Standard fault tolerant differential CAN-transceiver
- Bus failure management
- Low power mode management
- CAN data transmission rate up to 125 kBaud
- Low-dropout voltage 5 V regulator for internal and external supply; tolerance ± 2%
- High Side Switche
- Power on and under-voltage reset generator
- Window watchdog
- Programable time base
- Standard 8 bit SPI-Interface
- Wide input voltage range
- Wide temperature range
- Enhanced power P-DSO-Package



P-DSO-28-6
Enhanced Power

Type	Ordering Code	Package
▼ TLE 6263 G	on request	P-DSO-28-6 (SMD)

▼ New type

Functional Description

The TLE 6263 G is a monolithic integrated circuit in a P-DSO-28-6 package, which incorporates a failure tolerant low speed CAN-transceiver for differential mode data transmission, a low dropout voltage regulator for internal and external 5V supply as well as a SPI (serial peripheral interface) to control and monitor the IC. Further there are integrated a high side switch, a wake-up input, a window watchdog circuit as well as a reset and early warning feature. Both, the window watchdog and reset function are referring to a time base that is programmable via an external resistor.

The IC is designed to withstand the severe conditions of automotive applications.

Pin Configuration (not yet fixed)
(top view)

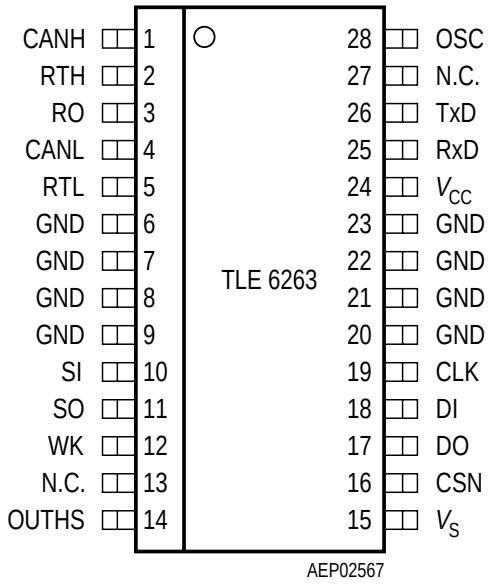


Figure 1

Pin Definitions and Functions

Pin No.	Symbol	Function
	CANH	**H Bus Line**; HIGH in dominant state
	RTH	**Termination Input** for CANH
	RO	**Reset Output**; integrated pull up
	CANL	**L Bus Line**; LOW in dominant state
	RTL	**Termination Input** for CANL
6, 7, 8, 9, 20, 21, 22, 23	GND	**Ground**; to reduce thermal resistance place cooling areas on PCB close to this pins.
	SI	**Early Warning Input**
	SO	**Early Warning Output;** internal pull up
	WK	**Wake-Up Input;** for wake-up via external contacts
	N.C.	not connected
	OUTHS	**High Side Output**; controlled via SPI, in sleep mode optionaly controlled by internal autotiming function
	V_S	**Power Supply**; block to GND directly at the IC with ceramic capacitor
	CSN	**SPI Interface Chip Select Not**; CSN is an active low input; serial communication is enabled by pulling the CSN terminal low; CSN input should only be transitioned when CLK is low; CSN has an internal active pull up and requires CMOS logic level inputs
	DO	**SPI Interface Data Out**; this tristate output transfers diagnosis data to the control device; the output will remain 3-stated unless the device is selected by a low on Chip-Select-Not (CSN); see **Table 2** for Diagnosis protocol
	DI	**SPI Interface Data In**; receives serial data from the control device; serial data transmitted to DI is a 16 bit control word with the Least Significant Bit (LSB) being transferred first: the input has an active pull down and requires CMOS logic level inputs; DI will accept data on the falling edge of CLK-signal; see **Table 1** for input data protocol.
	CLK	**SPI Interface Clock Input**; clocks the shiftregister; CLK has an internal active pull down and requires CMOS logic level inputs

Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Function
	V_{CC}	**Output Voltage Regulator**; 5 V logic supply, block to GND with an external capacitor $C_Q \geq 10\ \mu F$, ESR > 1 Ω
	RxD	**Receive Data Output;** integrated pull up
	TxD	**Transmit Data Input;** integrated pull up
	N.C.	not connected
	OSC	**Oscillator Input**; time base for power on reset, watchdog window and stand by timer for HS3, to program connect external resistor to GND

Functional Block Diagram

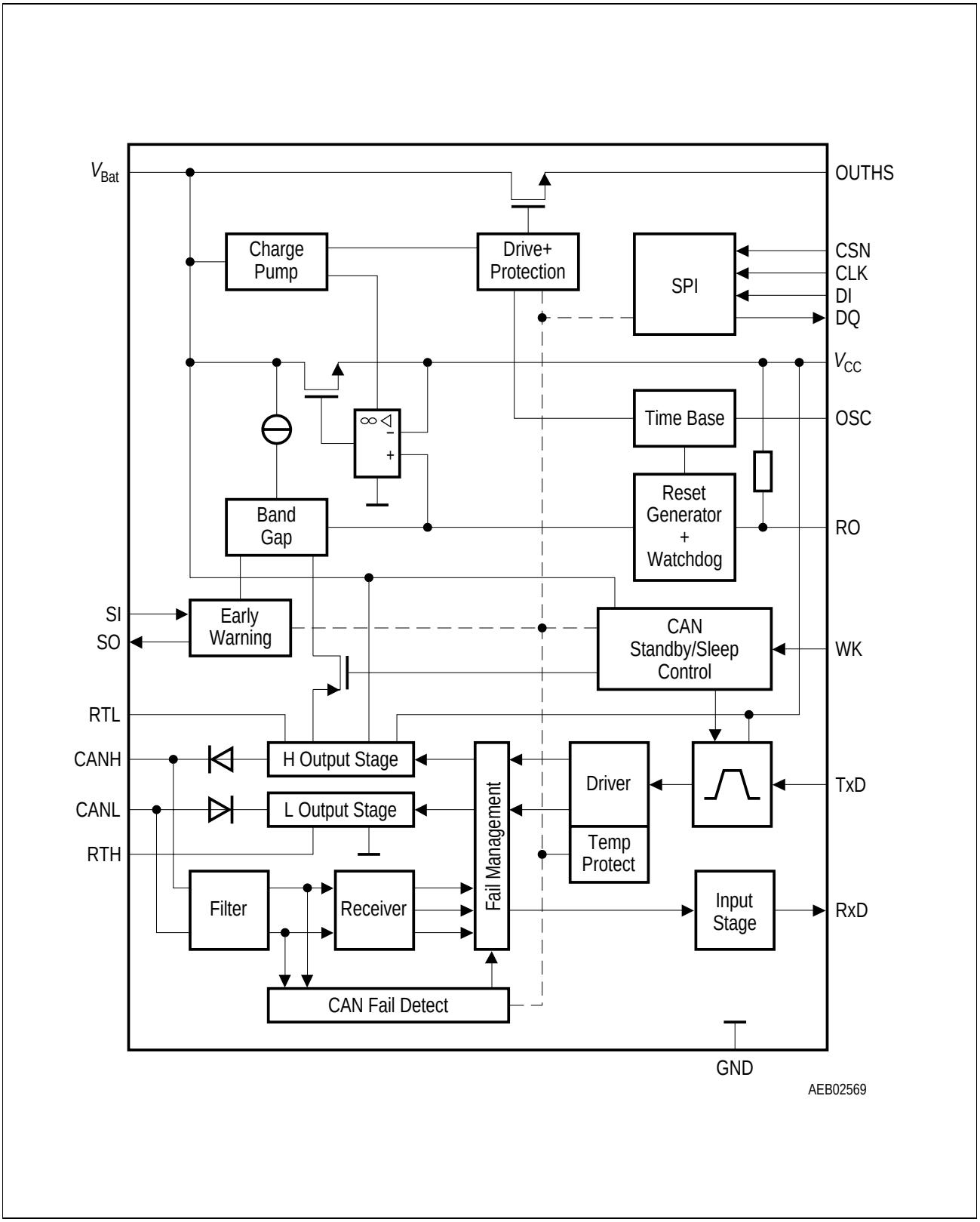


Figure 2

Circuit Description

The TLE 6263 G is a monolithic IC, which incorporates a failure tolerant low speed CAN-transceiver for differential mode data transmission, a low dropout voltage regulator for internal and external 5 V supply as well as a SPI (serial periperal interface) to control and monitor the IC. Further there are integrated a high side switche, a wake-up input, a window watchdog circuit as well as a reset circuit and early warning function. Both, the window watchdog and reset function are referring to a time base that is programmable via an external resistor.

Figure 2 shows a block schematic diagram of the TLE 6263 G.

CAN Transceiver

Apart from the following deviations the CAN transceiver integrated in the TLE 6263 G is identical to the stand-alone transceiver TLE 6252:

A pin NERR for flagging any failure does not exist. The bus failures according to **Table 3** can be monitored via the diagnosis protocol of the SPI interface. Therefore it is possible to distinguish 6 CAN bus failures or failure groups on the bits 8 to 13 (see **Table 2**).

When setting the transceiver into sleep mode the internal and external 5 V supplies are automatically disabled. This feature can be masced via the SPI input bit 7.

Setting/waking up of the CAN-transceiver into/from sleep mode or stand-by mode is done via the SPI interface (bits 2 and 3, see **Table 1**). When a reset occurs the transceiver circuit is switched to V_{bat}-stand-by mode because the SPI input bits are automatically set LOW for this event.

Wake-Up Input

In addition to a wake-up via the bus lines CANH or CANL it is also possible to wake-up the application via the Wake-up input WK.

Low Dropout Voltage Regulator

The TLE 6262 is able to drive external 5 V loads up to typ. 100 mA. Its output voltage tolerance is less than $\pm$ 2%.

An external reverse current protection is recommended to prevent the output capacitor from being discharged by negative transients or low input voltage.

Stability of the output voltage is guaranteed for output capacitors $C_Q \geq 100$ nF. Nevertheless a lot of applications require a much larger output capacitance to buffer the output voltage in case of low input voltage or negative transients. Furthermore the due function of e.g. the reset and early warning circuit circuit is supported by a larger output capacitance because of their reaction times. Therefore a output capacitance $C_Q \geq 10$ µF, ESR > 1 Ω is recommended.

SPI (Serial Peripheral Interface)

The 8-bit wide programming word or input word (see **Table 1**) is read in via the data input DI, and this is synchronised with the clock input CLK supplied by the µC. The diagnosis word appears synchronously at the data output DO (see **Table 2**).

The transmision cycle begins when the chip is selected by the chip select not input CSN (H to L). After the CSN input returns from L to H, the word that has been read in becomes the new control word. The DO output switches to tristate status at this point, thereby releasing the DO bus circuit for other uses.

For details of the SPI timing please refer to **Figure 3 to Figure 6**.

Oscillator

All internal delay times are referring to the internal oscillator frequency, which is set by an external resistor from pin OSC to GND. The oscillator frequency and the resulting internal cycling time can be calculated by the equations:

$$f_{OSC} = 35.9 \times 10^6\ [\text{Hz}\Omega]/R_{OSC}$$

$$t_{CYL} = 32/f_{OSC}$$

Window Watchdog, Reset

When the input voltage exceeds the reset threshold voltage the reset output RO is switched HIGH after a delay time of 16 cycles. This is necessary for a defined start of the microcontroller when the application is switched on. As soon as an under-voltage condition of the output voltage ($V_{CC} < V_{RT}$) appears, the reset output RO is switched LOW again. The LOW signal is guaranteed down to an output voltage $V_Q \geq 1$ V. Please refer to **Figure 9**, reset timing diagram.

After the above described delayed reset (LOW to HIGH transitition of RO) the window watchdog circuit is started. Now the microcontroller has to service a watchdog trigger signal via the SPI interface (input bit 0) after a closed window of 16 cycles. A watchdog trigger is detected as a falling edge by sampling a HIGH followed by a LOW of the SPI input bit 0. If the trigger signals do not meet the open window (16 cycles) following the closed window, the reset output RO is set LOW for a periode of 4 cycles. In addition, the SPI diagnosis bit 1 is set HIGH to monitor a watchdog reset. A correct watchdog service immediately results in starting the next closed window. Please refer to **Figure 8**, watchdog timing diagram.

Both, the undervoltage reset and the watchdog reset are setting all SPI input bits LOW.

To avoid a cyclic wake-up of the microcontroller in low power mode (sleep mode) the watchdog circuit can be automatically disabled at low output currents ($I_{CC} < I_{CCWD}$). To activate this feature the SPI input bit 1 has to be set HIGH. In this under-current mode the low side switches are switched off by the TLE 6261. When the microcontroller returns

back to normal mode ($I_{CC} > I_{CCWD}$) the first closed window is transformed to an open window so that the total open window time is 32 cycles. This ensures a simple synchronisation of the watchdog timing to the watchdog services.

Early Warning

This sense comparator can e.g. be used to supervise the input voltage V_S to give the microcontroller a prewarning before an undervoltage reset due to low input voltage occures. The prewarning is indicated by setting the sense out SO low. To activate this featrue, the sense out has to be set high via the SPI input bit 6.

High Side Switch

The high side output OUTHS is able to switch loads up to 150 mA. Its on-resistance is 1.0 Ω typ. @ 25 °C. This switch is controlled via the SPI input bits 4 and 5. In normal mode and stand-by mode the high side output is swiched on resp. off via bit 5. To supply external wake-up circuits in sleep mode the output OUTHS can be periodically switched on by the internal oscillator circuit. For activating this feature the SPI input bits 4 and 5 have be set high. The autotiming period then is 128 internal cycle times; the on-time is 2 cycles. In case of a watchdog reset the autotiming period is shortened.

The SPI diagnosis bit 0 flaggs a thermal prewarning. By this the microcontroller is able to reduce the power dissipation of the TLE 6263 G by switching off functions of minor priority until the temperature threshold of the thermal shutdown is reached. Further OUTH1 is protected against short circuit and overload. As soon as the under-voltage condition of the supply voltage is met ($V_S < V_{UVOFF}$), the switch is automatically disabled by the under-voltage lockout circuit. Moreover the switch is disabled when a reset occurs.

Table 1
Input Data Protocol (H = ON, L = OFF)

BIT	
7	Mask Inhibit
6	Early Warning Enable
5	OUTHS ON
4	OUTHS Auto Timing
3	Not Standby
2	Enable Transmit
1	Watchdog Control
0	Watchdog Trigger

Table 2
Diagnosis Data Protocoll (H = ON, L = OFF)

Bit	
7	CAN Failure 2 and 4
6	CAN Failure 1 and 3a
5	CAN Failure 6
4	CAN Failure 6a
3	CAN Failure 6a, 5 and 7
2	CAN Failure 3
1	Window Watchdog Reset
0	Temperature Prewarning

Table 3
CAN Bus Line Failure Cases (According to ISO 11519-2)

Failure #	**Failure Description**
1	CANL line interrupted
2	CANH line interrupted
3	CANL shorted to V_{bat}; CANH > 7.2 V
3a (no ISO failure)	CANL shorted to V_{bat}; 2.2 V < CANH < 7.2 V
4	CANH shorted to GND
5	CANL shorted to GND
6	CANH shorted to V_{bat}; CANL > 7.2 V
6a (no ISO failure)	CANH shorted to V_{bat}; 2.2 V < CANL < 7.2 V
7	CANL shorted to CANH

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Voltages					
Supply voltage	V_S	– 0.3	28	V	–
Supply voltage	V_S	– 0.3	40	V	t_p< 0.5 s; t_p/T < 0.1
Regulator output voltage	V_{CC}	– 0.3	5.5	V	–
CAN input voltage (CANH, CANL)	$V_{CANH/L}$	– 10	27	V	–
CAN input voltage (CANH, CANL)	$V_{CANH/L}$	– 40	40	V	V_S >0 V t_p< 0.5 s; t_p/T < 0.1
Logic input voltages (DI, CLK, CSN, OSC, TxD)	V_I	– 0.3	V_{CC} + 0.3	V	0 V < V_S < 24 V 0 V < V_{CC} < 5.5 V
Logic output voltage (DO, RO, SO, RxD)	$V_{DRSO,RD}$	– 0.3	V_{CC} + 0.3	V	0 V < V_S < 24 V 0 V < V_{CC} < 5.5 V
Termination input voltage (RTH, RTL)	$V_{TL/TH}$	– 0.3	V_S + 0.3	V	0 V < V_S < 24 V 0 V < V_{CC} < 5.5 V
Input voltages at WK and SI	$V_{WK/SI}$	– 0.3	28	V	–
Input voltages at WK and SI	$V_{WK/SI}$	– 0.3	40	V	t_p< 0.5 s; t_p/T < 0.1
Currents					
Output current; V_{CC}	I_{CC}	–	–	A	internally limited
Output current; OUTHS	I_{OUTH1}	*	0.2	A	* internally limited
Temperatures					
Junction temperature	T_j	– 40	150	°C	–
Storage temperature	T_{stg}	– 50	150	°C	–

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	$V_{UV\ OFF}$	28	V	After V_S rising above $V_{UV\ ON}$
Supply voltage slew rate	dV_S/dt	– 0.5	5	V/µs	–
Logic input voltage (DI, CLK, CSN, TxD)	V_I	– 0.3	V_{CC}	V	–
Output capacitor	C_{CC}	10	–	µF	–
C_{CC}-Series Resistor	R_{ESR}	–	10	Ω	T_a = – 40 °C; f = 10 kHz
SPI clock frequency	f_{CLK}	–	1	MHz	–
Junction temperature	T_j	– 40	150	°C	–

Thermal Resistances

Junction pin	$R_{thj\text{-}pin}$	–	25	K/W	measured to pin 7
Junction ambient	$R_{thj\text{-}a}$	–	65	K/W	–

Electrical Characteristics

9 V < V_S < 16 V; I_{CC} = 1 mA; normal mode; all outputs open; – 40 °C < T_j < 150 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Quiescent current Pin V_S						
Current consumption	I_S	–	5	–	mA	–
Quiescent current $I_{SSB1} = I_S - I_{CC}$	I_{SSB1}	–	–	100	µA	sleep mode; V_S = 12 V; T_j = 25 °C
Quiescent current $I_{SSB2} = I_S - I_{CC}$	I_{SSB2}	–	–	3	mA	OUTHS active; sleep mode; V_S = 12 V; T_j = 25 °C
Voltage Regulator; Pin V_{CC}						
Output voltage	V_{CC}	4.9	5.0	5.1	V	0.1 mA < I_{CC} < 100 mA
Output voltage	V_{CC}	4.8	5.00	5.5	V	0 A < I_{CC} < 100 µA
Line regulation	ΔV_{CC}	–	–	50	mV	6 V < V_S < 16 V; I_{CC} = 1 mA
Load regulation	ΔV_{CC}	–	–	50	mV	5 mA < I_{CC} < 100 mA; V_S = 6 V
Power supply ripple rejection	$PSRR$	tbd	40	–	dB	V_S < 1 V_{SS}; C_Q ≥ 10 µF 100 Hz < f < 100 kHz
Output current limt	I_{CCmax}	110	–	–	mA	Note 1
Dropvoltage $V_{DR} = V_S - V_{CC}$	V_{DR}	–	–	0.5	V	I_{CC} = 80 mA; Note 1

1) measured when the output voltage V_{CC} has dropped 100 mV from the nominal value obtained at 13.5 V input voltage V_S

Electrical Characteristics (cont'd)

9 V < V_S < 16 V; I_{CC} = 1 mA; normal mode; all outputs open; – 40 °C < T_j < 150 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Oscillator; Pin OSC						
Adjust resistor	R_{OSC}	51	–	680	kΩ	–
Oscillating frequency	f_{OSC}	52.8	70.4	88.0	kHz	R_{OSC} = 510 kΩ
Internal cycling time $(1/32 \times f_{OSC})^{-1}$	t_{CYL}	0.363	0.454	0.606	ms	R_{OSC} = 510 kΩ
Reset Generator; Pin RO						
Reset threshold voltage	V_{RT}	4.0	4.3	4.6	V	–
Reset low output voltage	V_{RO}	–	0.2	0.4	V	I_{RO} = 1 mA ($V_{CC} \geq V_{RT}$) or $V_{CC} \geq$ 1 V (I_{RO} = 200 µA)
Reset high output voltage	V_{RO}	4.0	–	V_{CC} + 0.1	V	–
Reset pull up current	I_{RO}	20	150	500	µA	V_{RO} = 0 V
Reset reaction time	t_{RR}	1	3	10	µs	$V_{CC} < V_{RT}$ to RO = L
Reset delay time (16 cyl.)	t_{RD}	5.8	7.3	10.6	ms	R_{OSC} = 510 kΩ
Early Warning						
Sense In threshold voltage	V_{ST}	–	2.5	–	V	V_S > 3 V
Sense Out low voltage	V_{SO}	–	0.2	0.4	V	I_{SO} = 1 mA ($V_{CC} \geq V_{RT}$)
Sense Out high voltage	V_{SO}	4.0	–	V_{CC} + 0.1	V	–
Sense pull up current	I_{RO}	20	150	500	µA	V_{SO} = 0 V
Sense reaction time	t_{SR}	–	5	–	µs	$V_S < V_{ST}$ to SO = low

Electrical Characteristics (cont'd)

9 V < V_S < 16 V; I_{CC} = 1 mA; normal mode; all outputs open; – 40 °C < T_j < 150 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Watchdog Generator						
Watchdog time (22 cyl.)	t_{WD}	8.0	10	13.3	ms	R_{OSC} = 510 kΩ
Closed window time (16 cyl.)	t_{CW}	5.8	7.3	10.6	ms	R_{OSC} = 510 kΩ
Open window time (16 cyl.)	t_{OW}	5.8	7.3	10.6	ms	R_{OSC} = 510 kΩ
Watchdog reset-puls time (4 cyl.)	t_{WDR}	1.5	1.8	2.4	ms	R_{OSC} = 510 kΩ
Watchdog activating current	I_{CCWD}	2	4	7	mA	T_j < 85 °C; Watchdog OFF when I_{CC} < I_{CCWD} and SPI-bit 1 = H
Watchdog activating current hysteresis	$I_{CCWDhys}$	–	0.5	–	mA	–
Long open window (32 cyl.)	$I_{CCWDhys}$	11.2	14.6	21.2	ms	R_{OSC} = 510 kΩ sleep mode (WD OFF) to normal mode

Electrical Characteristics (cont'd)

9 V < V_S < 16 V; I_{CC} = 1 mA; normal mode; all outputs open; – 40 °C < T_j < 150 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
High Side Output OUTHS; (Controlled by Bit 4 and Bit 5 of SPI Input Word)						
Static Drain-Source ON-Resistance; I_{OUTH3} = – 0.15 A	$R_{DSON\ HS}$	–	1.0	1.5	Ω	T_j = 25 °C
			–	3.0	Ω	–
			2.5	3.0	Ω	5.2 V ≤ V_S ≤ 9 V T_j = 25 °C
			–	5.0	Ω	5.2 V ≤ V_S ≤ 9 V
Active zener voltage	V_{OUTHS}	–	– 3	–	V	I_{OUTHS} = – 0.15 A
Clamp diode forward voltage	V_{OUTHS}	–	–	1	V	I_{OUTHS} = 0.15 A
Leakage current	I_{QLHS}	– 100	–	–	µA	V_{OUTHS} = 0 V
Switch ON delay time	t_{dONHS}	–	–	100	µs	CSN high to OUTHS
Switch OFF delay time	t_{dOFFHS}	–	–	100	µs	CSN high to OUTHS
Overcurrent shutdown threshold	I_{SDHS}	– 0.8	– 0.4	– 0.2	A	–
Shutdown delay time	t_{dSDHS}	10	25	40	µs	–
Current limit	I_{OCLHS}	– 1.2	– 0.6	– 0.3	A	–
UV-Switch-ON voltage	$V_{UV\ ON}$	–	5.35	6.00	V	V_S increasing
UV-Switch-OFF voltage	$V_{UV\ OFF}$	4.50	4.85	5.20	V	V_S decreasing
UV-ON/OFF-Hysteresis	$V_{UV\ HY}$	–	0.5	–	V	$V_{UV\ ON} - V_{UV\ OFF}$
Auto time periode (128 cyl.)	t_{PHS}	29	58	87	ms	R_{OSC} = 510 kΩ; SPI-bit 4/5 = H, no WD reset
Auto time ON duty cycle (2 cyl.)	D.C.	–	1/64	–	–	refering to t_{PHS}

Electrical Characteristics (cont'd)

9 V < V_S < 16 V; I_{CC} = 1 mA; normal mode; all outputs open; – 40 °C < T_j < 150 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
SPI-Interface **Logic Inputs DI, CLK and CSN**						
H-input voltage threshold	V_{IH}	–	–	0.7 * V_{CC}	V	–
L-input voltage threshold	V_{IL}	0.2 * V_{CC}	–	–	V	–
Hysteresis of input voltage	V_{IHY}	50	200	500	mV	–
Pull up current at pin CSN	I_{ICSN}	– 100	– 25	– 5	µA	$V_{CSN} = 0.7 \times V_{CC}$
Pull down current at pin DI and CLK	$I_{ICLK/DI}$	5	25	100	µA	$V_{DI} = 0.2 \times V_{CC}$
Pull down current at pin CLK	I_{ICLK}	10	25	50	µA	$V_{CLK} = 0.2 \times V_{CC}$
Input capacitance at pin CSN, DI or CLK	C_I	–	10	15	pF	0 V < V_{CC} < 5.25 V
Logic Output DO						
H-output voltage level	V_{DOH}	V_{CC} – 1.0	V_{CC} – 0.7	–	V	I_{DOH} = 1 mA
L-output voltage level	V_{DOL}	–	0.2	0.4	V	I_{DOL} = – 1.6 mA
Tri-state leakage current	I_{DOLK}	– 10	–	10	µA	$V_{CSN} = V_{CC}$ 0 V < V_{DO} < V_{CC}
Tri-state input capacitance	C_{DO}	–	10	15	pF	$V_{CSN} = V_{CC}$ 0 V < V_{CC} < 5.25 V

Electrical Characteristics (cont'd)

9 V < V_S < 16 V; I_{CC} = 1 mA; normal mode; all outputs open; – 40 °C < T_j < 150 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Data Input Timing						
Clock period	t_{pCLK}	1000	–	–	ns	–
Clock high time	t_{CLKH}	500	–	–	ns	–
Clock low time	t_{CLKL}	500	–	–	ns	–
Clock low before CSN low	t_{bef}	500	–	–	ns	–
CSN setup time	t_{lead}	500	–	–	ns	–
CLK setup time	t_{lag}	500	–	–	ns	–
Clock low after CSN high	t_{beh}	500	–	–	ns	–
DI setup time	t_{DISU}	250	–	–	ns	–
DI hold time	t_{DIHO}	250	–	–	ns	–
Input signal rise time at pin DI, CLK and CSN	t_{rIN}	–	–	200	ns	–
Input signal fall time at pin DI, CLK and CSN	t_{fIN}	–	–	200	ns	–
Data Output Timing						
DO rise time	t_{rDO}	–	50	100	ns	C_L = 100 pF
DO fall time	t_{fDO}	–	50	100	ns	C_L = 100 pF
DO enable time	t_{ENDO}	–	–	250	ns	low impedance
DO disable time	t_{DISDO}	–	–	250	ns	high impedance
DO valid time	t_{VADO}	–	100	250	ns	V_{DO} < 0.1 V_{CC}; V_{DO} > 0.9 V_{CC}; C_L = 100 pF

Electrical Characteristics (cont'd)

9 V < V_S < 16 V; I_{CC} = 1 mA; normal mode; all outputs open; – 40 °C < T_j < 150 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Thermal Prewarning and Shutdown (Junction Temperatures)						
Thermal prewarning ON temperature	T_{jPW}	120	145	170	°C	bit 0 of SPI diagnosis word
Thermal prewarning hyst.	ΔT	–	30	–	K	–
Thermal shutdown temp.	T_{jSD}	150	175	200	°C	–
Thermal switch-on temp.	T_{jSO}	120	–	170	°C	–
Thermal shutdown hyst.	ΔT	–	30	–	K	–
Ratio of SD to PW temp.	T_{jSD}/T_{jPW}	1.05	1.20	–	–	–

Timing Diagrams

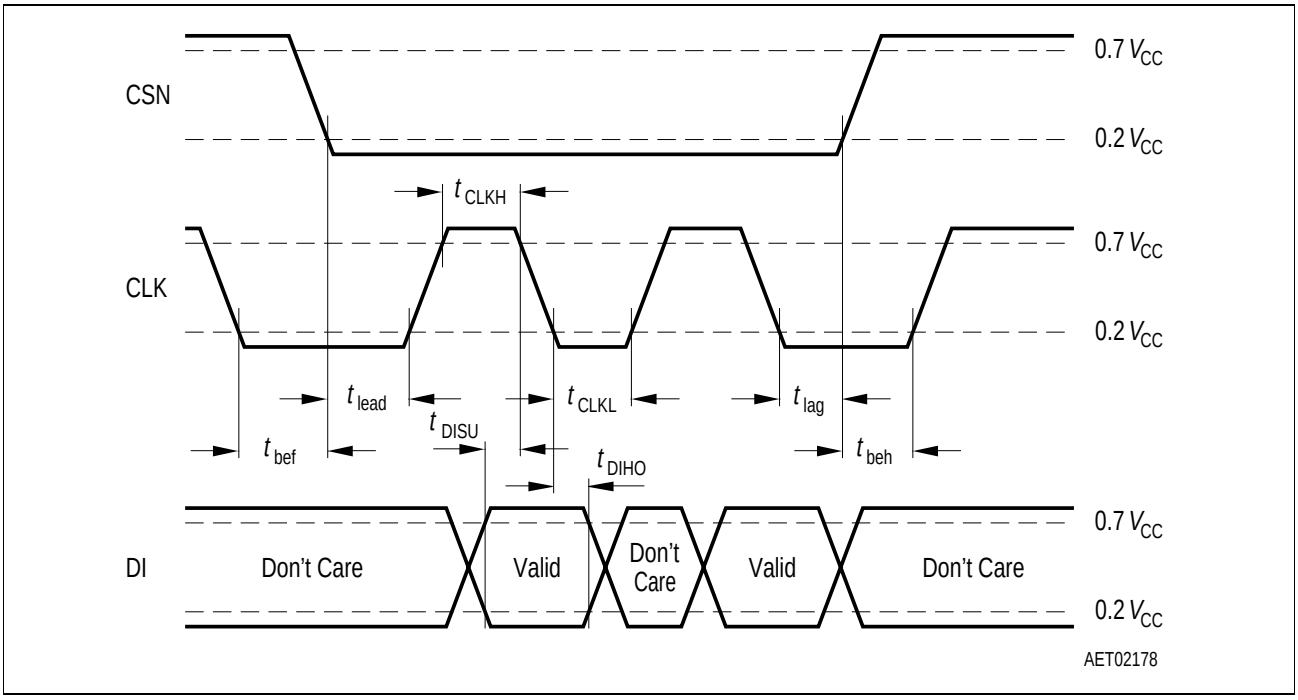


Figure 3
SPI-Input Timing

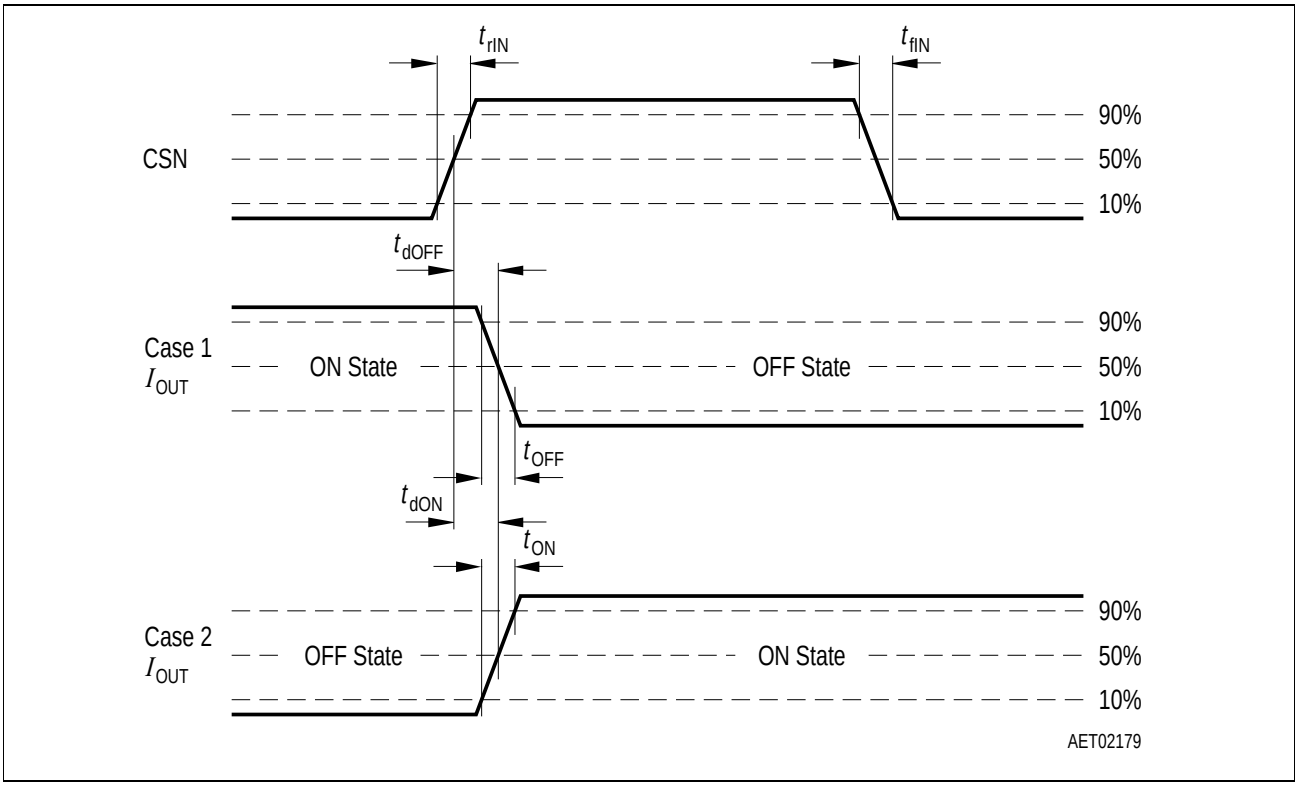


Figure 4
Turn OFF/ON Time

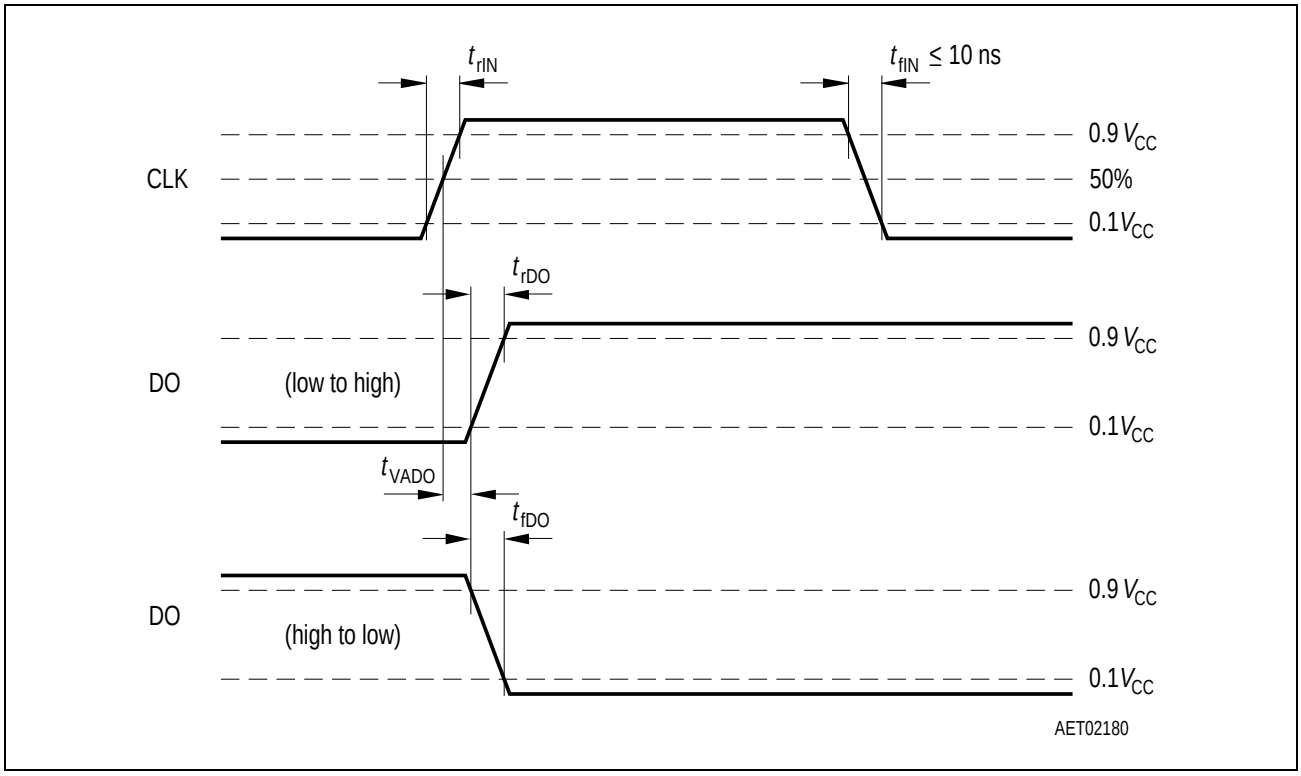


Figure 5
DO Valid Data Delay Time and Valid Time

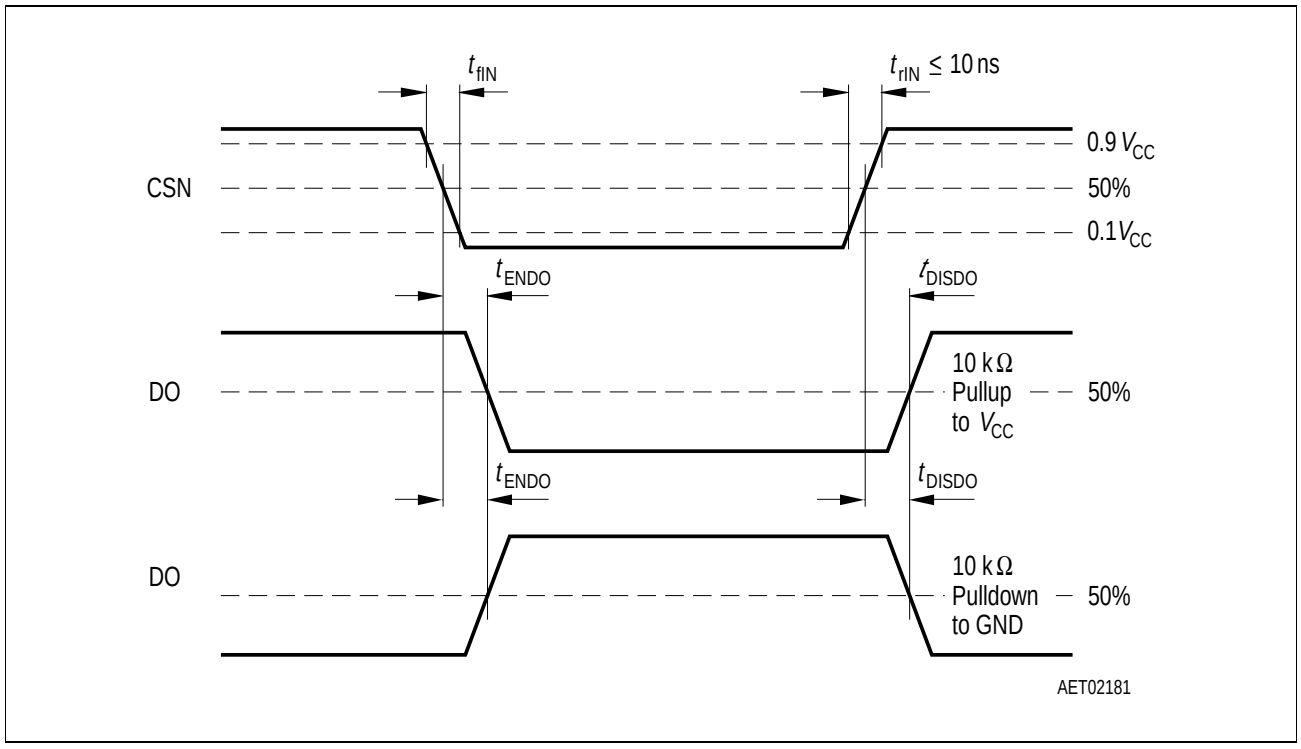


Figure 6
DO Enable and Disable Time

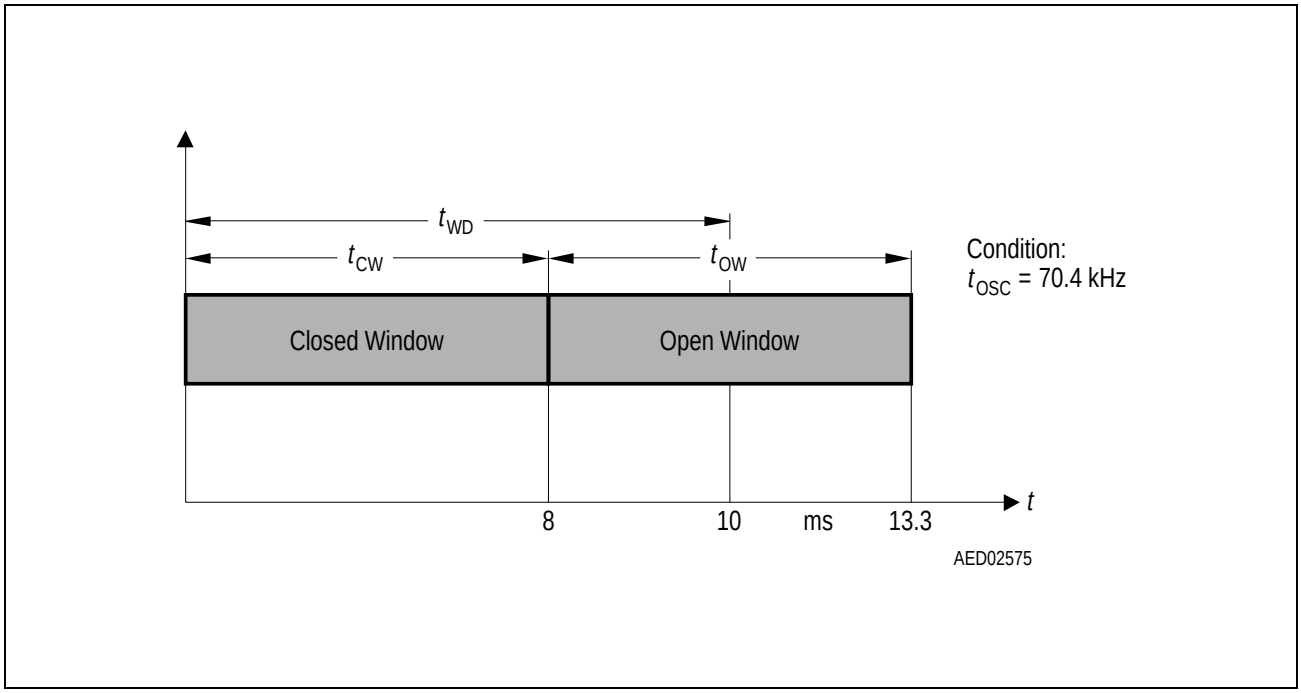


Figure 7
Watchdog Timeout Definitions

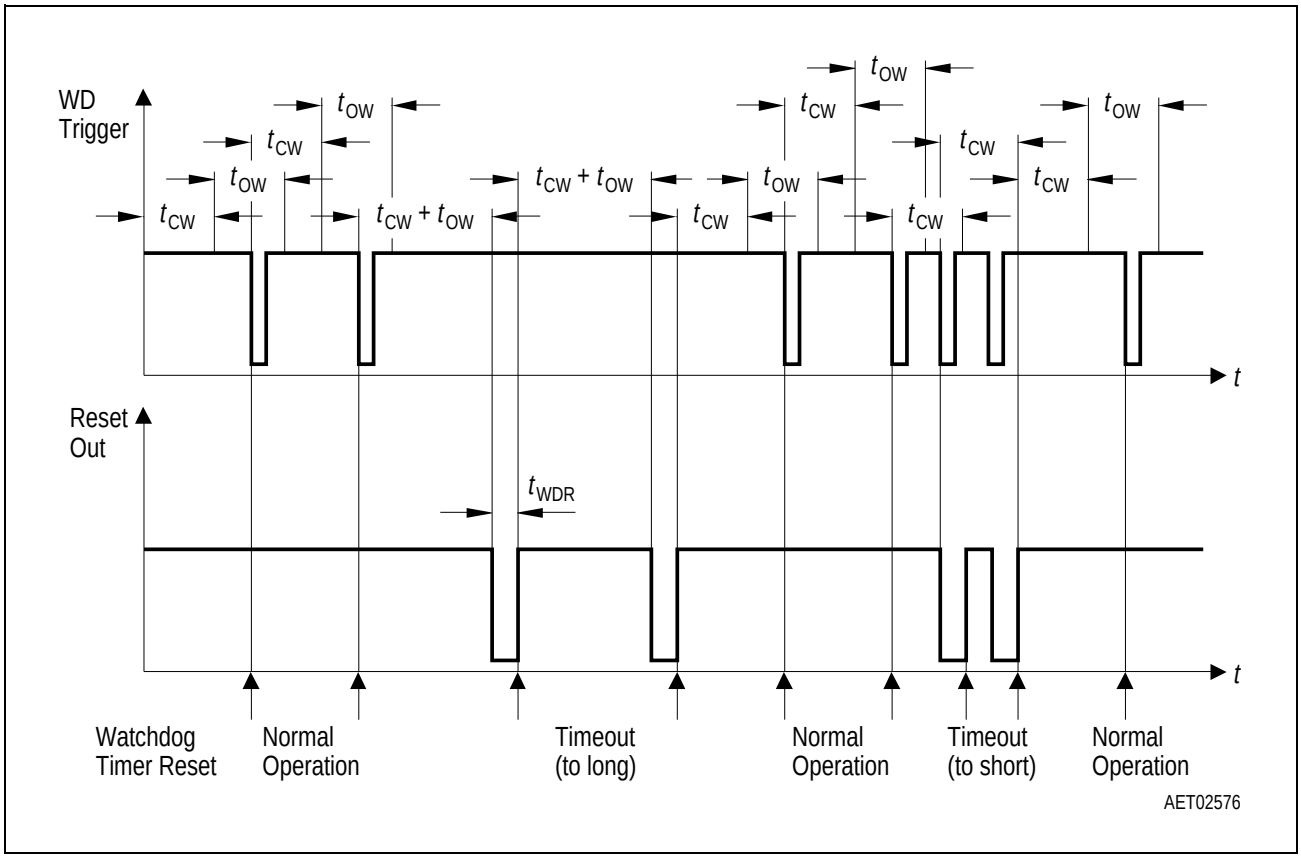


Figure 8
Watchdog Timing Diagram

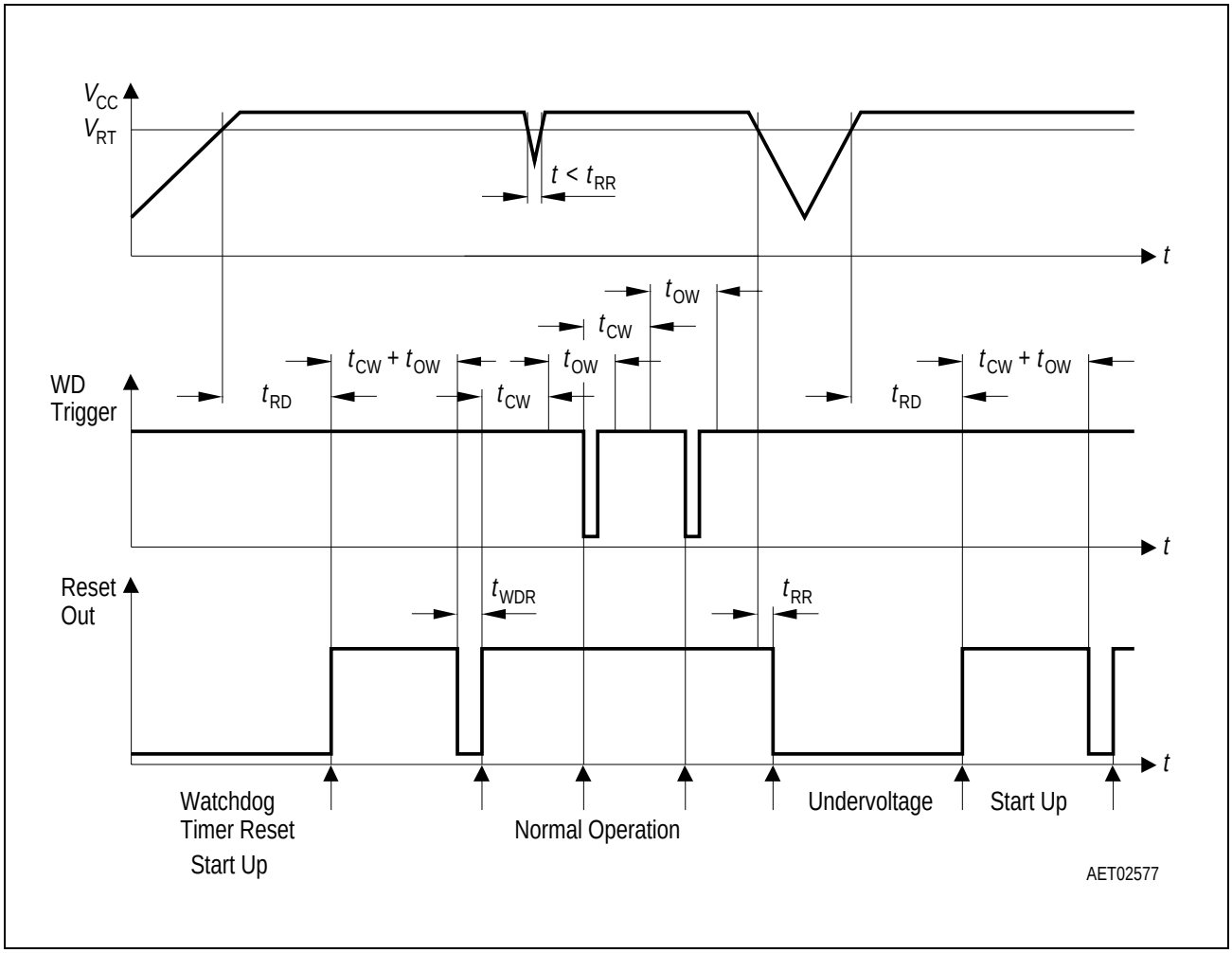


Figure 9
Reset Timing Diagram

Application

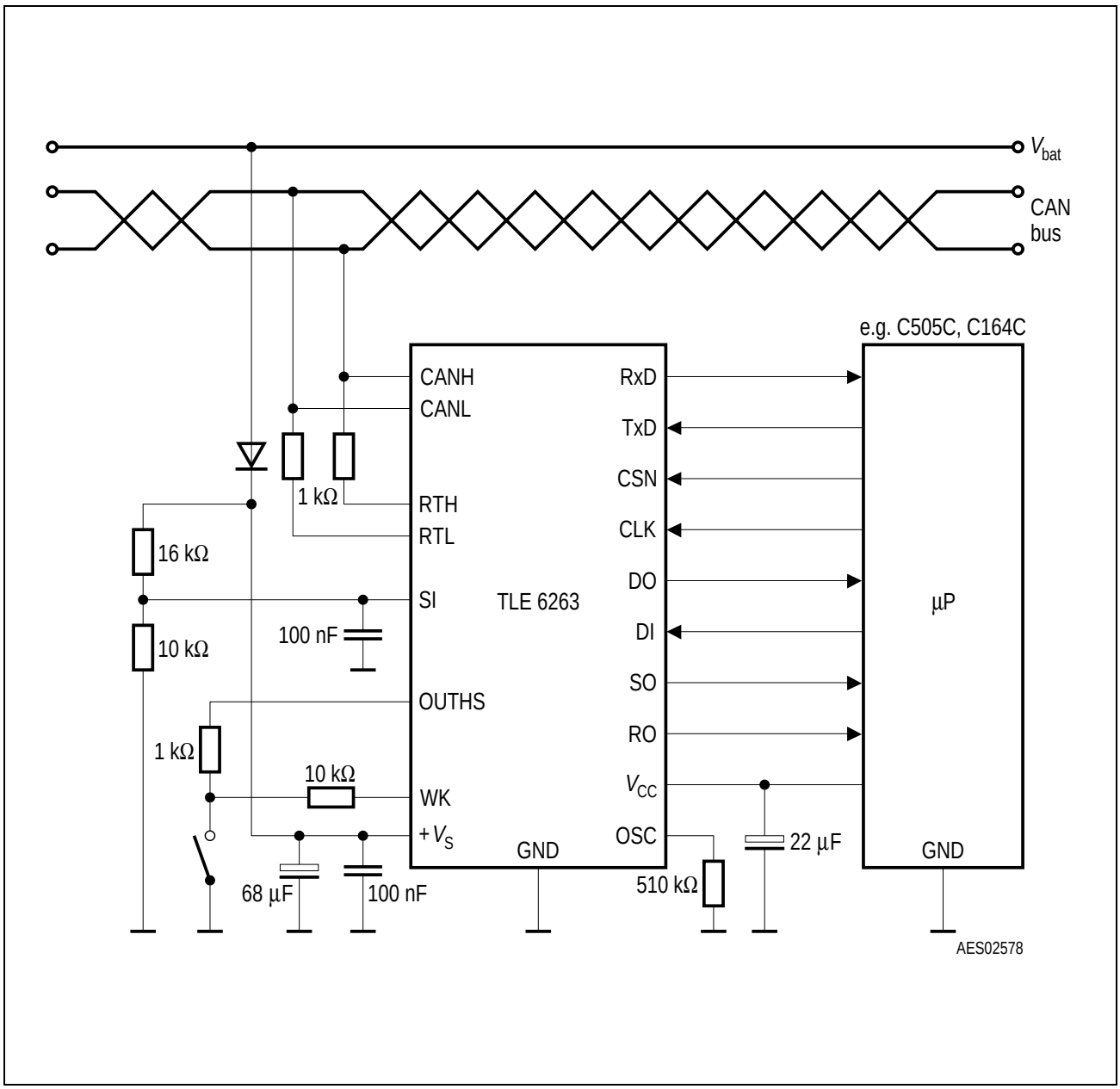
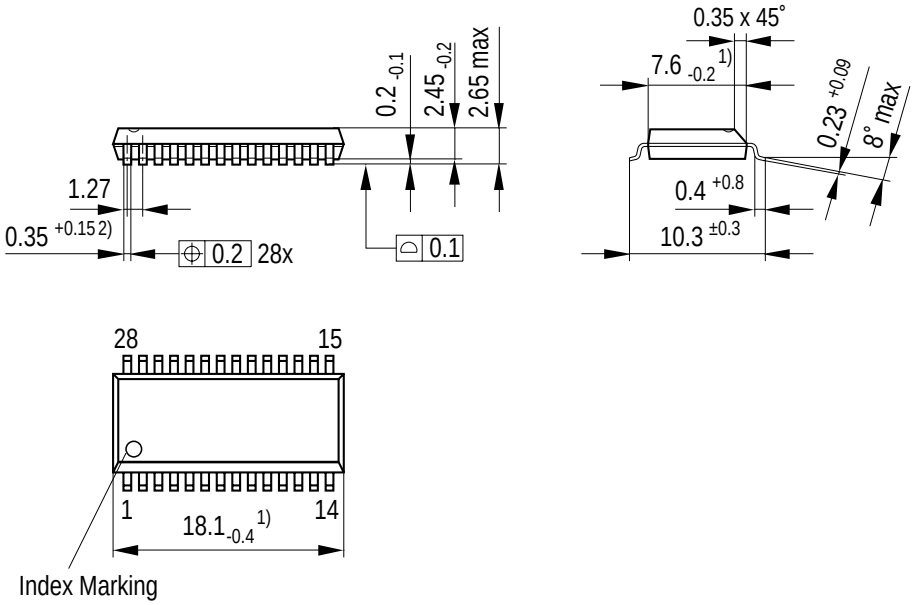


Figure 10
Application Circuit

Package Outlines

P-DSO-28-6
(Plastic Dual Small Outline)



1) Does not include plastic or metal protrusions of 0.15 max rer side
2) Does not include dambar protrusion of 0.05 max per side

GPS05123

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.
SMD = Surface Mounted Device

Dimensions in mm