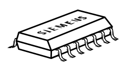
SIEMENS

Fault Tolerant Differential CAN Transceiver — TLE 6252 G

Target Data

Features



P-DSO-14-2

- Data transmission rate up to 125 kBaud
- Very low current consumption in stand-by and sleep mode
- Optimized EMI behavior due to limited and symmetric dynamic slopes of CANL and CANH signals
- Switches to single-wire mode during bus line failure events
- Supports one-wire transmission mode with ground offset voltages up to 1.5 V
- Preventation from bus occupation in case of CAN controller failure
- Fully-integrated receiver filters
- Short-circuit detection to battery and ground in 12 V powered systems
- Thermal protection
- Bus line error protection against transients in automotive environment

Type	Ordering Code	Package
▼ TLE 6252 G	Q67006-A9337	P-DSO-14-2 (SMD)

▼ New type

Functional Description

The CAN Transceiver works as the interface between the CAN protocol controller and the physical differential CAN bus. **Figure 1** shows the principle configuration of a CAN network.

The TLE 6252 is optimized for low-speed data transmission (up to 125 kBaud) in automotive and industrial applications.

In normal operation mode a differential signal is transmitted/received. When bus wiring failures are detected the device automatically switches in single-wire mode to maintain communication.

While no data is transferred, the power consumption can be minimized by multiple low power modes.

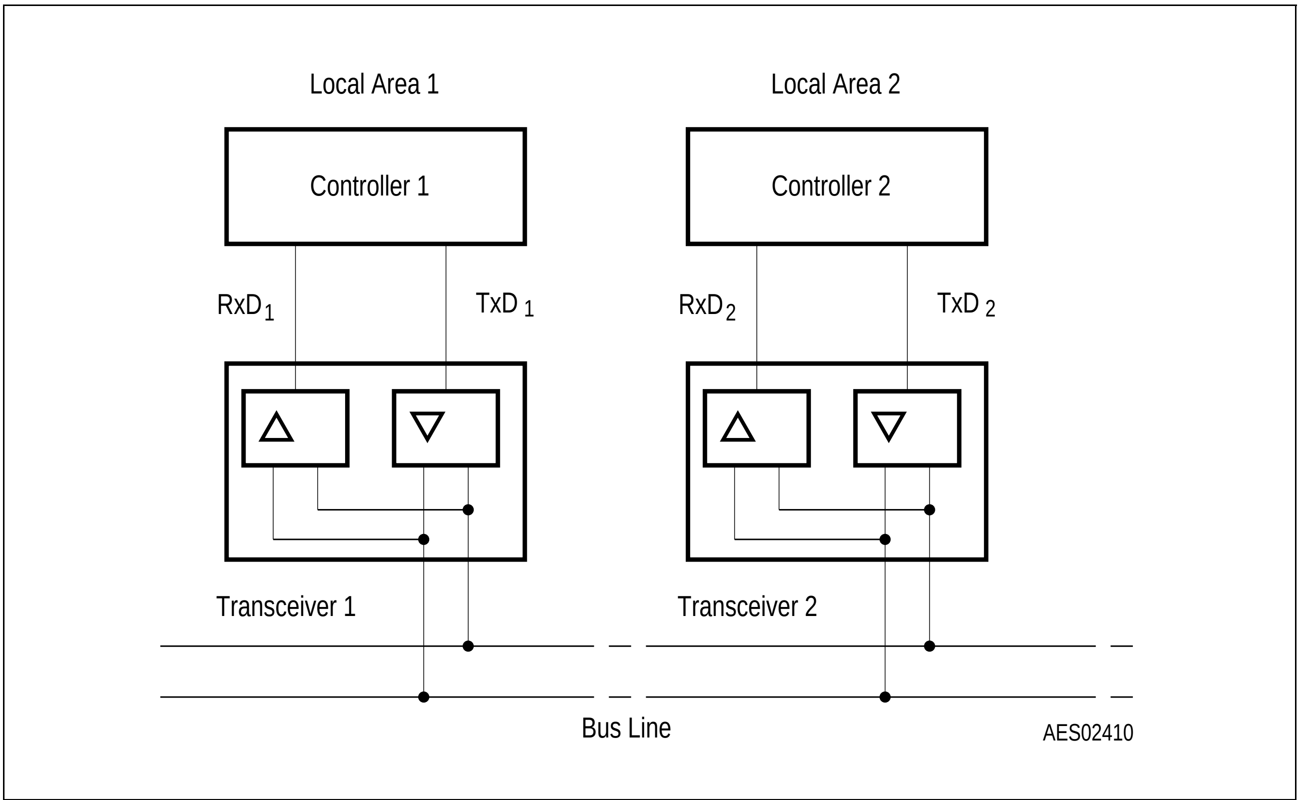


Figure 1 CAN Network Example

Pin Configuration

(top view)

P-DSO-14-2

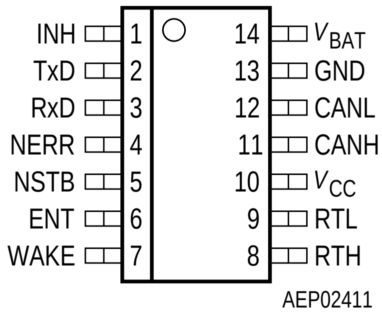


Figure 2

Table 1 Pin Definitions and Functions

Pin No.	Symbol	Function
1	INH	**Inhibit output;** For controlling an external 5 V regulator
2	TxD	**Transmit data input;** LOW: bus is dominant, HIGH: bus is recessive
3	RxD	**Receive data output;** LOW: bus is dominant
4	NERR	**Error flag output;** LOW: bus error
5	NSTB	**Not stand-by input;** Digital control signal for low power modes
6	ENT	**Enable transfer input;** Digital control signal for low power modes
7	WAKE	**Wake-up input;** If level of V_{WAKE} changes the device initials a wake-up from sleep mode by switching INH HIGH
8	RTH	**Termination resistor output;** For CANH line, controlled by internal failure management
9	RTL	**Termination resistor output;** For CANL line, controlled by internal failure and mode management
10	V_{CC}	**Supply voltage;** + 5 V
11	CANH	**Bus line H;** HIGH: dominant state, external pull-down for termination
12	CANL	**Bus line L;** LOW: dominant state, external pull-up for termination
13	GND	**Ground**
14	V_{BAT}	**Battery voltage;** + 12 V

Functional Block Diagram

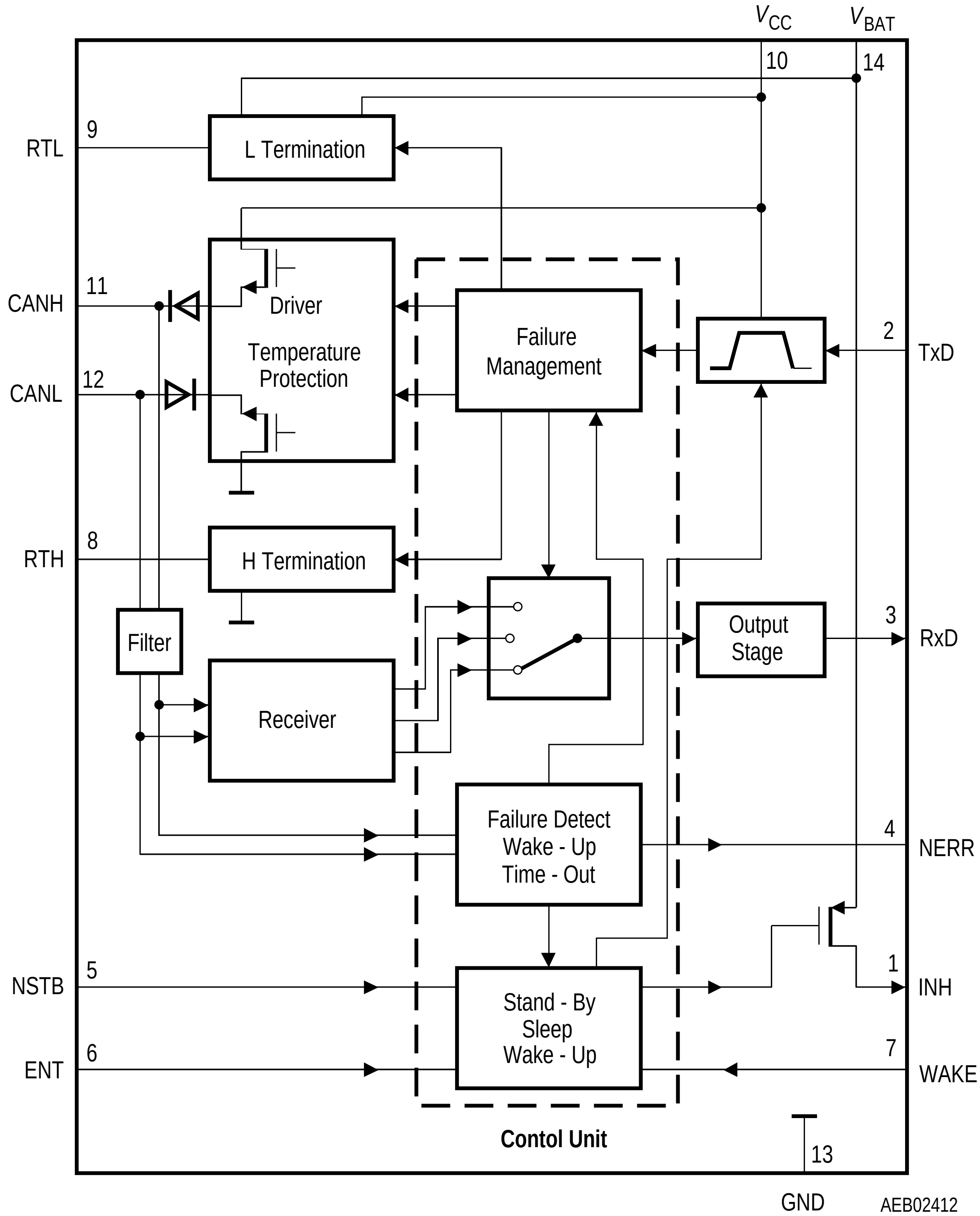


Figure 3 Block Diagram

General Operation Modes

In addition to the normal operation mode, the CAN transceiver offers three multiple low power operation modes to save power when there is no bus achieved: sleep mode, V_{Bat} stand-by mode and V_{CC} stand-by mode (see **Table 2** and **Figure 4**). Via the control inputs NSTB and ENT the operation modes are selected by the CAN controller.

In sleep operation mode the lowest power consumption is achieved. To deactivate the external voltage regulator for 5 V supply, the INH output is switched to high impedance in this mode. Also CANL is pulled-up to the battery voltage via the RTL output and the pull-up paths at input pins TxD and RxD are disabled from the internal supply.

On a wake-up request either by bus line activities or by the input WAKE, the transceiver automatically switches on the voltage regulator (5 V supply). The WAKE input reacts to rising and falling edges. As soon as V_{CC} is provided, the wake-up request can be read on both the NERR and RxD outputs, upon which the microcontroller can activate the normal operation mode by setting the control inputs NSTB and ENT high.

In V_{CC}-stand-by mode the wake up request is only reported at the RxD-output. The NERR output in this mode is set low when the supply voltage at pin V_{bat} was below the battery voltage threshold of 1 V.

When entering the normal mode the V_{bat}-Flag is reseted and the NERR becomes high again.

In addition the V_{bat}-Flag is set at a first connection of the device to battery voltage. This feature is usefull e.g. when changing the ECU and therefore a presetting routine of the microcontroller has to be started.

If either of the supply voltage drop below the specified limits, the transceiver automatically goes to a stand-by mode.

Table 2 Truth Table of the CAN Transceiver

<table>
<tr><th>NSTB</th><th>ENT</th><th>Mode</th><th>INH</th><th>NERR</th><th>RxD</th><th>RTL</th></tr>
<tr><td>0</td><td>0</td><td>V_{BAT} stand-by [1)]</td><td>V_{bat}</td><td colspan="2" rowspan="3">active LOW wake-up interrupt if V_{CC} is present</td><td>switched to V_{BAT}</td></tr>
<tr><td>0</td><td>0</td><td>sleep mode [2)]</td><td>floating</td><td>switched to V_{BAT}</td></tr>
<tr><td>0</td><td>1</td><td>go to sleep command</td><td>floating</td><td>switched to V_{BAT}</td></tr>
<tr><td>1</td><td>0</td><td>V_{CC} stand-by [3)]</td><td>V_{bat}</td><td>active LOW V_{BAT} power-on flag</td><td>active LOW wake-up interrupt</td><td>switched to V_{CC}</td></tr>
<tr><td>1</td><td>1</td><td>normal mode</td><td>V_{bat}</td><td>active LOW error flag</td><td>HIGH = receive;
LOW = dominant receive data</td><td>switched to V_{CC}</td></tr>
</table>

1) Wake-up interrupts are released when entering normal operation mode.

2) If go to sleep command was used before. ENT may turn LOW as V_{CC} drops, without affecting internal functions.

3) V_{BAT} power-on flag will be reseted when entering normal operation mode.

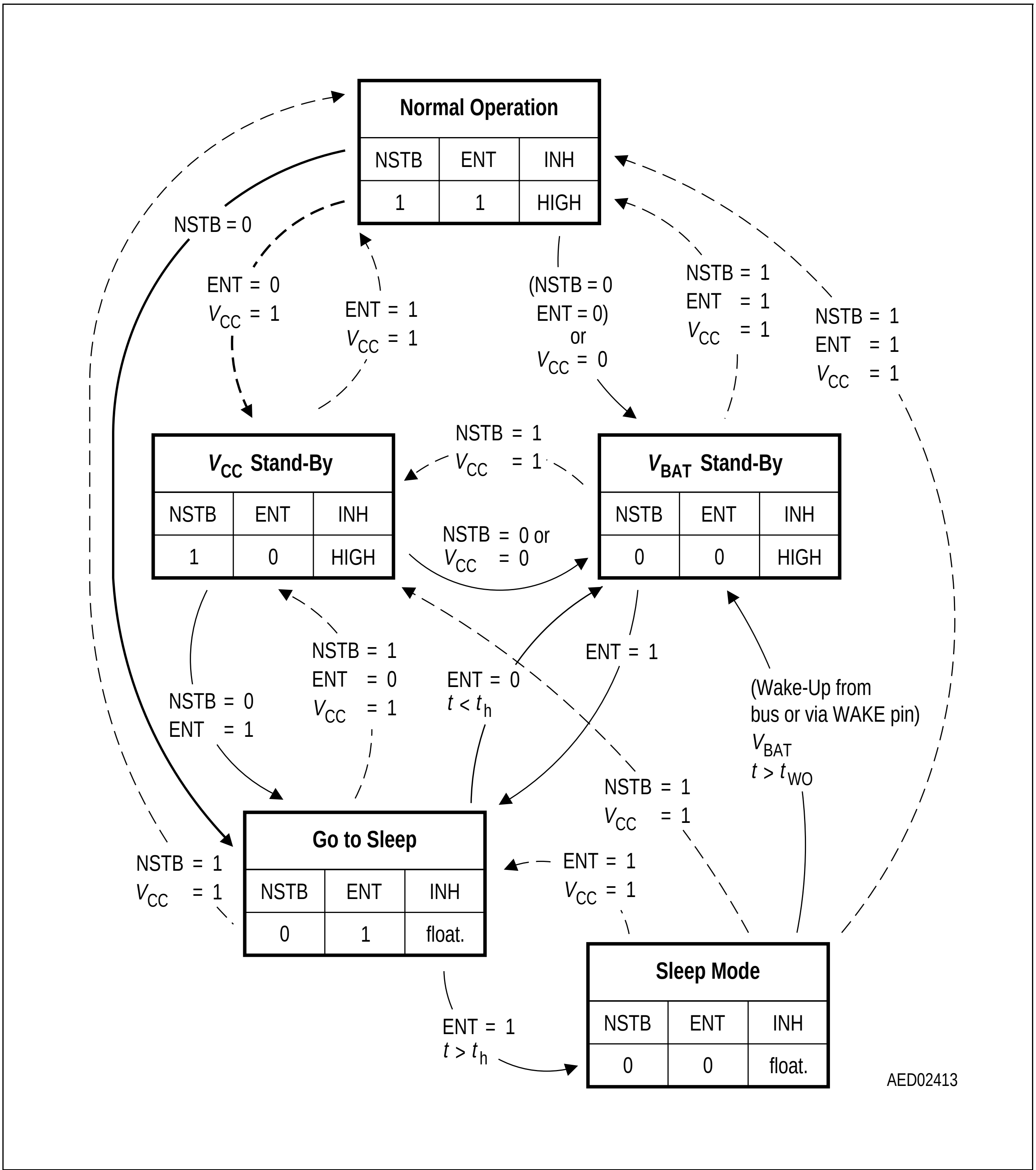


Figure 4 State Diagram

The transceiver will stay in a present operating mode until a suitable condition disposes a state change. If not otherwise defined all conditions are AND-combined. The signals V_{CC} and V_{BAT} show if the supply is available (e.g. $V_{CC} = 1$: V_{CC} voltage is present). If at minimum one supply voltage is switched on, the start-up procedure begins (not figured). After a delay time the device changes to normal operating or stand-by mode.

Bus Failure Management

The TLE 6252 detects the bus failures as described in the following (**Table 3**, failures listed according to ISO 11519-2) and automatically switches to a dedicated CANH or CANL single wire mode to maintain data transmission if necessary. Therefore, it is equipped with one differential receiver and 4 single ended comparators, two for each bus line. To avoid false triggering by external RF influences the single wire modes are activated after a certain delay time. As soon as the bus failure disappears the transceiver switches back to differential mode after another time delay. Bus failures are indicated in the normal operation mode by setting the NERR output to LOW.

To reduce EMI the dynamic slopes of the CANL and CANH signals are both limited and symmetric. This allows the use of an unshielded twisted or parallel pair of wires for the bus. During single-wire transmission the EMI performance of the system is degraded from the differential mode.

The differential receiver threshold is set to – 2.8 V. This ensures correct reception in the normal operation mode as well as in the failure cases 1, 2 and 4 with a noise margin as high as possible. For these failures, further failure management is not necessary. Detection of the failure cases 1, 2 and 4 is only possible when the bus is dominant. Nevertheless, they are reported on the NERR output until transmission of the next CAN word on the bus begins.

When one of the bus failures 3, 5, 6, 6a and 7 is detected, the defective bus wire is disabled by switching off the affected bus termination and the respective output stage. A wake-up from sleep mode via the bus is possible either via a dominant CANH or CANL line. This ensures that a wake-up is possible even if one of the failures 1 to 7 occurs.

In case the transmission data input, TxD from the CAN controller is permanently dominant, both, the CANH and CANL transmitting stage, are deactivated after a delay time. This is necessary to prevent blocking the bus by a defective protocol unit. The transmit time out error is flagged on NERR.

Table 3 Specified Wiring Failure Cases on the Bus Line [1)] (according to ISO 11519-2)

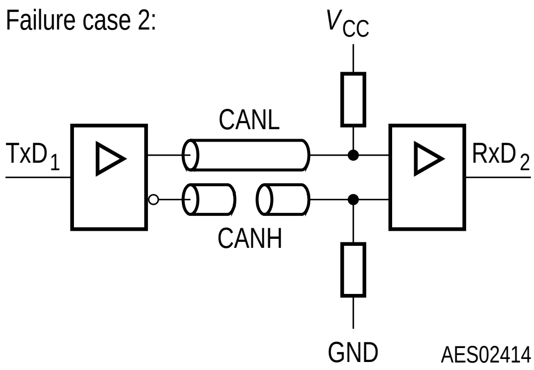
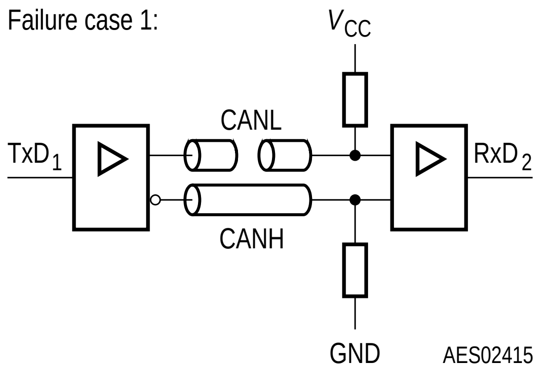
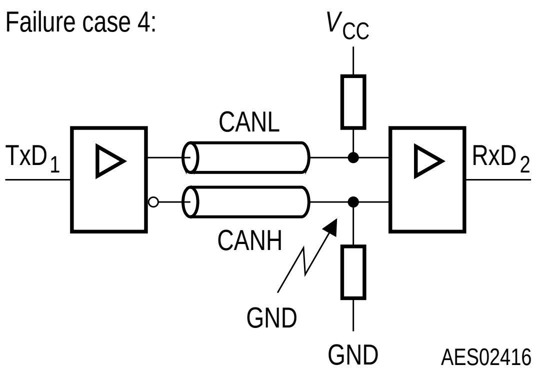
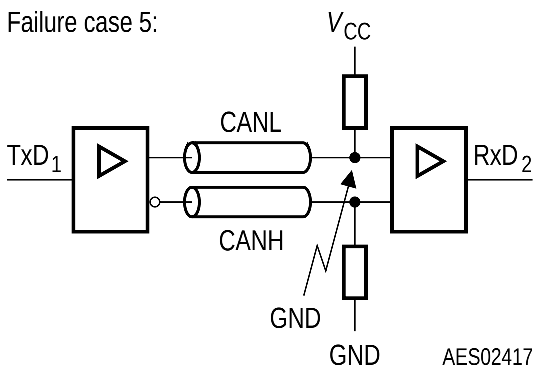
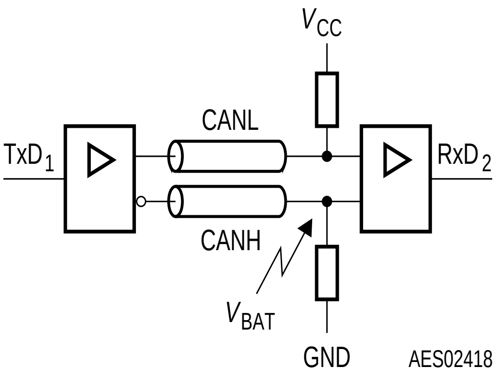
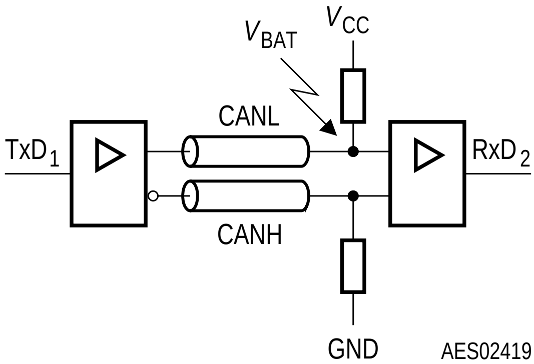
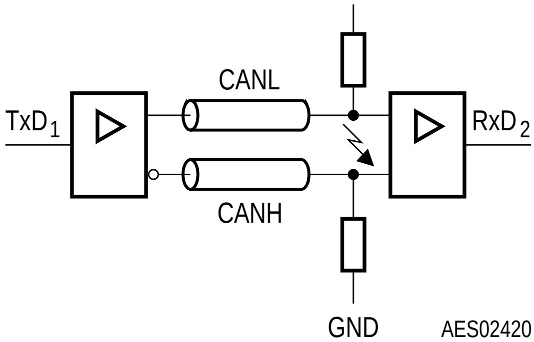
CANH	CANL
Wire Interrupted	
	
Wire Short-Circuited to GND	
	

Table 3 Specified Wiring Failure Cases on the Bus Line (cont'd) [1)]
(according to ISO 11519-2)

CANH	CANL
Wire Short-Circuited to Battery	
Failure case 6: V_{CANH} > 7.2 V Failure case 6a: 1.8 V < V_{CANH} < 7.2 V (no ISO failure) 	Failure case 3: V_{CANL} > 7.2 V Failure case 3a: 1.8 V < V_{CANL} < 7.2 V (no ISO failure) 
CANL Mutually Short-Circuited to CANH	
Failure case 7: 	

1) The images represent a communication between two participants of the network (see **Figure 1**). The controller of the local area 1 transmits data ($T \times D_1$) to the receiver of the local area 2 ($R \times D_2$). When a single failure of cases 1 to 7 occurs, the error handling enables communication through appreciated reactions.

Circuit Protection

A current limiting circuit protects the CAN transceiver output stages from damage by short-circuit to positive and negative battery voltages.

The CANH and CANL pins are protected against electrical transients which may occur in the severe conditions of automotive environments.

The transmitter output stage generates the majority of the power dissipation. Therefore it is disabled if the junction temperature exceeds the maximum value. This effectively reduces power dissipation, and hence will lead to a lower chip temperature, while other parts of the IC can remain operating.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input voltage at V_{BAT}	V_{BAT}	– 0.3	40	V	–
Logic supply voltage V_{CC}	V_{CC}	– 0.3	6	V	–
Input voltage at TxD, RxD, NERR, NSTD and ENT	V_{IN}	– 0.3	V_{CC} + 0.3	V	–
Input voltage at CANH and CANL	V_{BUS}	– 10	27	V	–
Input voltage at CANH and CANL	V_{BUS}	– 40	40	V	1)
Transient voltage at CANH and CANL	V_{BUS}	– 150	100	V	2)
Input voltage at WAKE	V_{IN}	–	V_{BAT} + 0.3	V	–
Input current at WAKE	I_{IN}	– 15	–	mA	3)
Input voltage at INH, RTH and RTL	V_{IN}	– 0.3	V_{BAT} + 0.3	V	–
Termination resistances at RTL and RTH	$R_{RTL/H}$	500	16000	Ω	–
Junction temperature	T_j	– 40	150	°C	–
Storage temperature	T_{stg}	– 55	155	°C	–
Electrostatic discharge voltage at any pin	V_{esd}	– 4000	4000	V	4)

1) V_{CC} = 0 to 5.5 V; V_{BAT} > 0 V; t < 0.1 ms; load dump

2) See ISO 7637

3) Negative currents flowing out of the IC.

4) Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.

Note: Maximum ratings are absolute ratings; exceeding one of these values may cause irreversible damage to the integrated circuit.

Operating Range

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Logic input voltage	V_{CC}	4.75	5.25	V	–
Battery input voltage	V_{BAT}	6	27	V	–
Junction temperature	T_j	– 40	150	°C	–

Thermal Resistance

Junction ambient	R_{thja}	–	120	K/W	–

Static Characteristics

4.75 V ≤ V_{CC} ≤ 5.25 V; V_{NSTB} = V_{CC}; 6 V ≤ V_{BAT} ≤ 27 V; – 40 ≤ T_j ≤ + 125 °C (unless otherwise specified). All voltages are defined with respect to ground. Positive current flowing into the IC.

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Supplies V_{CC}, V_{BAT}						
Supply current	I_{CC}	–	3.5	10	mA	recessive; TxD = V_{CC}; normal operating mode
		–	6	20	mA	dominant; TxD = 0 V; no load; normal operating mode
Supply current (V_{CC} stand-by)	I_{CC} + I_{BAT}	–	120	500	µA	V_{CC} = 5 V; V_{BAT} = 12 V; T_A < 90 °C
Supply current (V_{BAT} stand-by)	I_{BAT} + I_{CC}	–	55	100	µA	
Supply current (sleep operation mode)	I_{BAT}	–	15	30	µA	V_{CC} = 0 V; V_{BAT} = 12 V; T_A < 90 °C
Battery voltage for setting power-on flag	V_{BAT}	–	–	1.0	V	V_{CC} stand-by mode
Battery voltage low time for setting power-on flag	$t_{pw(on)}$	–	200	–	µs	V_{CC} stand-by mode
Receiver Output R×D and Error Detection Output NERR						
HIGH level output voltage (pin NERR)	V_{OH}	V_{CC} – 0.9	–	V_{CC}	V	I_0 = – 100 µA
HIGH level output voltage (pin RxD)	V_{OH}	V_{CC} – 0.9	–	V_{CC}	V	I_0 = – 250 µA
LOW level output voltage	V_{OL}	0	–	0.9	V	I_0 = – 1.25 mA

Static Characteristics (cont'd)

4.75 V ≤ V_{CC} ≤ 5.25 V; V_{NSTB} = V_{CC}; 6 V ≤ V_{BAT} ≤ 27 V; – 40 ≤ T_j ≤ + 125 °C (unless otherwise specified). All voltages are defined with respect to ground. Positive current flowing into the IC.

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Transmission Input T×D, Not Stand-By NSTB and Enable Transfer ENT						
HIGH level input voltage threshold	V_{IH}	0.7 × V_{CC}	–	V_{CC} + 0.3	V	500 mV hysteresis
LOW level input voltage threshold	V_{IL}	– 0.3	–	0.3 × V_{CC}	V	500 mV hysteresis
HIGH level input current (pins NSTB and ENT)	I_{IH}	–	9	20	µA	V_i = 4 V
LOW level input current (pins NSTB and ENT)	I_{IL}	0	1	–	µA	V_i = 1 V
HIGH level input current (pin TxD)	I_{IH}	– 200	– 50	– 25	µA	V_i = 4 V
LOW level input current (pin TxD)	I_{IL}	– 800	– 200	– 100	µA	V_i = 1 V
Forced battery voltage stand-by mode (fail safe)	V_{CC}	2.75	–	4.5	V	–
Minimum hold time for Go-To-Sleep command	t_{hSLP}	4	22	38	µs	–
Wake-up Input WAKE						
Input current	I_{IL}	– 3	– 2	– 1	µA	–
Wake-up threshold voltage	$V_{WK(th)}$	2.0	3.0	4.0	V	V_{NSTB} = 0 V

Static Characteristics (cont'd)

4.75 V ≤ V_{CC} ≤ 5.25 V; V_{NSTB} = V_{CC}; 6 V ≤ V_{BAT} ≤ 27 V; – 40 ≤ T_j ≤ + 125 °C (unless otherwise specified). All voltages are defined with respect to ground. Positive current flowing into the IC.

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Inhibit Output INH						
HIGH level voltage drop $\Delta V_H = V_{BAT} - V_{INH}$	ΔV_H	–	0.5	0.8	V	I_{INH} = – 0.18 mA;
Leakage current	I_{LI}	– 5	–	5.0	µA	sleep operation mode; V_{INH} = 0 V
Bus Lines CANL, CANH						
Differential receiver recessive-to-dominant threshold voltage	$V_{dRxD(rd)}$	– 2.8	– 2.5	– 2.2	V	V_{CC} = 5.0 V
Differential receiver dominant-to-recessive threshold voltage	$V_{dRxD(dr)}$	– 3.17	– 2.87	– 2.58	V	V_{CC} = 5.0 V
CANH recessive output voltage	V_{CANHr}	0.1	0.2	0.3	V	TxD = V_{CC}; R_{RTH} < 4 kΩ
CANL recessive output voltage	V_{CANLr}	V_{CC} – 0.2	–	–	V	TxD = V_{CC}; R_{RTL} < 4 kΩ
CANH dominant output voltage	V_{CANHd}	V_{CC} – 1.4	–	V_{CC}	V	TxD = 0 V; normal mode; I_{CANH} = – 40 mA
CANL dominant output voltage	V_{CANLd}	–	1.1	1.4	V	TxD = 0 V; normal mode; I_{CANL} = 40 mA
CANH output current	I_{CANH}	– 130	– 90	– 50	mA	V_{CANH} = 0 V; TxD = 0 V
		–	0	–	µA	sleep operation mode; V_{CANH} = 12 V

Static Characteristics (cont'd)

4.75 V ≤ V_{CC} ≤ 5.25 V; V_{NSTB} = V_{CC}; 6 V ≤ V_{BAT} ≤ 27 V; – 40 ≤ T_j ≤ + 125 °C (unless otherwise specified). All voltages are defined with respect to ground. Positive current flowing into the IC.

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
CANL output current	I_{CANL}	– 50	90	130	mA	V_{CANL} = 5 V; TxD = 0 V
		–	0	–	µA	sleep operation mode; V_{CANL} = 0 V; V_{BAT} = 12 V
Voltage detection threshold for short-circuit to battery voltage on CANH and CANL	$V_{det(th)}$	6.5	7.3	8.0	V	normal operation mode
Voltage detection threshold for short-circuit to battery voltage on CANH	$V_{det(th)}$	V_{BAT} – 2.5	V_{BAT} – 2	V_{BAT} – 1	V	stand-by/ sleep operation mode
CANH wake-up voltage threshold	V_{WAKEH}	1.2	1.9	2.7	V	–
CANL wake-up voltage threshold	V_{WAKEL}	2.4	3.1	3.8	V	–
Wake-up voltage threshold difference	ΔV_{WAKE}	0.2	–	–	V	ΔV_{SLP} = V_{SLPL} – V_{SLPH}
CANH single-ended receiver threshold	V_{CANH}	1.5	1.9	2.3	V	failure cases 3, 5 and 7
CANL single-ended receiver threshold	V_{CANL}	2.8	3.1	3.8	V	failure case 6 and 6a
CANH leakage current	I_{CANHl}	–	0	5	µA	V_{CC} = 0 V, V_{bat} = 0 V, V_{CANL} = 13.5 V, R_{RTL} = 100 Ω, T_j < 85 °C

Static Characteristics (cont'd)

4.75 V ≤ V_{CC} ≤ 5.25 V; V_{NSTB} = V_{CC}; 6 V ≤ V_{BAT} ≤ 27 V; – 40 ≤ T_j ≤ + 125 °C (unless otherwise specified). All voltages are defined with respect to ground. Positive current flowing into the IC.

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
CANL leakage current	I_{CANLl}	–	0	5	µA	V_{CC} = 0 V, V_{bat} = 0 V, V_{CANH} = 5 V, R_{RTH} = 100 Ω, T_j < 85 °C

Termination Outputs RTL, RTH

RTL to V_{CC} switch-on resistance	R_{RTL}	–	43	95	Ω	I_o = – 10 mA; normal operating mode
RTL output voltage	V_{oRTL}	V_{CC} – 1.0	V_{CC} – 0.7	–	V	$\|I_o\|$ < 1 mA; V_{CC} stand-by mode
RTL to BAT switch series resistance	R_{oRTL}	10	16	35	kΩ	V_{BAT} stand-by or sleep operation mode
RTH to ground switch-on resistance	R_{RTH}	–	43	95	Ω	I_o = 10 mA; normal operating mode
RTH output voltage	V_{oRTH}	–	0.7	1.0	V	I_o = 1 mA; low power mode
RTH pull-down current	I_{RTHpd}	–	75	–	µA	normal operating mode, failure cases 6 and 6a
RTL pull-up current	I_{RTLpu}	–	– 75	–	µA	normal operating mode, failure cases 3, 3a, 5 and 7
RTH leakage current	I_{RTHl}	–	0	5	µA	V_{CC} = 0 V, V_{bat} = 0 V, V_{CANH} = 5 V, R_{RTH} = 100 Ω, T_j < 85 °C

Static Characteristics (cont'd)

4.75 V ≤ V_{CC} ≤ 5.25 V; V_{NSTB} = V_{CC}; 6 V ≤ V_{BAT} ≤ 27 V; – 40 ≤ T_j ≤ + 125 °C (unless otherwise specified). All voltages are defined with respect to ground. Positive current flowing into the IC.

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
RTL leakage current	I_{RTLI}	–	0	5	µA	V_{CC} = 0 V, V_{bat} = 0 V, V_{CANL} = 13.5 V, R_{RTL} = 100 Ω, T_j < 85 °C

Thermal Shutdown

Shutdown junction temperature	T_{jSH}	150	–	–	°C	–

Dynamic Characteristics

V_{CC} = 4.75 V to 5.25 V; V_{NSTB} = V_{CC}; V_{BAT} = 6 V to 27 V; T_A = – 40 to + 125 °C (unless otherwise specified). All voltages are defined with respect to ground. Positive current flows into the IC.

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
CANH and CANL bus output transition time recessive-to-dominant	t_{rd}	0.6	1.4	2.0	µs	10% to 90%; C_1 = 10 nF; C_2 = 0; R_1 = 100 Ω
CANH and CANL bus output transition time dominant-to-recessive	t_{dr}	0.7	1.0	1.3	µs	10% to 90%; C_1 = 1 nF; C_2 = 0; R_1 = 100 Ω
Minimum dominant time for wake-up on CANL or CANH	$t_{wu(min)}$	8	22	38	µs	stand-by modes V_{BAT} = 12 V
Minimum WAKE Low time for wake-up	$t_{WK(min)}$	20	36	60	µs	Low power modes V_{BAT} = 12 V
Failure cases 3 and 6 detection time	t_{fail}	30	55	80	µs	normal operating mode
Failure case 6a detection time		2	4.8	8	ms	normal operating mode
Failure cases 5, 6, 6a and 7 recovery time		30	55	80	µs	normal operating mode
Failure cases 3 recovery time		150	450	750	µs	normal operating mode
Failure cases 5 and 7 detection time		0.75	1.8	4.0	ms	normal operating mode
Failure cases 5, 6, 6a and 7 detection time		0.8	3.6	8.0	ms	stand-by modes; V_{BAT} = 12 V
Failure cases 5, 6, 6a and 7 recovery time		–	2	–	µs	stand-by modes; V_{BAT} = 12 V

Dynamic Characteristics (cont'd)

V_{CC} = 4.75 V to 5.25 V; V_{NSTB} = V_{CC}; V_{BAT} = 6 V to 27 V; T_A = – 40 to + 125 °C (unless otherwise specified). All voltages are defined with respect to ground. Positive current flows into the IC.

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Propagation delay TxD-to-RxD LOW (recessive to dominant)	$t_{PD(L)}$	–	0.8	1.5	µs	C_1 = 100 pF; C_2 = 0; R_1 = 100 Ω; no failures and bus failure cases 1, 2, 3a and 4
		–	0.8	1.5	µs	C_1 = C_2 = 3.3 nF; R_1 = 100 Ω; no bus failure and failure cases 1, 2, 3a and 4
		–	1.2	1.8	µs	C_1 100 pF; C_2 = 0; R_1 = 100 Ω; bus failure cases 3, 5, 6, 6a and 7
		–	1.2	1.8	µs	C_1 = C_2 = 3.3 nF; R_1 =100 Ω; bus failure cases 3, 5, 6, 6a and 7

Dynamic Characteristics (cont'd)

V_{CC} = 4.75 V to 5.25 V; V_{NSTB} = V_{CC}; V_{BAT} = 6 V to 27 V; T_A = – 40 to + 125 °C (unless otherwise specified). All voltages are defined with respect to ground. Positive current flows into the IC.

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Propagation delay TxD-to-RxD HIGH (dominanat to recessive)	$t_{PD(H)}$	–	1.5	2.0	µs	C_1 = 100 pF; C_2 = 0; R_1 =100 Ω; no failures and bus failure cases 1, 2, 3a and 4
		–	2.5	3.0	µs	C_1 = C_2 = 3.3 nF; R_1 = 100 Ω; no bus failure and failure cases 1, 2, 3a and 4
		–	1.0	1.5	µs	C_1 100 pF; C_2 = 0; R_1 = 100 Ω; bus failure cases 3, 5, 6, 6a and 7
		–	1.4	2.1	µs	C_1 = C_2 = 3.3 nF; R_1 = 100 Ω; bus failure cases 3, 5, 6, 6a and 7
Minimum hold time to go sleep command	$t_{h(min)}$	4	22	38	µs	–
Edge-count difference (falling edge) between CANH and CANL for failure cases 1, 2, 3a and 4 detection NERR becomes LOW	n_e	–	4	–	–	normal operating mode
Edge-count difference (rising edge) between CANH and CANL for failure cases 1, 2, 3a and 4 recovery		–	2	–	–	
TxD permanent dominant disable time	t_{TxD}	1	2.5	4	ms	normal mode

Test and Application

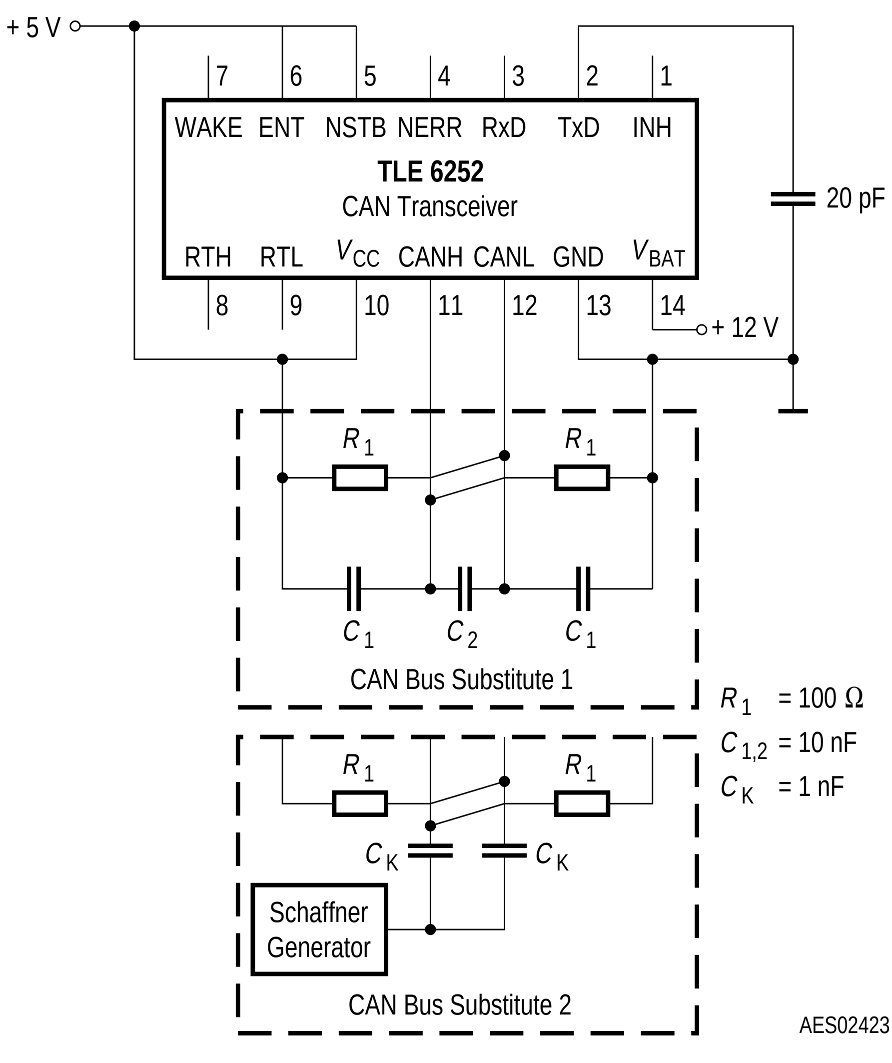


Figure 5 Test Circuits

For isolated testing the CAN Bus Substitute 1 is connected to the CAN Transceiver (see **Figure 5**). The capacitors $C_{1\text{-}3}$ simulate the cable. Allowed minimum values of the termination resistors R_{RTH} and R_{RTL} are 500 Ω. Electromagnetic interference on the bus lines is simulated by switching to CAN Bus Substitute 2. The waves of the applied transients will be in accordance with ISO 7637 part 1, test 1, test pulses 1, 2, 3a and 3b.

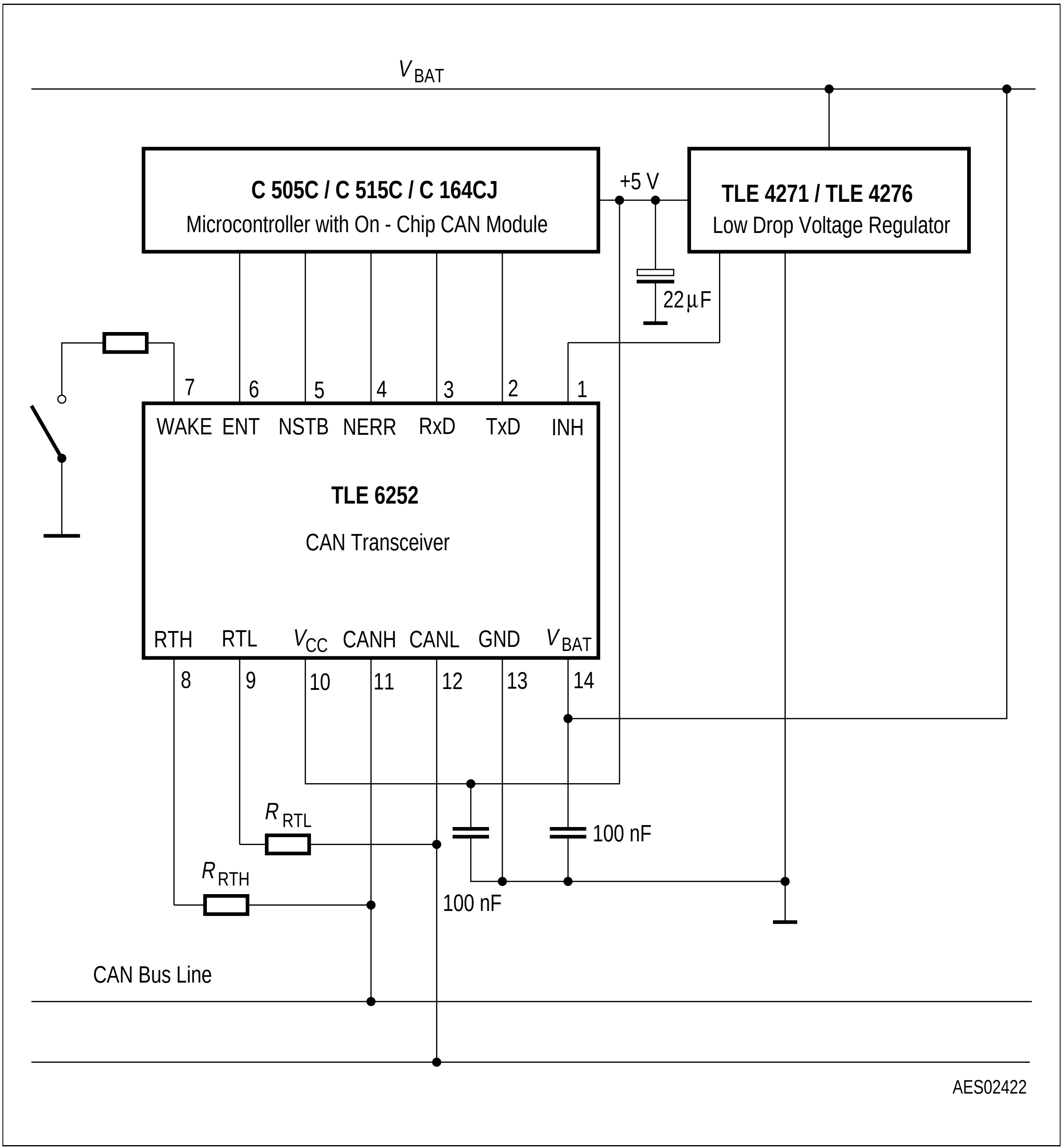
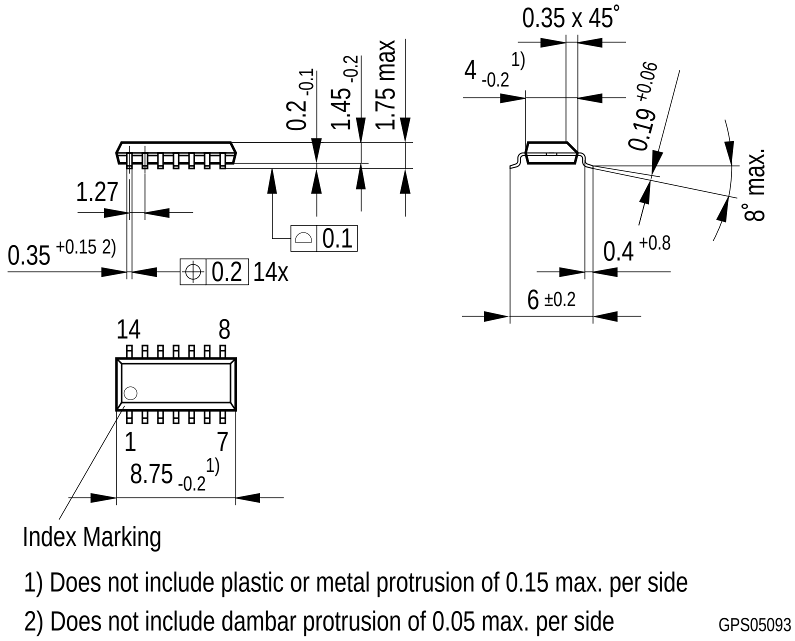


Figure 6 Application of the TLE 6252 G

Package Outlines

P-DSO-14-2
(Plastic Dual Small Outline)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm