SIEMENS

Triple-Halfbridge Driver with Serial Peripheral Interface I/O

TLE 6208-3 G

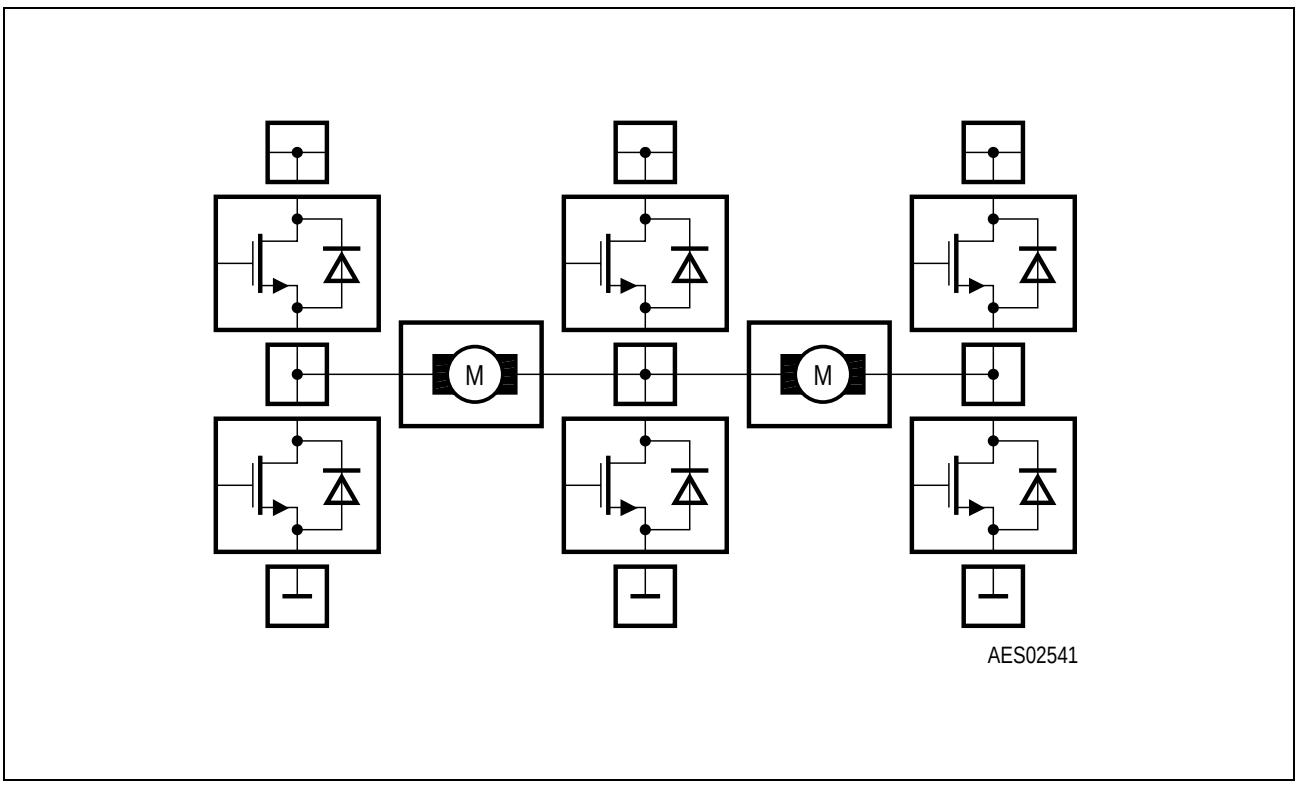

Figure 1

Features

- Three High-Side and three Low-Side-Drivers already connected as half-bridges
- Optimized for DC motor management applications
- 0.6 A continuous, 1.5 A peak current per switch
- $R_{DS\ ON}$; typ. 0.8 Ω, @ 25 °C per switch
- Output: short circuit protected and diagnosis
- Overtemperature-Protection with hysteresis and diagnosis
- Standard SPI-Interface/Daisy chain capable
- Interfaces directly to microcontroller using SPI Protocol
- SPI communication for control and fault reporting
- Serial operation is guaranteed to 1 MHz
- Full compatibility to the TLE 5208-6G with six highside and six lowside switches
- Very low current consumption (typ. 20 µA, @ 25 °C) in stand-by (inhibit) mode
- Over- and Undervoltage-Detection
- Over- and Undervoltage-Lockout
- CMOS/TTL compatible inputs with hysteresis
- Small enhanced power P-DSO-14 Package

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1 Circuit Description

1.1 Introduction

The **TLE 6208-3 G** was conceived, specified, designed and developed for automotive applications, but is well suited for other environments. The **TLE 6208-3 G** is a full protected triple halfbridge driver with a 16 bit serial peripheral interface I/O.

The device incorporates the Siemens power technology **SPT** which allows CMOS logic, bipolar/MOS analog circuitry, and DMOS power MOSFETs existing on the same monolithic circuitry. Many benefits are realized as a direct result of using this mixed technology. A simplified block diagram of the **TLE 6208-3 G** is shown in **Figure 2**.

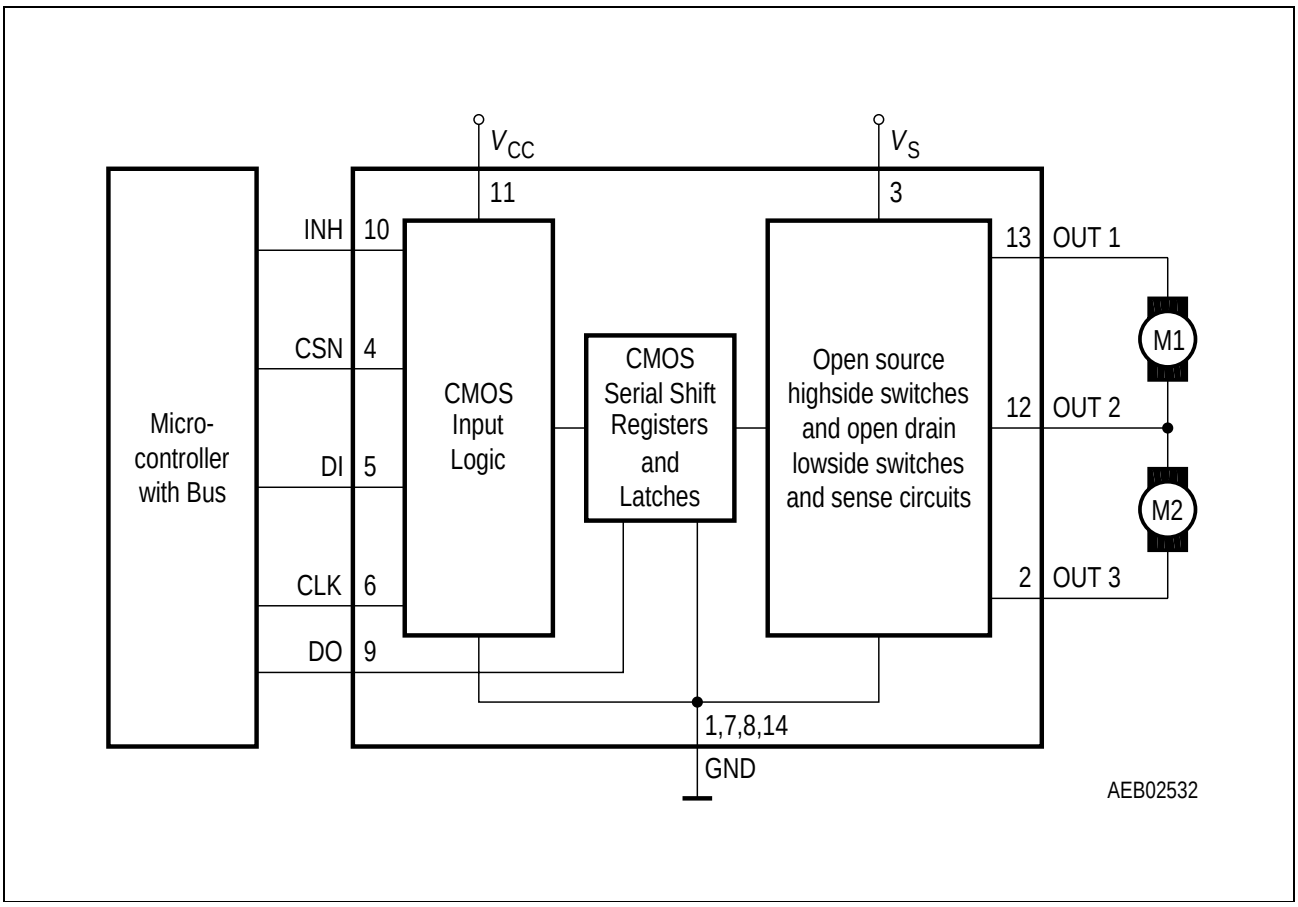

Figure 2 Simplified Application

In motion control up to two actuators (DC-motors) can be connected to the three halfbridge-outputs (cascade configuration) due to the three possible states of the halfbridges (high, low and tristate). This tristate functionality for motor halfbridges saves a complete halfbridge driver in the case of “multimotor applications”, since the motors can simply be connected in series. Operation modes forward (cw), reverse (ccw), brake and high impedance are controlled from a standard serial peripheral interface (SPI).

1.2 I/O-Interface

The **TLE 6208-3 G** directly interfaces to an microcontroller and operates at system clock serial frequencies in excess of 1.0 MHz using a synchronous peripheral interface (SPI) for control and diagnostic readout.

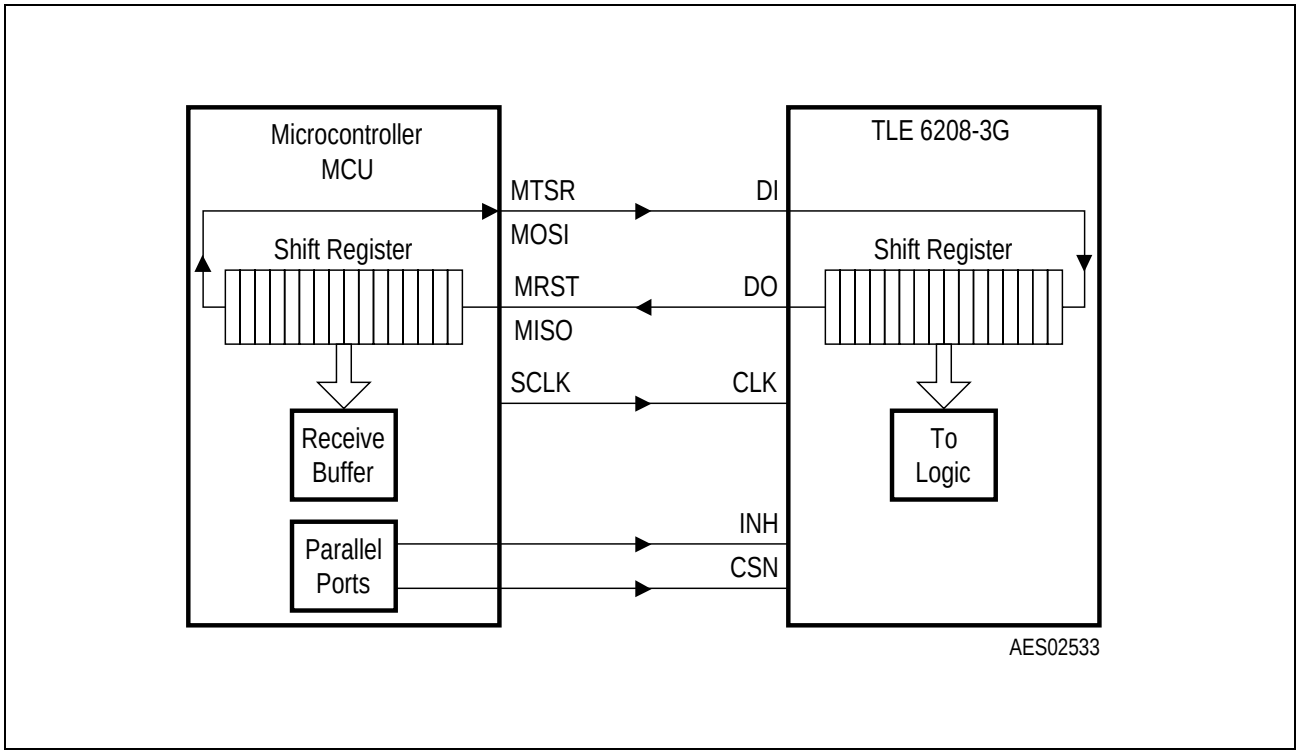

Figure 3 SPI Interface with Microcontroller

The SPI system is flexible enough to communicate directly with numerous standard peripherals. SPI reduces the number of pins necessary for input/output (I/O) on the **TLE 6208-3 G.** It also offers an easy means of expanding the I/O function using few MCU pins. The SPI system of communication consists of the MCU transmitting, and in return, receiving one databit of information per clock cycle. The MCU acts as Master and the **TLE 6208-3 G** acts as Slave. So Databits are simultaneously transmitted by one pin, Master Transmit Slave Receive (MTSR) respectively Master Out Slave In (MOSI). The data is received by another pin, Master Receive Slave Transmit (MRST) respectively Master In Slave Out (MISO).

Some features of SPI are:

- Full Duplex, that means a three-wire synchronous Data Transfer from and to the device at the same time
- Provides Write Collision Flag Protection on MCU
- Provides End of Message Interrupt Flag on MCU
- Three I/Os associated with SPI (MTSR, MRST, SCLK)

One main advantage of the **TLE 6208-3 G** is the serial port which when coupled to an MCU, receives “on/off” commands from the MCU and in return transmits the status of the

device's outputs. Many devices can be "daisy-chained" together to form a larger system as shown in **Figure 4**.

Note in this example that only one dedicated parallel port (aside from the required SPI) is needed for chip select to control a larger number of possible loads. Due to the compatibility the TLE 5208-6G can also be a member of the daisy-chain.

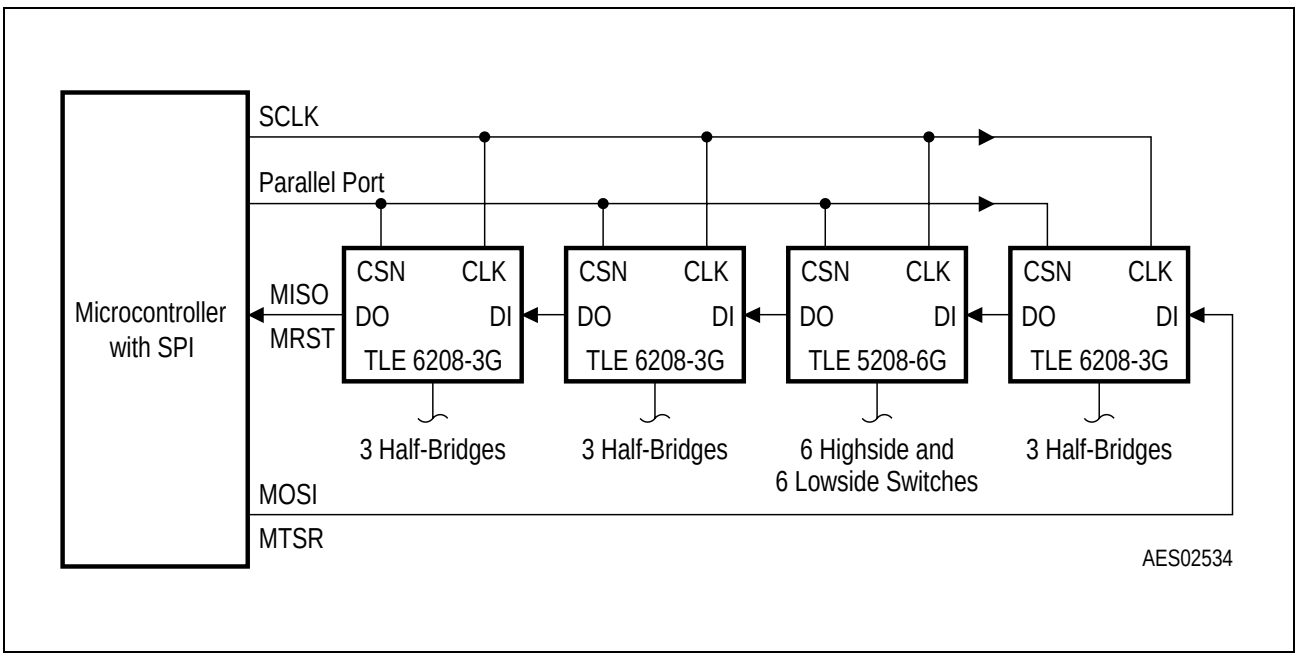

Figure 4 TLE6208-3G SPI System Daisy Chain

Multiple **TLE6208-3G** devices can also be controlled in a parallel input fashion using SPI. **Figure 5** shows the possibility to run 6 Halfbridges being controlled by only two dedicated parallel MCU ports used for chip select.

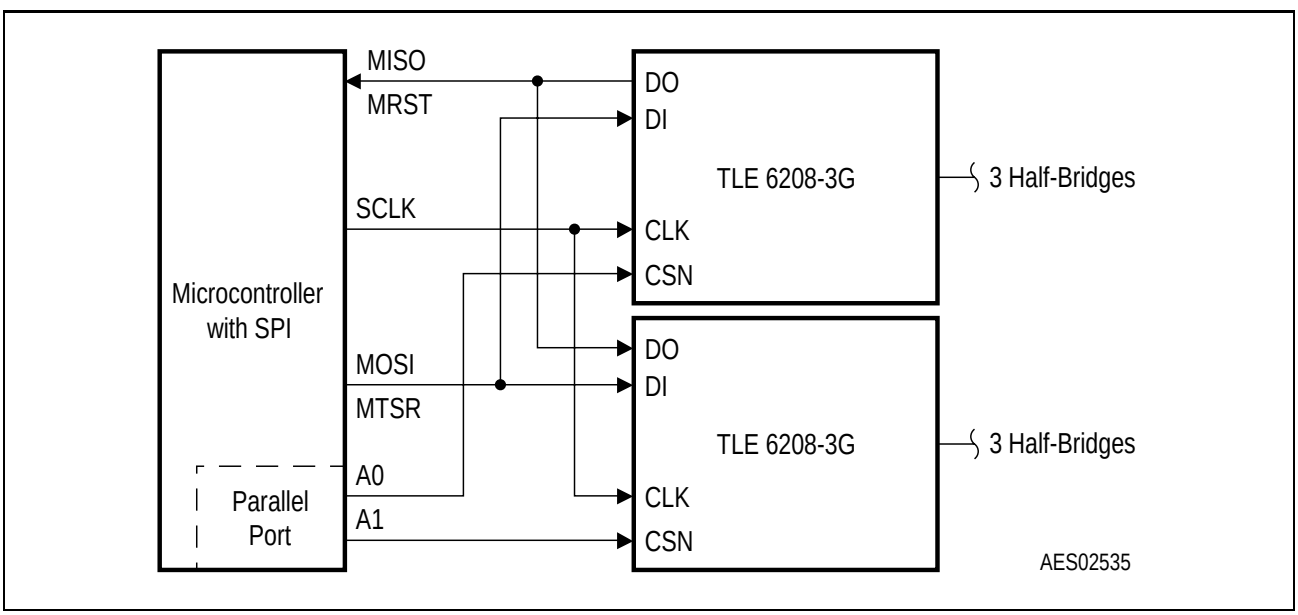

Figure 5 Parallel I/O SPI Control

The only drawbacks of SPI are that the MCU is required for efficient operational control and, in contrast to parallel input control, is slower but still sufficient at performing pulse width modulating (PWM) functions.

1.3 Power Stages

The IC is protected against short-circuits and overtemperatures. The SPI interface allows full diagnosis of overload and underload, overvoltage and undervoltage. In the event of serious overheating, the IC sends an overtemperature warning signal, so that the intelligent control system can intervene to reduce the dissipated power accordingly. This additional feature is designed for applications with increased safety requirements.

It is also possible to mask the overload current shut down threshold via software, so that power-on current spikes such as those occurring with motor loads can be managed.

The overvoltage shutdown can likewise be disabled via software. This means that the IC can also be used for industrial electronics with supply voltages up to 40 V.

The **TLE 6208-3 G** has a separate inhibit input for standby running if required (or as a “safety disable”), which switches the module into sleep mode with an extremely low current consumption of less than 10 µA.

The **TLE 6208-3 G** is specified over a temperature range of $-40\ °C < T_j < 150\ °C$ and $8\ V < V_S < 40\ V$ supply.

All of these functions are incorporated in a small **P-DSO-14** surface mount plastic package, thanks to the latest **Siemens Power Technology (SPT4)**. The special leadframe design “enhanced power” reduces thermal resistance to such an extent that intelligent distribution of dissipated power allows all loads to be handled simultaneously on the driver chip.

In summary: the **TLE 6208-3 G** provides a technically elegant and very cost effective solution for a wide range of automotive and industrial applications.

2 Functions of the TLE 6208-3 G

Figure 6 shows a block schematic diagram of the IC.

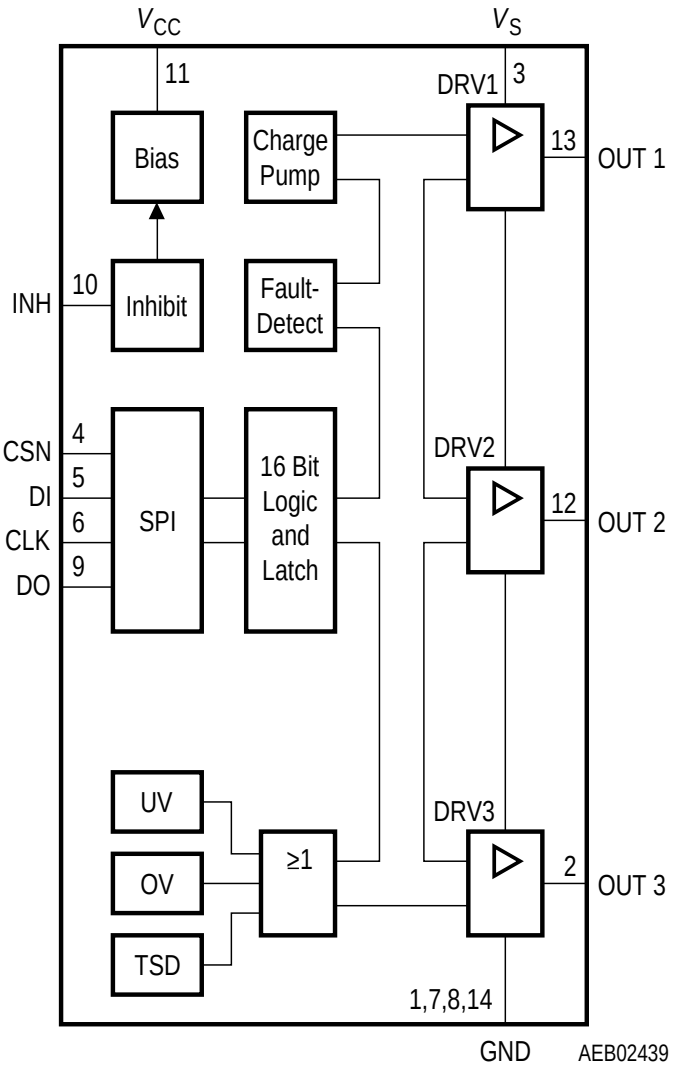

Figure 6 Block Schematic Diagram of the TLE 6208-3 G

There are three halfbridge drivers on the right-hand side. A highside driver and a lowside driver are combined to form a halfbridge driver in each case.

The drivers communicate via the internal data bus with the logic and the other control and monitoring functions: undervoltage (UV), overvoltage (OV), overtemperature (TSD), charge pump and fault detect.

Two pins are provided for supply to the IC: All power drivers are connected to the supply voltage V_S. This supply voltage is monitored by overvoltage and undervoltage comparators with hysteresis, so that the correct function can be checked in the application at any time.

The logic is supplied by the V_{CC} voltage, typ. with 5 V. The V_{CC} voltage uses an internally generated Power-on Reset (POR) to initialize the IC at power-on. The advantage of this system is that information stored in the logic remains intact in the event of short-term failures in the supply voltage V_S. The system can therefore continue to operate following V_S undervoltage, without having to be reprogrammed. The “undervoltage” information is stored, and can be read out via the interface. The same logically applies for overvoltage. “Interference spikes” on V_S are therefore effectively suppressed.

The situation is different in the case of undervoltage on the V_{CC} connection pin. If this occurs, then the internally stored data is deleted, and the output levels are switched to high-impedance status (tristate). The IC is initialized by V_{CC} following restart (Power-on Reset = POR)

The 16-bit wide programming word or control word is read in via the DI data input, and this is synchronized with the clock input CLK. The status word appears synchronously at the DO data output.

The transmission cycle begins when the chip is selected with the CSN input (H to L). If the CSN input changes from L to H then the word which has been read in becomes the control word. The DO output switches to tristate status at this point, thereby releasing the DO bus circuit for other uses.

The INH inhibit input can be used to switch the IC in stand-by mode. This reduces the current consumption to just a few µA, and results in the loss of any data stored. The output levels are switched to tristate status. The module is reinitialized with the internally generated POR (Power-on Reset) at restart.

This feature allows the use of this module in battery-operated applications (vehicle body control applications).

Figure 7 shows an overview of the chip layout.

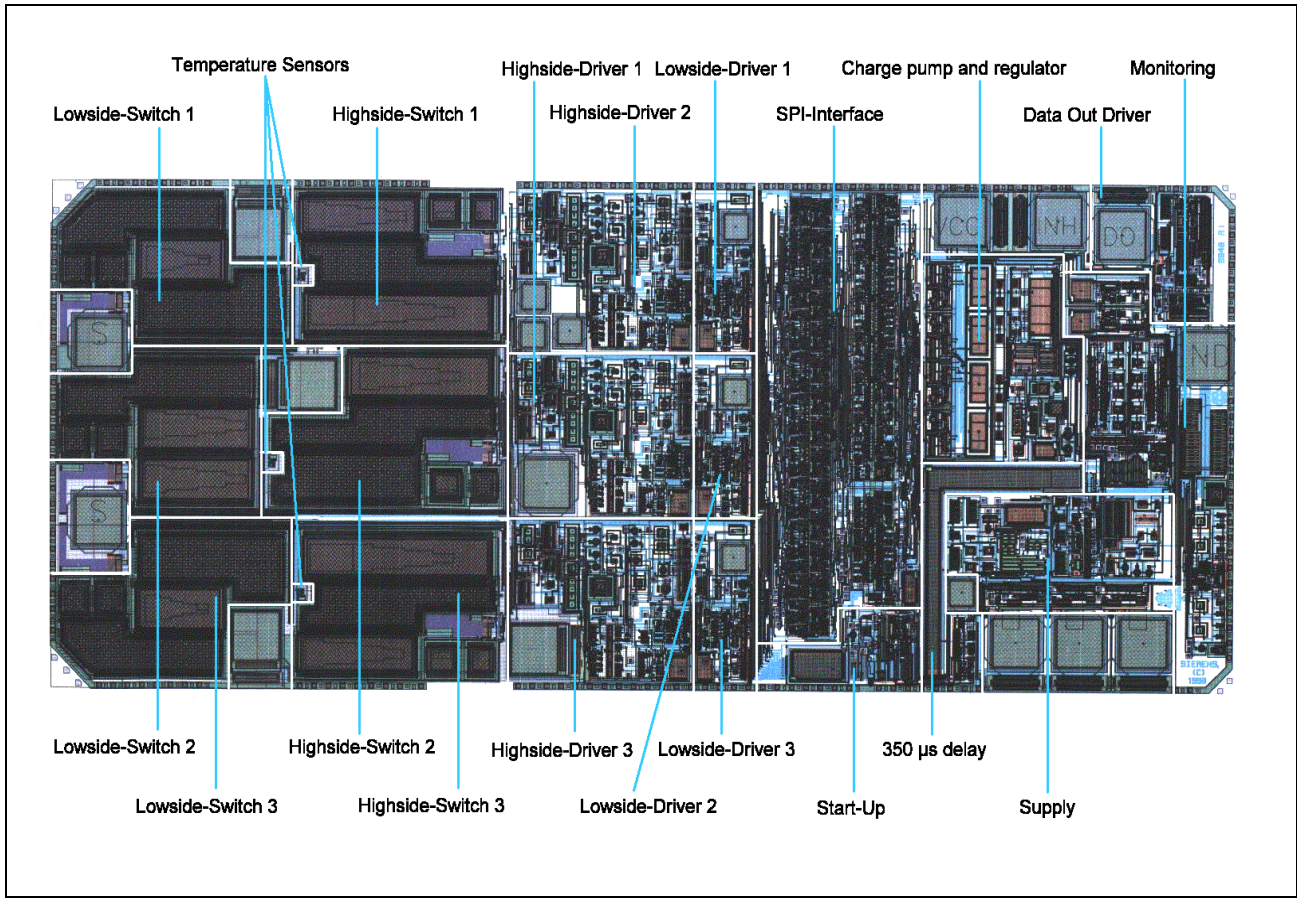

Figure 7 The TLE 6208-3 G Chip

The chip layout is explained from left to right. There are three lowside power switches on the left-hand side followed by the three highside switches. Three temperature sensors are located in the output stages to detect the overtemperature. The drivers for the highside and the lowside switches are followed by the shift register of the SPI interface and the Start-Up circuitry. The analog circuitries for the 350 µs delay, internal supply, charge pump and regulator, and monitoring which are sensitive to temperature gradients (e.g. the bandgap reference) are located at the right side of the chip, i.e. the farthest possible from the power stages.

3 Output Driver Levels

Every driver block from DRV 1 to 3 contains a low-side driver and a high-side driver. The outputs are internally connected to form a halfbridge.

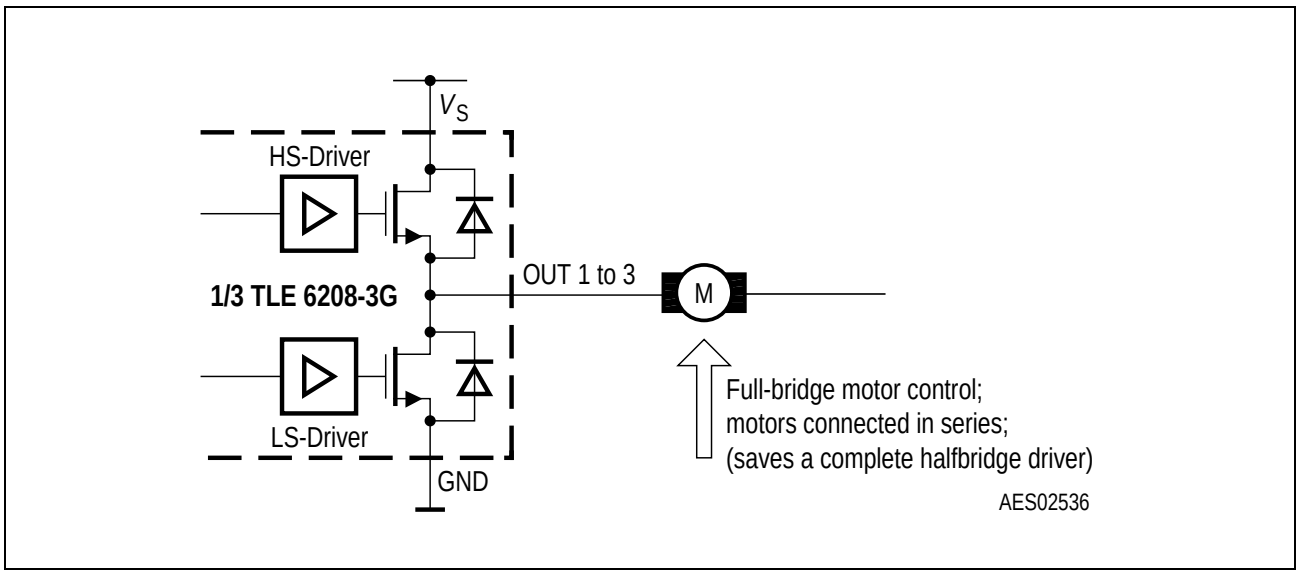

Figure 8 A Highside and a Lowside Switch Are Building the Halfbridge TLE 6208-3 G

When commutating inductive loads, the dissipated power peak can be significantly reduced by activating the transistor located parallel to the internal freewheeling diode. A special, integrated “timer” for power ON/OFF times ensures there is no crossover current at the halfbridge.

3.1 Low-side Driver

The following detailed block schematic diagrams of the output levels are provided for further clarification. The low-side driver connection is shown in **Figure 9**.

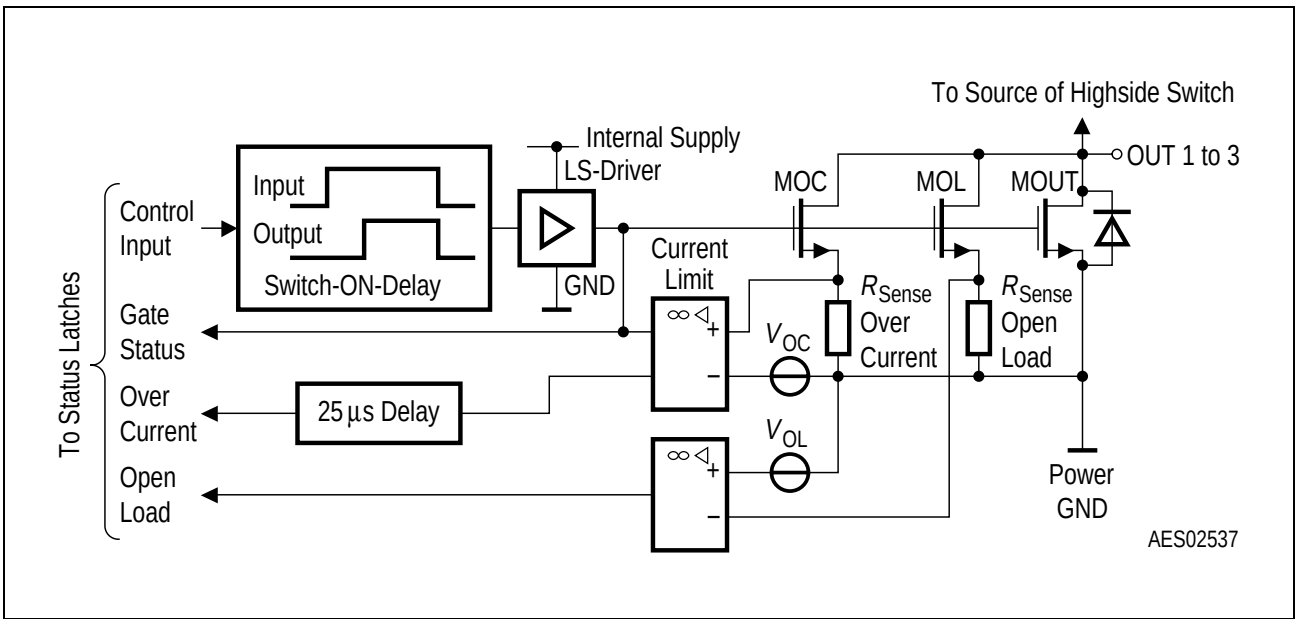

Figure 9 The Low-Side Driver Connection on the TLE 6208-3 G

The output transistor M_{OUT}, a power MOS (D-MOS) transistor, has an R_{DSON} of typ. 0.8 Ω at 25 °C. Its source connection is linked to the Power-GND connection. The drain is connected with the open source of the highside switch to build the output OUT1 to OUT3. Two sense devices (transistor, resistor and comparator) are used to detect overloads and underloads.

In the event of overcurrent, the gate voltage is also restricted. Following a specified dead time of typ. 25 µs, the logic cuts off the output transistor, and stores the information “Overcurrent at Switch X” in the status register.

It is possible to override the cut-off after 25 µs by resetting the overcurrent ON/OFF bits. However, the current continues to be restricted. This function allows the power-on of e.g. lights, motors, and heavy capacitive loads, which have high inrush currents and relatively short conducting periods.

Furthermore, delayed power-on allows the low-side drivers to be adapted to the switching times of the HS switch. For the halfbridge operation, this ensures that the HS switch is turned off before the LS switch starts to conduct (suppression of crossover current).

In order to ensure reliable underload detection in the case of commutating, inductive loads, an identical underload dead time has been integrated for all channels (including the high-side switches). The timer for this dead time (typ. 350 µs is started with the positive edge of the CSN. Explanation: All commutation processes start with this edge (e.g. to drive a motor in reverse mode), if inductance is present. Commutation processes

must be interpreted as underload by the underload detection system, since the current requires a finite period firstly to change the polarity and then to exceed the underload threshold. This dead time allows this “false information” to be suppressed, and its storage in the status register is prevented.

3.2 High-side Driver

Like the LS driver, the high-side driver circuit shown in **Figure 10** contains an overcurrent read-out, an undercurrent read-out and a current limit. Only the sense resistors are now in the drain branch. The comparator inputs therefore have supply voltage V_S as a fixed reference potential.

The signal processing which takes place in logic is similar to that of the LS switch. However, gate control is now supplied by the internal charge pump voltage V_{CP}, which is approx. 12 V higher than V_S.

The start-up configuration of the **TLE 6208-3 G** also ensures that no uncontrolled switching of the output levels occurs in the whole of the undervoltage range for V_S and V_{CC}. All output transistors are switched to tristate status. The functional range of the supply voltages is therefore specified up to 0 V.

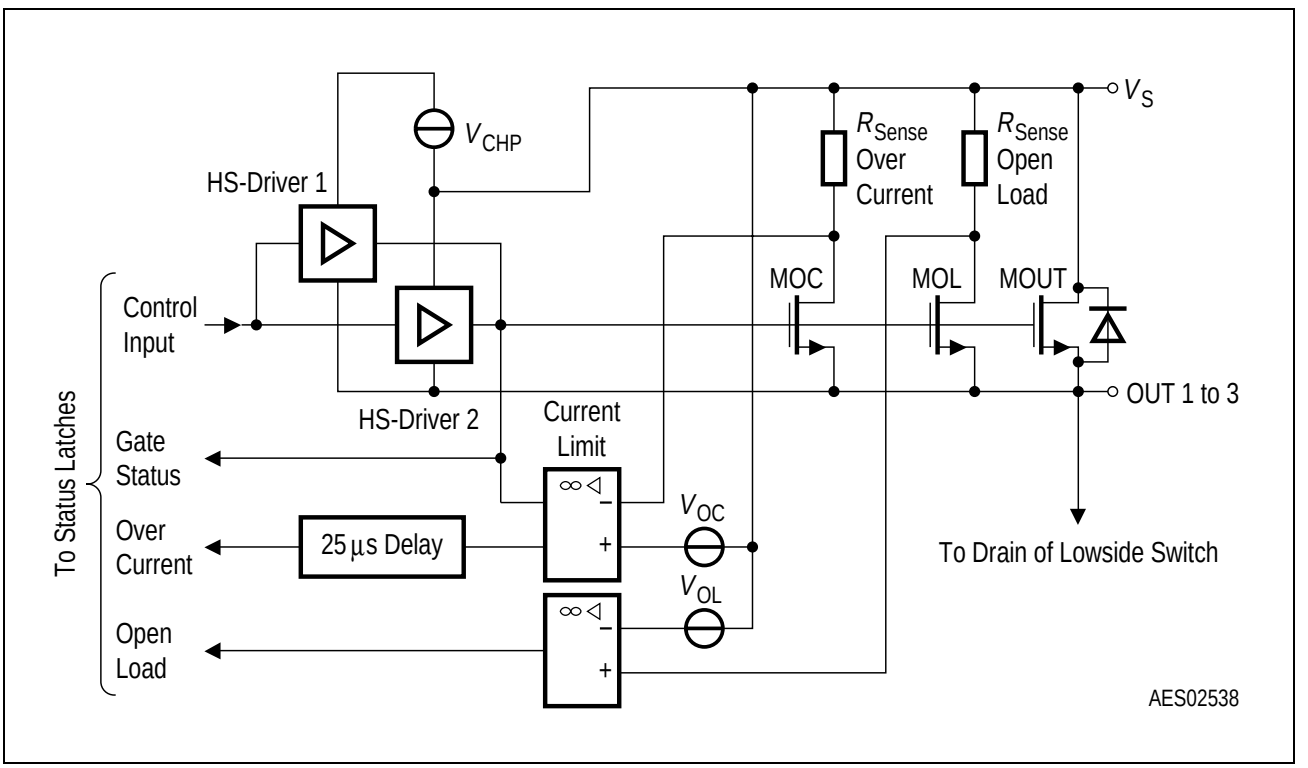

Figure 10 The High-Side Driver Circuit on the TLE 6208-3 G

The most important data for the output drivers is summarized again in **Table 1**.

Table 1 The Main Parameters of the Output Drive

Parameter	Symbol	Value for T_J = – 40 to 150 °C			Unit
		min.	typ. @25 °C	max.	
ON resistance	R_{DSONH}	–	0.8	2.0	Ω
	R_{DSONL}	–	0.75	2.0	Ω
Tristate leakage current	I_{QLH}	– 50	– 2	–	µA
	I_{QLL}	–	150	500	µA
Shut down current threshold	I_{SD}	1.0	1.3	2.0	A
Shut down dead time	t_{DSD}	10	28	40	µs
Current limit	I_{OCL}	–	2.4	5.0	A
Open circuit/Underload detection current threshold	I_{OCD}	15	30	60	mA
Open circuit/Underload dead time	t_{DOC}	200	370	500	µs

4 Programming the TLE 6208-3 G

The SPI interface is used to control the module or read out the status word. **Figure 11** shows a typical read/write cycle in the form of an oscillogram.

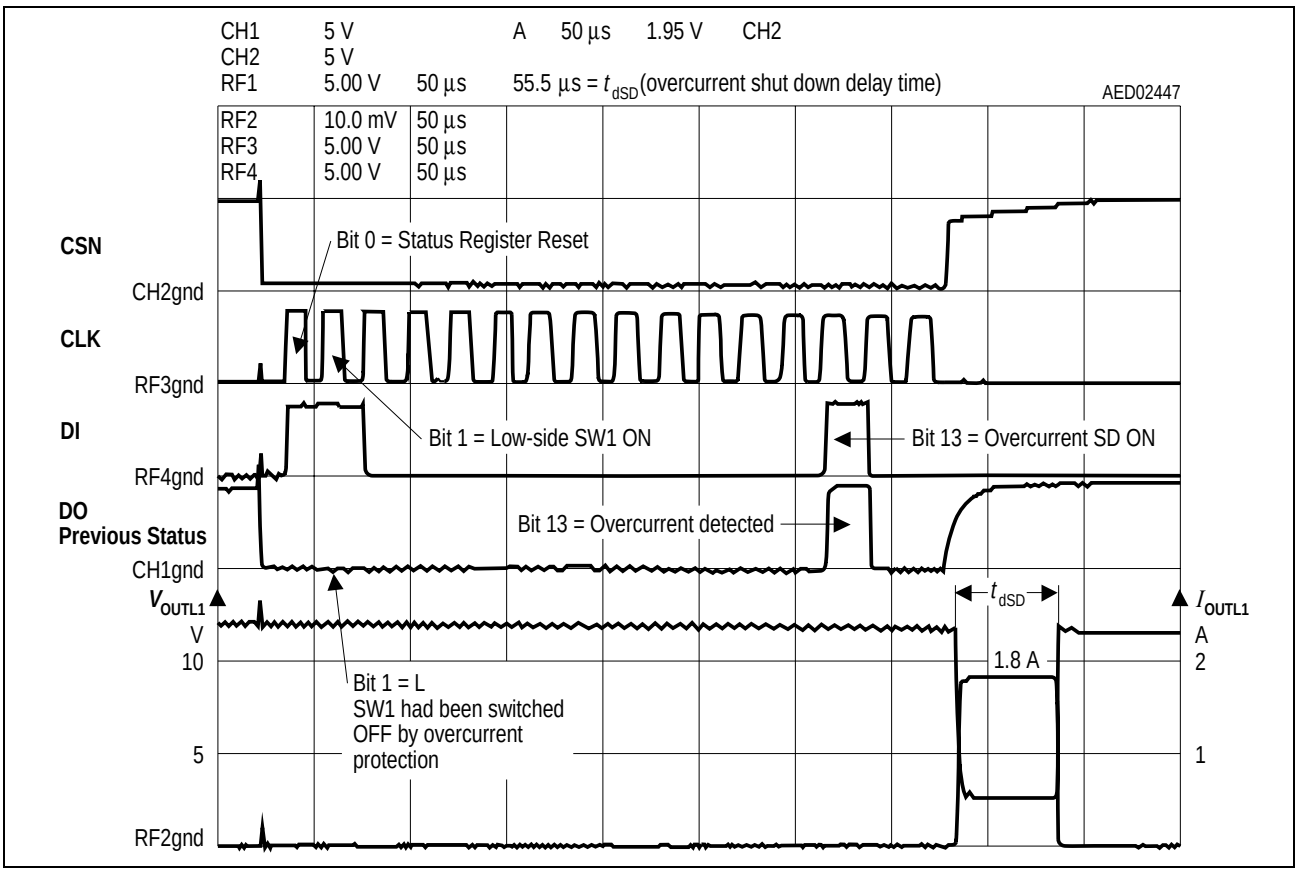

Figure 11 TLE 6208-3 G Read/Write Cycle

Read-in of the 16-bit long control word begins after the H-L edge of the CSN signal. Read-in of the control word at the DI input is synchronized with the CLK clock. The status word for the previous control word appears at the data output DO. When the CSN signal changes from L to H, the data which has been read in takes effect. The module is programmed. This is shown in **Figure 11** where the two lower lines represent the voltage and the current of LS Switch 1 (was programmed with Bit 1 = H at power-on; Bit 0 = H has also been read in). After approx. 25 µs the module cuts off the output because it is overloaded with more than 2 A, and Bit 13 = H (current cutoff active) was programmed at the same time. The exact timing is not detailed here. This data is specified in the TLE 6208-3 G Data Sheet.

A special software has been developed to provide simple control of an application board. This can be run under Windows® on any standard PC. The printer interface LPT1 or LPT2 can be used as an “SPI interface with inhibit”. Further details are provided below.

Table 2 and **Table 3** show the allocation of functions and switches to the control and diagnostics word.

4.1 Control Word

Table 2 The TLE 6208-3 G Control Word

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OVLO on/off	not used	Overcurrent SD on/off	not used	not used	not used	not used	not used	not used	HS-Switch 3	LS-Switch 3	HS-Switch 2	LS-Switch 2	HS-Switch 1	LS-Switch 1	Status Register Reset

H = ON
L = OFF

Details are as follows:

- **Bit 0: Status Register Reset**

  Bit 0 = L All data remains stored in the status register.

  Bit 0 = H The status register is reset after every programming cycle.

- **Bit 1 to 6: Driver Control**

  Bit 1 = L LS Switch 1 OFF

  Bit 1 = H LS Switch 1 ON

  and so on until

  Bit 6 = L HS Switch 3 OFF

  Bit 6 = H HS Switch 3 ON

- **Bit 7 to 12: Not Used**
- **Bit 13: Overcurrent Lockout**

  Bit 13 = L Overcurrent lockout after 25 µs is not active; the current is limited to typ. 3 A.

  Bit 13 = H Overcurrent lockout after 25 µs is active.

- **Bit 14: Not Used**
- **Bit 15: Overvoltage Lockout**

  Bit 15 = L Overvoltage lockout (OVLO) is not active.
  The module can be operated up to V_S = 40 V.

  Bit 15 = H Overvoltage lockout is active.
  All outputs are cut off if V_S = min. 34 V.

4.2 Status Word

Table 3 The TLE 6208-3 G Status Word

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Power Supply fail	Underload	Overload	not used	not used	not used	not used	not used	not used	Status HS-Switch 3	Status LS-Switch 3	Status HS-Switch 2	Status LS-Switch 2	Status HS-Switch 1	Status LS-Switch 1	Temp. Prewarning

High Means Switch is ON
Low Means Switch is OFF

The status word transmits the following information:

- **Bit 0: Overtemperature Prewarning**

  If the chip temperature rises above typ. T_j = 145 °C, then Bit 0 is set to H.

  The information is stored in the status register.

  At typ. T_j = 175 °C, all output levels are cut off (emergency off).

  The data remains stored in all registers.

  If the chip temperature drops below typ. T_j = 125 °C, then Bit 0 is set to L.

  The information in the status register is overwritten (all-clear).

- **Bits 1 to 6: ON/OFF Status Indicator of the Driver Levels**

  Status bits of the switches; assigned in the same way as the control word.

  This has the advantage that a simple EX-OR comparison of the control and status word after two read-ins is sufficient to check the transmission path and the application.

  The driver status is inserted in the status word. Analysis is performed by measuring the gate voltage at the output transistors.

  L means: Output level is deactivated (inhibited)

  H means: Output level is active (conducting)

- **Bit 7 to 12: Not Used**

- **Bit 13: Overload/Short-Circuit Indicator**

  “Overload” information is output here.
  H means that one or more of the 6 switches is or was overloaded. Status Bits 1 to 6 can be used to identify the switch concerned.

- **Bit 14: Underload/Broken Wire Indicator**

  “Underload” information is output here.

  H means that underload has been detected on one or more of the 6 switches.

  The exact identification of the switch concerned is likewise given by status bits 1 to 6.

- **Bit 15: Supply Voltage Fault**

  “Overvoltage or undervoltage at V_S” information is output here.

  H means that overvoltage or undervoltage has been or is still being detected at V_S. Overvoltage is also indicated if Bit 15 of the control word has been set to L (OVLO not active).

All information is stored, unless Bit 0 of the control word is set and a new control cycle has been initiated (see Bit 0 of the control word). In the same way, the status register is deleted by turning V_{CC} on or off, or by deactivating the IC via the inhibit input (INH = L).

5 Applications

The following section is concerned with possible applications of the IC.

The most important information is the pin configuration (pinning) and the package dimensions, and these are shown in **Figure 12** and **Figure 13**.

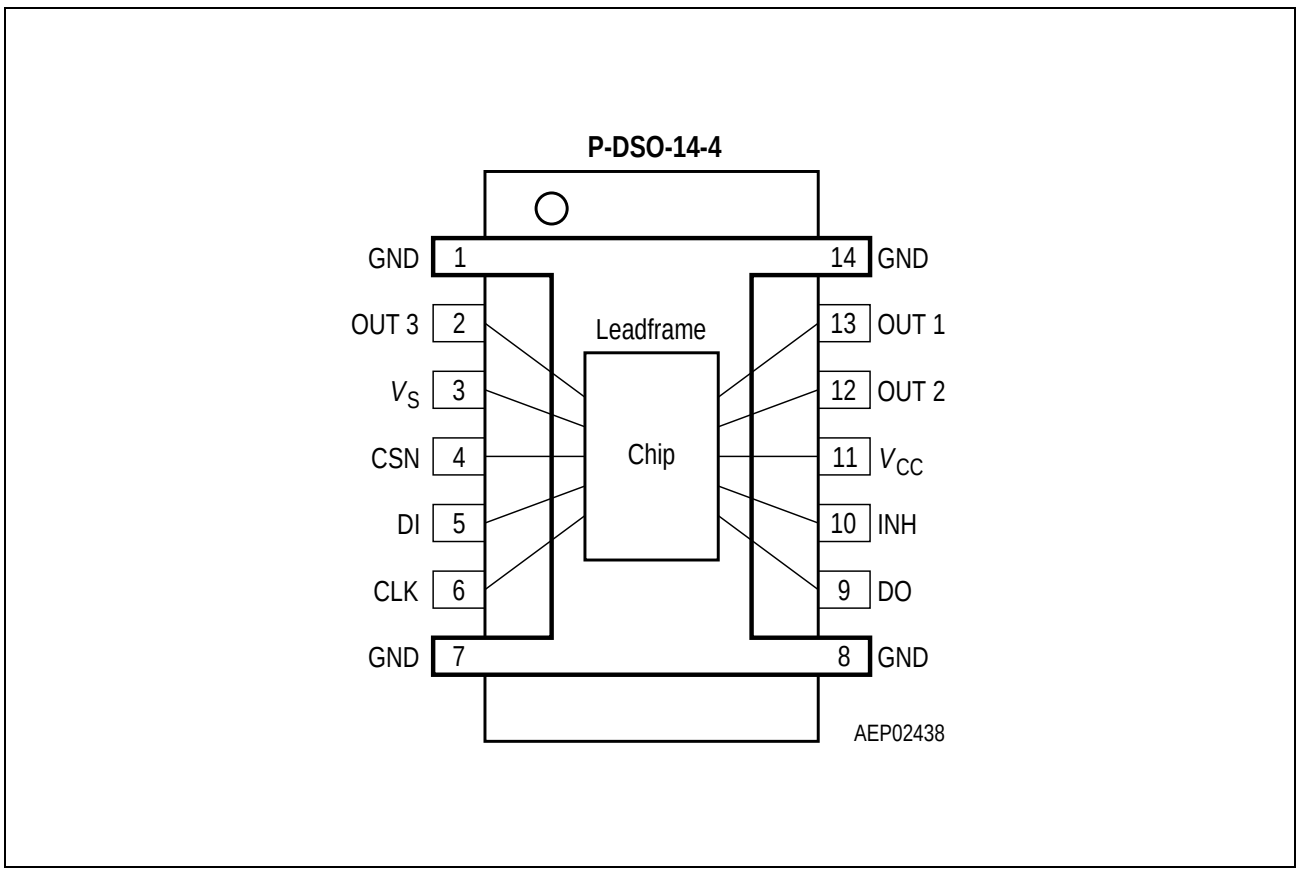

Figure 12 TLE 6208-3 G Pinning

Legend

GND	Ground
OUT	Output
V_S	Power supply voltage
V_{CC}	5V Supply
DI	Data Input
DO	Data Output
CLK	Clock Input
CSN	Chip-Select-Not Input
INH	Inhibit

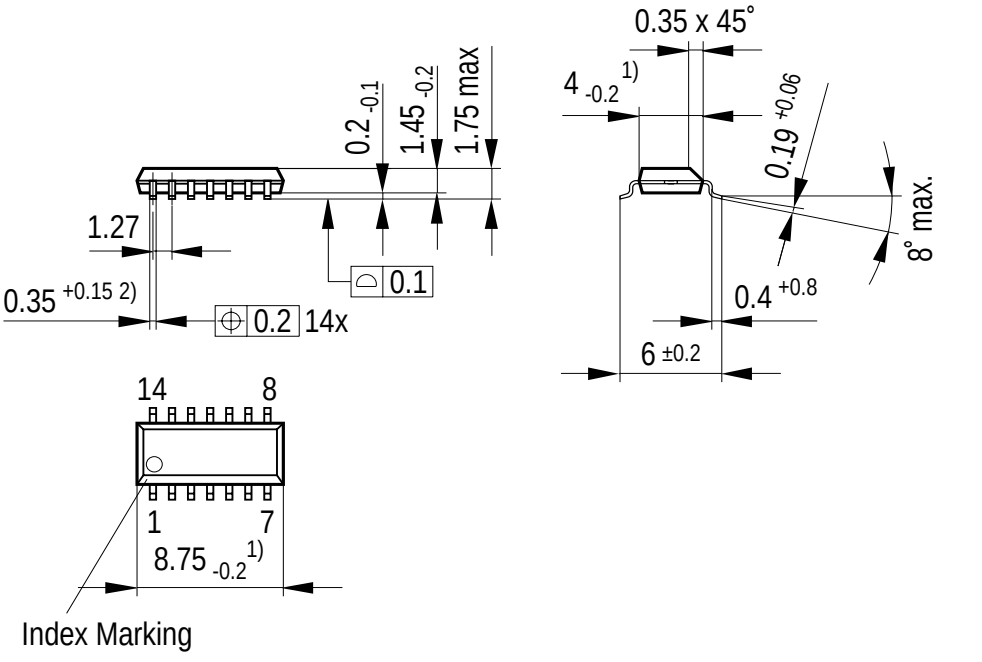

Figure 13 TLE 6208-3 G Package Diagram

The 4 connections of the serial interfaces (DI, DO, CLK and CSN) and the inhibit input are located close to each other from pin 4 to 10. The power supply and the output stages are located in the upper section of the device from pin 1 to 3 and 12 to 14. This considerably simplifies PCB design.

In order to use the PCB as a heat sink, as many copper-covered surfaces as possible should be located beside the GND connections, especially at pin 1 and pin 14. Thermal resistance can also be significantly reduced by using termal wire holes in combination with a double side PCB with 70 µm power copper layers next to the IC.

Of the wide range of possible applications, the one shown in **Figure 14** and featuring a series of two motors which are required e.g. for vehicle mirror positioning. Quasi-synchronous control of the two motors can be achieved via software, although only one motor is driven at any time, in a sort of time-multiplexing operation. The dissipated power is limited to very low values in this way.

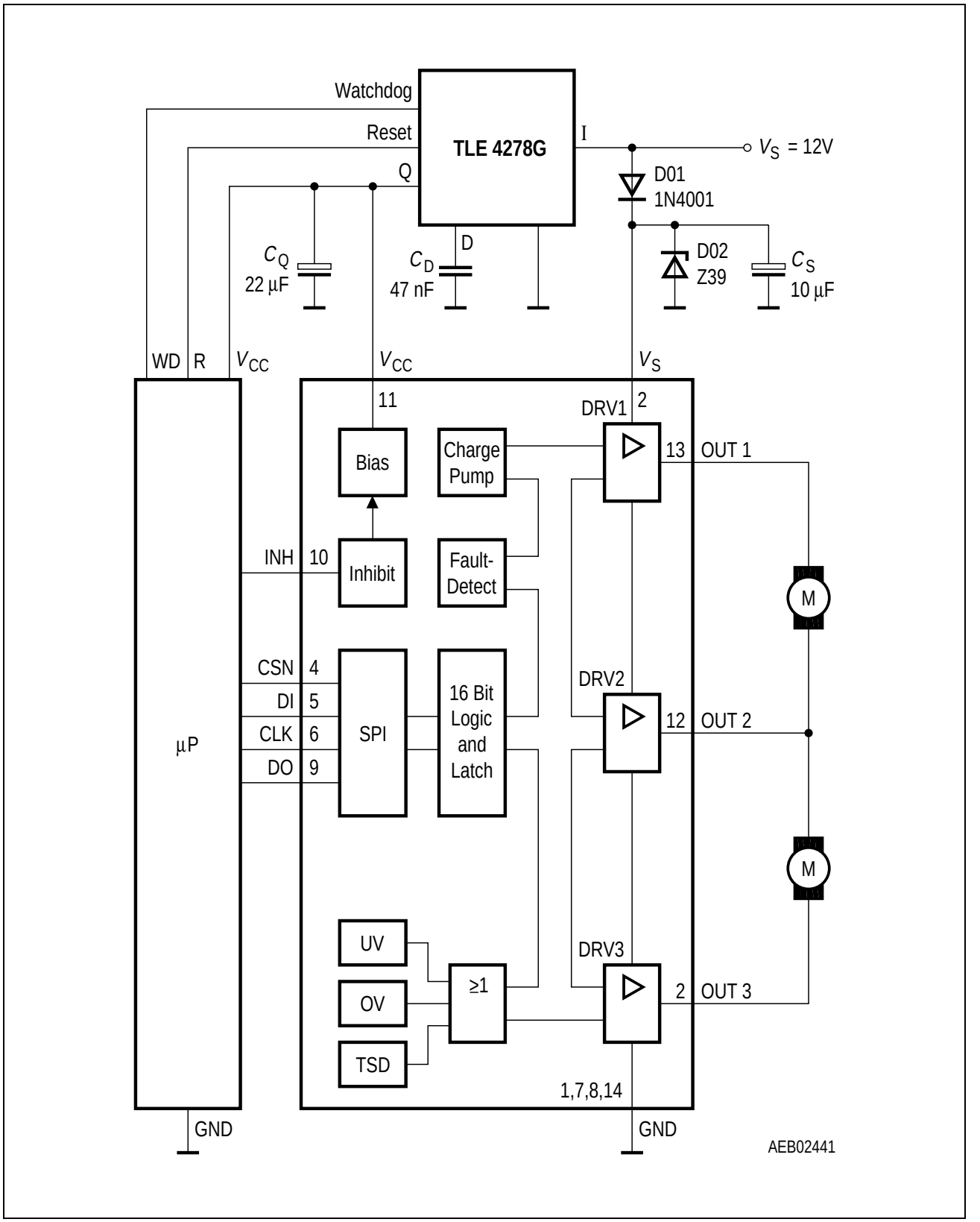

Figure 14 Application Circuit with TLE 6208-3 G and TLE 4278 G for Mirror Positioning

The Siemens low-drop voltage regulator **TLE 4278 G** can be used for the V_{CC} power supply. It has additional functions such as reset and watchdog for integrated controller management, features excellent EMC stability and is also available in a P-DSO-14 package. If this voltage regulator does not meet the application requirements, there is a wide range of different Siemens low-drop voltage regulators available.

The external circuitry of the **TLE 6208-3 G** is very simple, because e.g. pull-up, pull-down resistors or freewheeling diodes are already integrated. Only one blocking capacitor C_S to V_S and one diode for the reverse-polarity protection are needed. The capacitor C_S has to store any reverse inductive energy, because the diode prevents the current flow back to the power supply. For this reason C_S should not be too small.

If a Zener diode of e.g. 36 V is connected from V_S to GND then this rule no longer applies. C_S can be considerably smaller in this case (a few µF). The slew rate of the supply voltage dV_S/dt is now the determining parameter. C_S should be selected so that dV_S/dt remains clearly below 10 V/µs.

High power-on peak currents frequently occur in these applications. These may be up to an order of magnitude higher than the rated current. The **TLE 6208-3 G** can switch load currents of up to 3 A per channel if the overcurrent lockout has been deactivated by setting Bit 13 to L. Once the power-on procedure has been completed, the overcurrent lockout can be reactivated via software control (Bit 13 to H), in order to protect the load (blocked motor etc.) and the IC against overload. If the current now rises above the cutoff threshold of typ. I_{SD} = 1.5 A during nominal operation, then the channel is disconnected after a dead time of typ. t_{DSD} = 25 µs. **Figure 11** shows a typical cutoff process: Shortly after the CSN control signal changes from L to H, the OUTL1 output is switched to overload and disconnected after the time t_{DSD}.

The V_S operating voltage range can be extended up to 40 V by setting the overvoltage Bit 15 to L. This therefore satisfies all the main industrial requirements.

6 Application Board and Control Software

For the purposes of laboratory testing and as a development system, an application board is available with various loads switched by a TLE 6208-3 G, together with Windows® control software.

Application Board Configuration

- 2 motors in series or
- Three sockets directly connected to the outputs for individual loads
- Test switches to demonstrate the diagnostic features if openload, short circuit of load, short circuit to the supply voltage or short circuit to ground occurs.

Figure 15 shows the schematic circuit diagram and **Figure 16** shows the associated PCB for the application board.

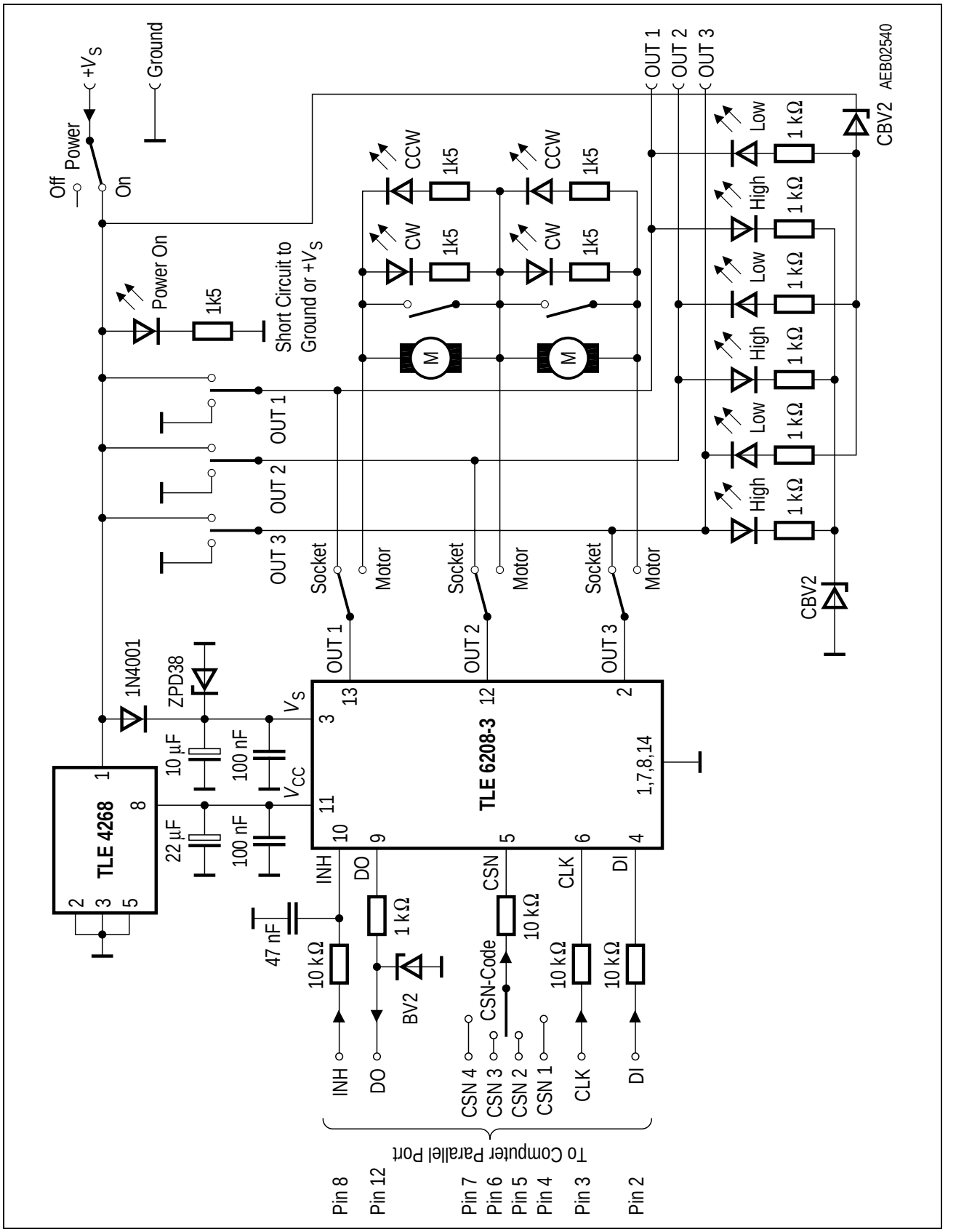

Figure 15 Schematic Circuit Diagram of the TLE 6208-3G Application Board

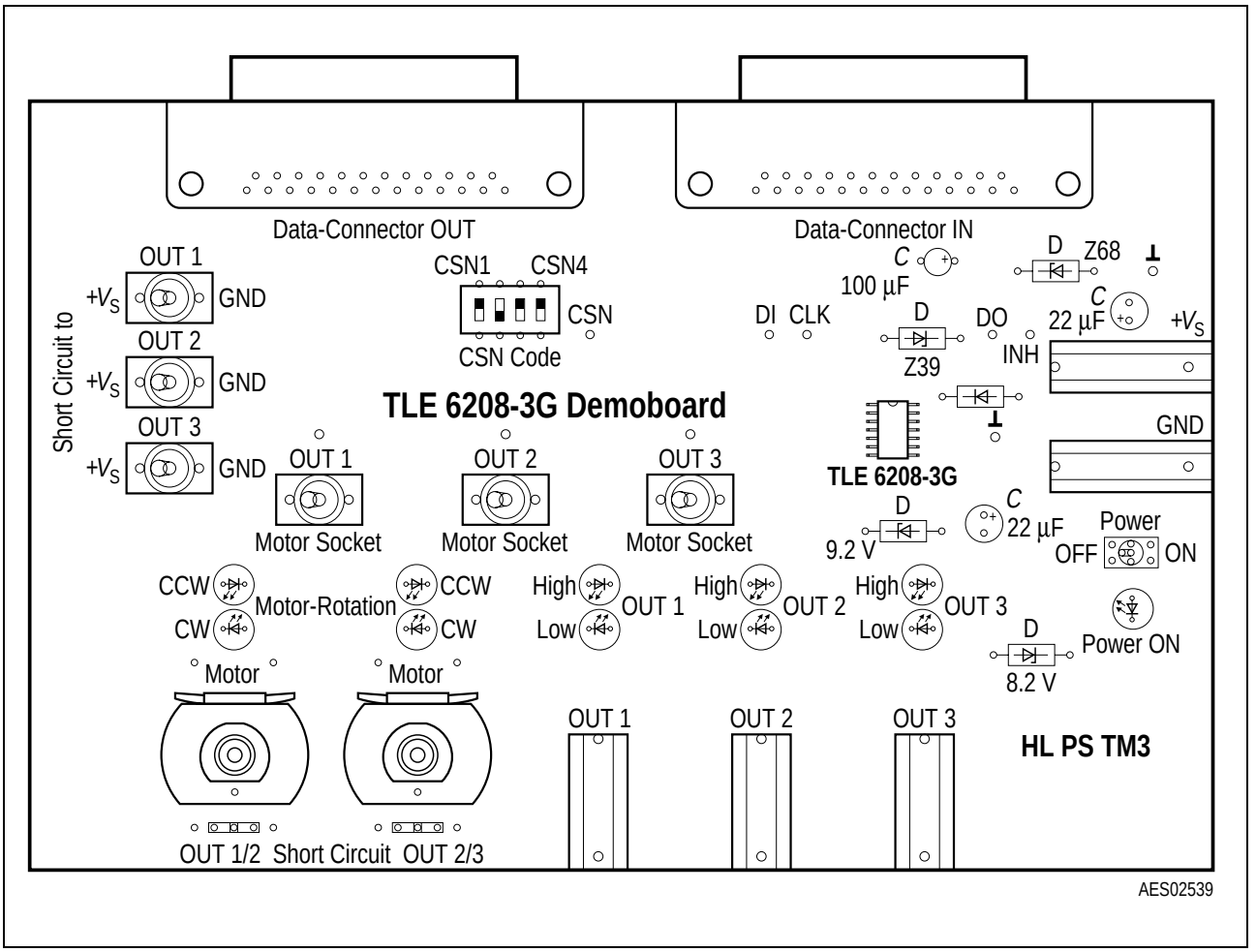

Figure 16 Layout of the TLE 6208-3G Application Board

The standard parallel interface on a PC is used to control and read the status word. Software running under Windows allows the simple definition of macros, which can be combined to create a sequence program. The standard screen masks are shown in **Figure 17**.

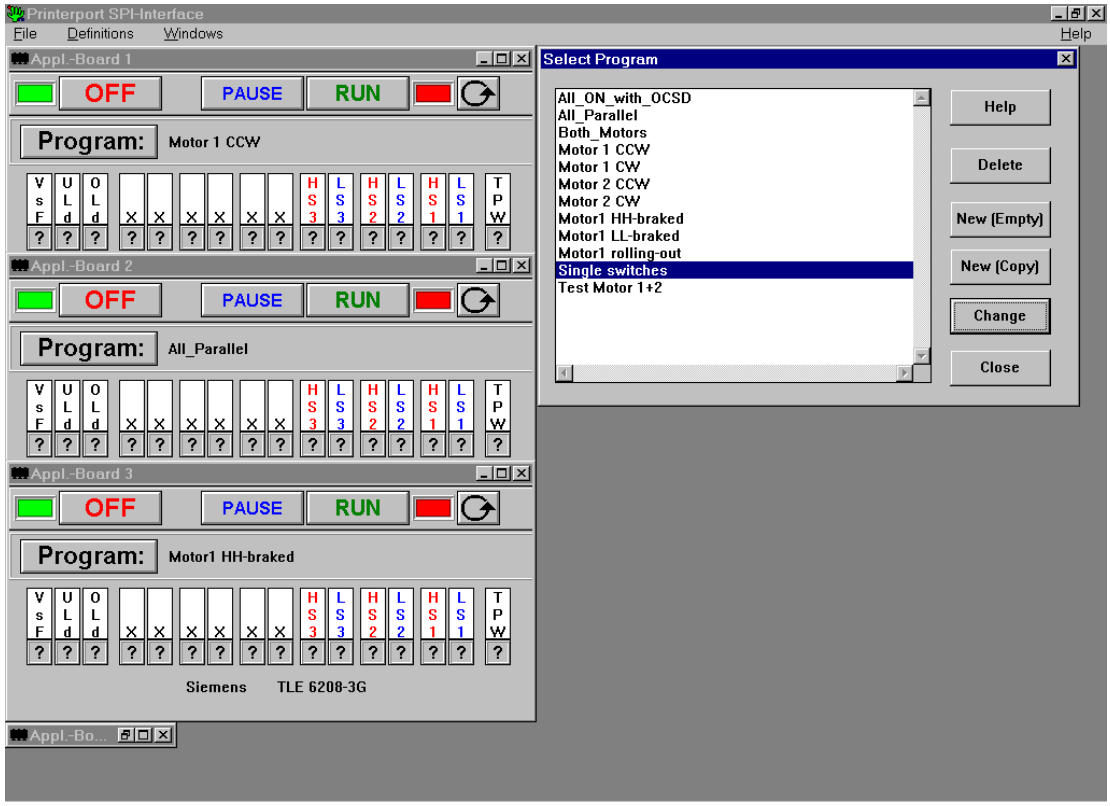

Figure 17 Standard Masks for the TLE 6208-3 G Control Software

The control software can address four boards via corresponding chip select lines. A small bus system can easily be constructed in this way.

The complete system can be disconnected via the INH button on the PC.

The only additional hardware required is a 12 V supply voltage and a standard PC with a printer interface. The documentation supplied with the application board contains lots of additional information to provide a better understanding of the IC. The application board and the control software can be obtained from Siemens sales offices.

7 Further Information

Order No.: TLE 6208-3 on request

Data sheets and further information are available on the latest semiconductor CD ROM and on the World Wide Web at:

http://www.siemens.de/Semiconductor/products/36/36.htm

or from our sales offices.