SIEMENS

The Universal Driver TLE 5208-6 G

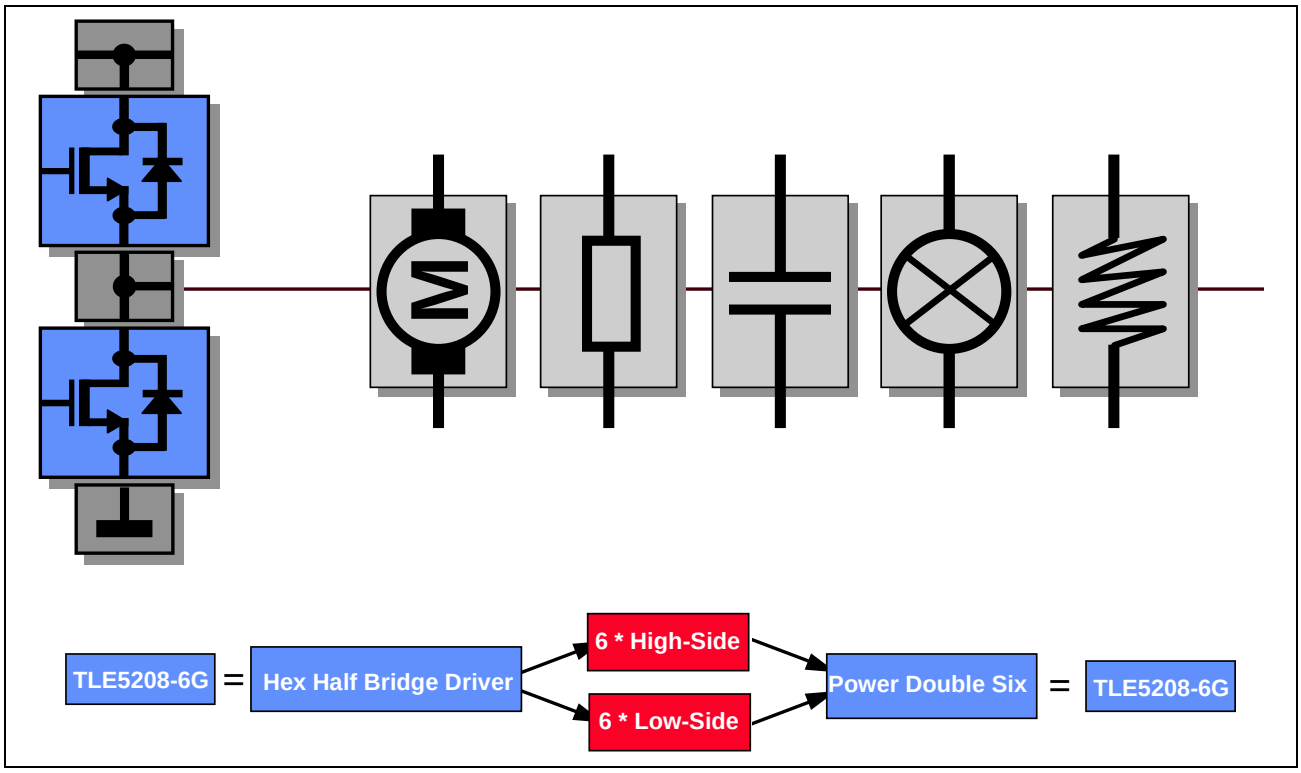


Figure 1

Features

- Six High-Side and six Low-Side-Drivers
- Free configurable as switch, halfbridge or H-bridge
- Optimized for DC motor management applications
- 0.6 A continuous, 1 A peak current per switch
- $R_{DS\ ON}$; typ. 1 Ω, @ 25 °C per switch
- Output: short circuit protected and diagnosis
- Overtemperature-Protection with hysteresis and diagnosis
- Standard SPI-Interface
- Very low current consumption (typ. 20 µA, @ 25 °C) in stand-by (Inhibit) mode
- Over- and Undervoltage-Lockout
- CMOS/TTL compatible inputs with hysteresis
- No crossover current
- Internal clamp diodes
- Enhanced power P-DSO-Package

Introduction

There is a growing requirement for flexible driver ICs up to 1 A in the increasingly complex electronic systems used for automobile electronics, industrial electronics and consumer electronics. The interface for these ICs has to be “bus-capable”, so that the complex control signals can be processed easily. The **TLE 5208-6 G** is a Smart Power IC, developed specially for this fast-growing market.

The **TLE 5208-6 G** contains 6 high-side (HS) drivers and 6 low-side (LS) drivers, which can be configured as required. These 12 switches are controlled via a 16-bit SPI interface. As a result, parallel or serial connections can be used to implement any switch applications required, and any motor controls in full-bridge or halfbridge configurations. This tristate functionality for motor halfbridges saves a complete halfbridge driver in the case of “multimotor applications”, since the motors can simply be connected in series (see **Figure 15**).

The IC is protected against short-circuits and overtemperatures. The SPI interface allows full diagnosis of overload and underload, overvoltage and undervoltage. In the event of serious overheating, the IC sends an overtemperature warning signal, so that the intelligent control system can intervene to reduce the dissipated power accordingly. This additional feature is designed for applications with increased safety requirements.

It is also possible to mask the overload current cut-off threshold via software, so that power-on current spikes such as those occurring with motor and lighting loads can be managed.

The overvoltage cut-off can likewise be disabled via software. This means that the IC can also be used for industrial electronics with supply voltages up to 40 V.

The **TLE 5208-6 G** has a separate inhibit input for standby running if required (or as a “safety disable”), which switches the module into sleep mode with an extremely low current consumption.

All of these functions are incorporated in a **P-DSO-28** package, thanks to the latest **Siemens Power Technology (SPT)**. The special leadframe design “enhanced power” reduces thermal resistance to such an extent that intelligent distribution of dissipated power allows nearly all loads to be handled simultaneously on the driver chip.

In summary: Where there is a requirement to switch an increasing number of loads, the **TLE 5208-6 G** will often provide the most cost-effective and technically elegant solution.

Functions of the TLE 5208-6 G

Figure 2 shows a block schematic diagram of the IC.

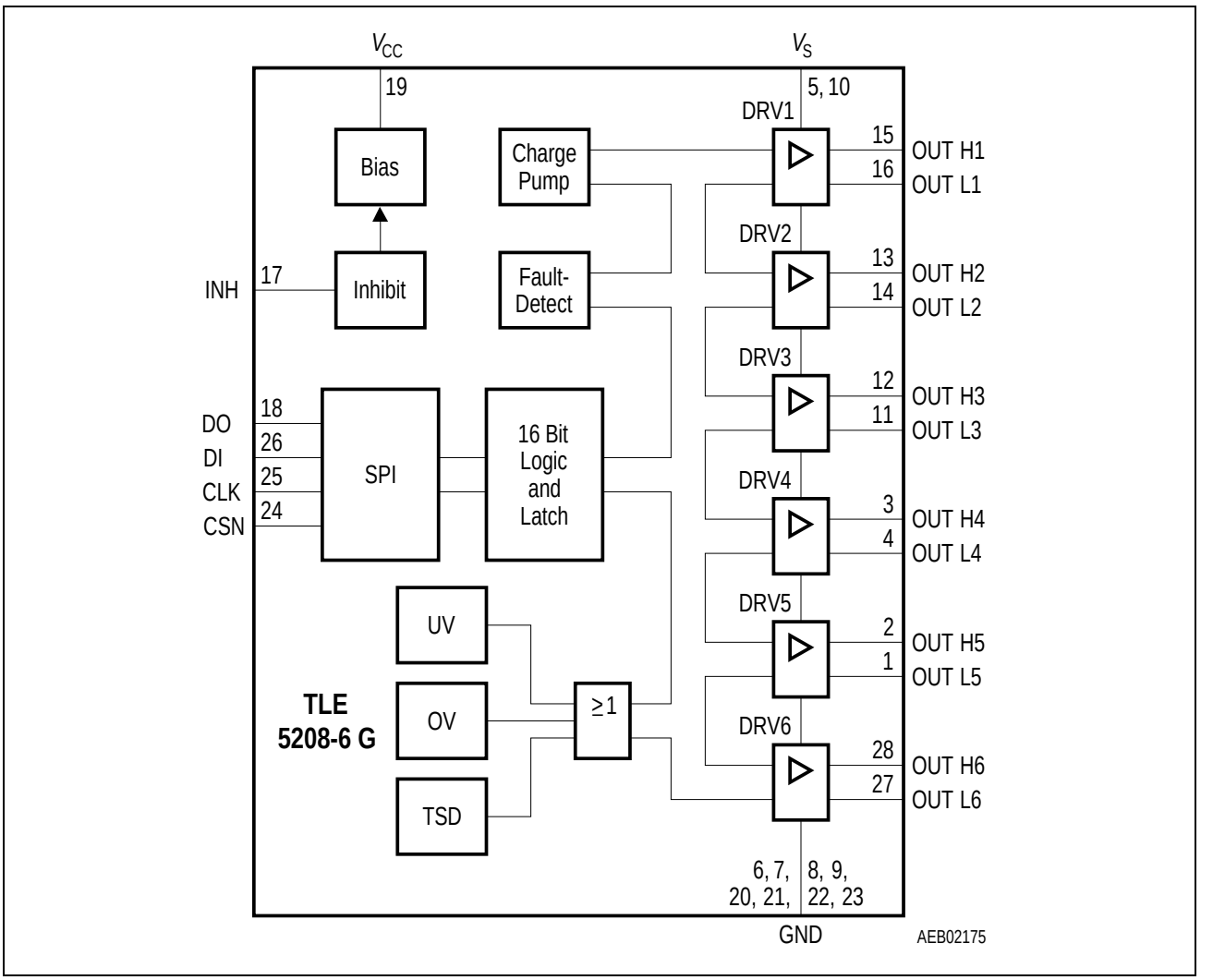


Figure 2 Block Schematic Diagram of the TLE 5208-6 G

There are 6 halfbridge drivers on the right-hand side. An HS driver and an LS driver are combined to form a halfbridge driver in each case.

The drivers communicate via the internal data bus with the logic and the other control and monitoring functions: undervoltage (UV), overvoltage (OV), overtemperature (TSD), charge pump and fault detect.

Two pins are provided for supply to the IC: All power drivers are connected to the supply voltage V_S. These are monitored by overvoltage and undervoltage comparators with hysteresis, so that the correct function can be checked in the application at any time.

The logic is supplied by the V_{CC} voltage, typ. with 5 V. The V_{CC} voltage uses an internally generated Power-on Reset (POR) to initialize the IC at power-on. The advantage of this system is that information stored in the logic remains intact in the event of short-term

failures in the supply voltage V_S. The system can therefore continue to operate following V_S undervoltage, without having to be reprogrammed. The “undervoltage” information is stored, and can be read out via the interface. The same logically applies for overvoltage. “Interference spikes” on V_S are therefore effectively suppressed.

The situation is different in the case of undervoltage on the V_{CC} connection pin. If this occurs, then the internally stored data is deleted, and the output levels are switched to high-impedance status (tristate). The IC is initialized by V_{CC} following restart (Power-on Reset = POR)

The 16-bit wide programming word or control word is read in via the DI data input, and this is synchronized with the clock input CLK. The status word appears synchronously at the DO data output.

The transmission cycle begins when the chip is selected with the CSN input (H to L). If the CSN input changes from L to H then the word which has been read in becomes the control word. The DO output switches to tristate status at this point, thereby releasing the DO bus circuit for other uses.

The INH inhibit input can be used to cut off the complete IC. This reduces the current consumption to just a few µA, and results in the loss of any data stored. The output levels are switched to tristate status. The module is reinitialized with the internally generated POR (Power-on Reset) at restart.

This feature allows the use of this module in battery-operated applications (vehicle body control applications).

Figure 3 shows an overview of the chip layout:

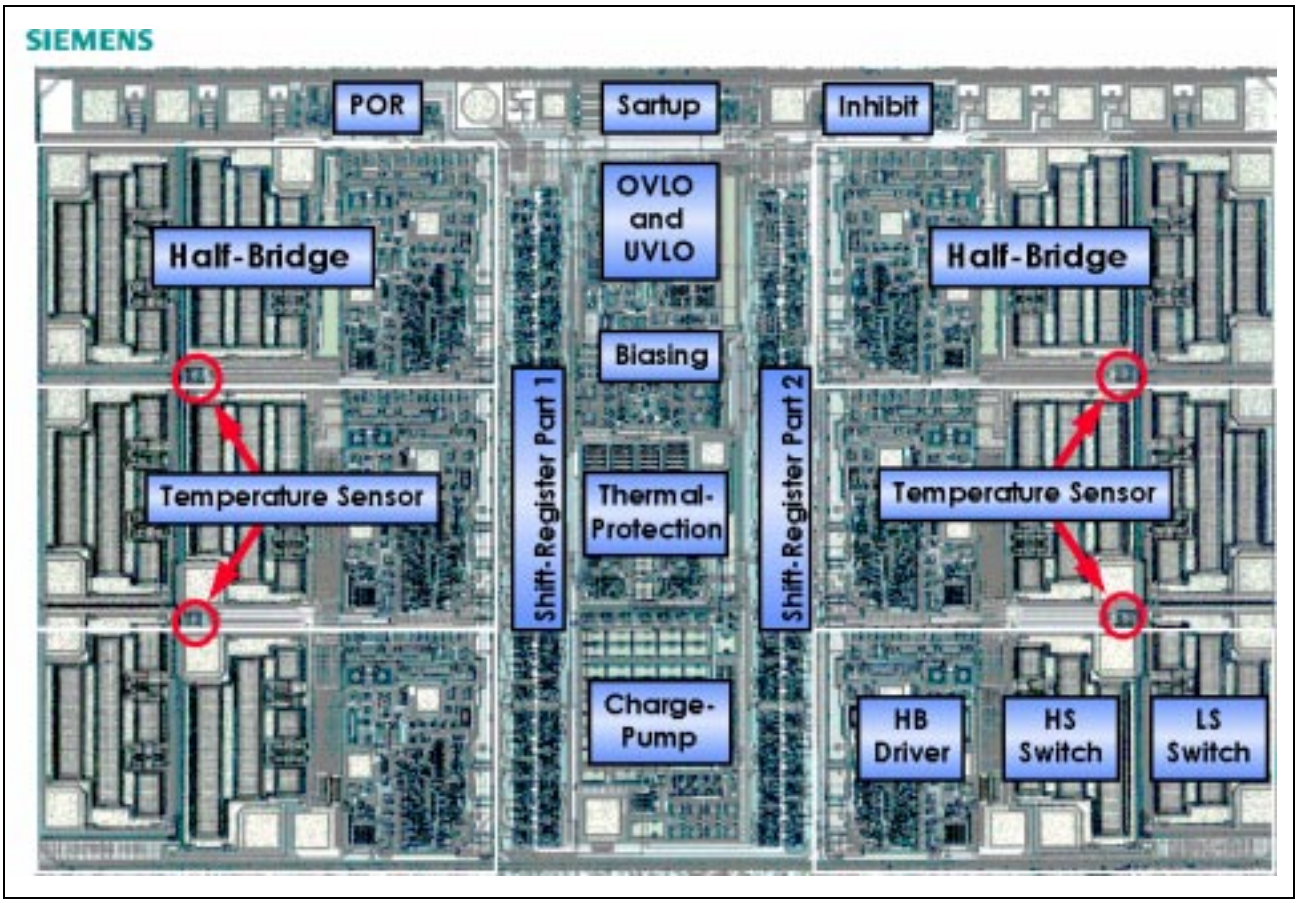


Figure 3 The TLE 5208-6 G Chip

There are 6 power semiconductor switches on both the right-hand and left-hand sides. This represents the optimum system of power distribution in terms of heating the other ICs. The analog levels which are sensitive to temperature gradients (e.g. the bandgap reference) are located at the exact center of the chip, i.e. the farthest possible from the power levels. These in turn can use the surface under the allocated driver levels to drain the dissipated heat. Optimum heat distribution on the chip is achieved using the Finite Element Method (FEM) for different cases.

The FEM model for the P-DSO-28-6 package, consisting of chip, glue, bonding wires, leadframes and molding compound, is shown in **Figure 4**.

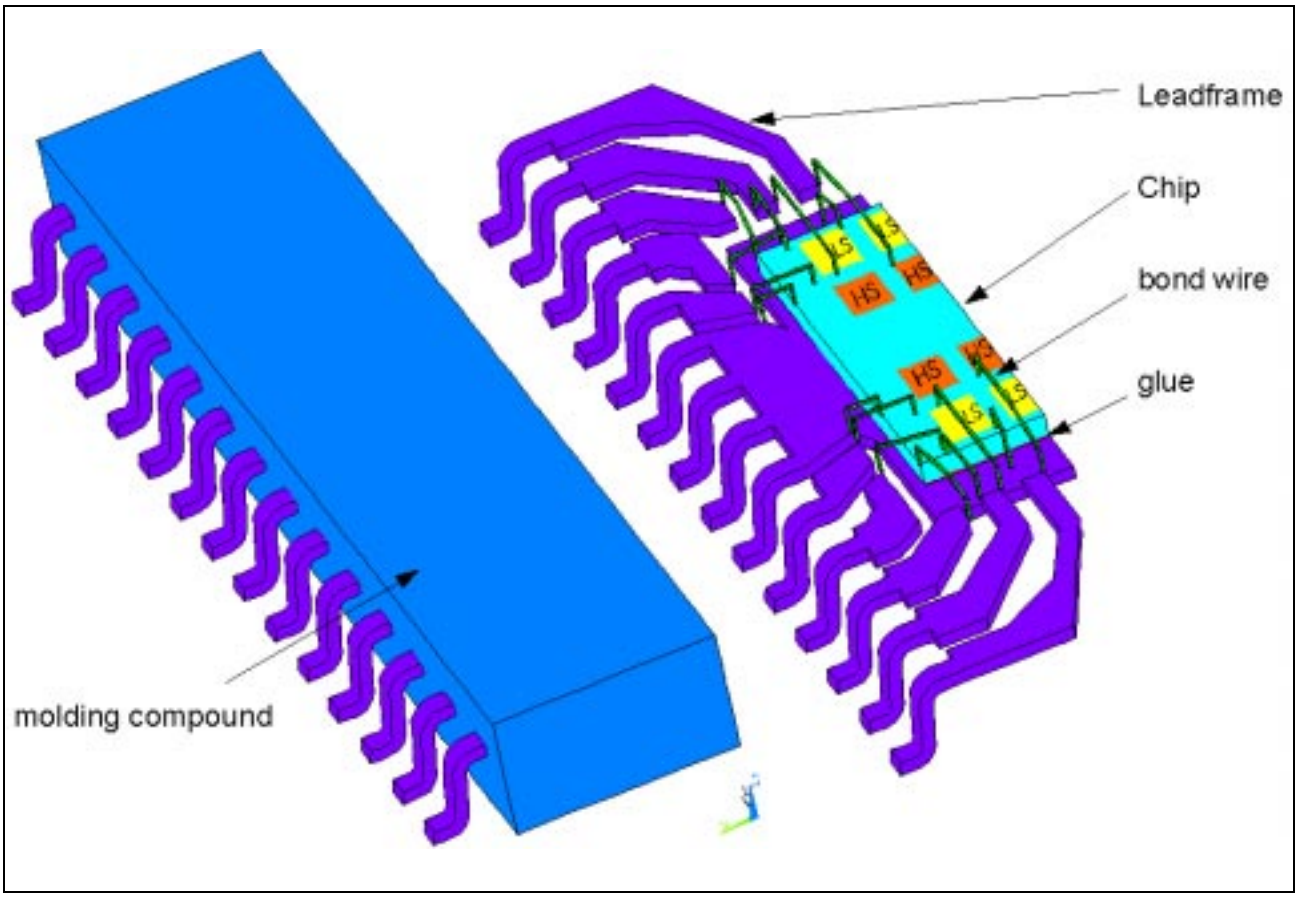


Figure 4 Finite Element Model (FEM): Half-Symmetrical View of P-DSO-28-6 Leadframe and TLE 5208-6 G Chip

The “enhanced power” leadframe is easy to identify, where the 4 central connections on each side (Pins 6 to 9 and 20 to 23) provide a metal bridge to the leadframe itself. These 8 pins on the leadframe therefore provide a very effective lateral heat drain.

The “worst-case” dissipated power occurs when all switches are loaded. **Figure 5** shows the temperature distribution for this scenario. Only a quarter of the layout is shown, since the rest is symmetrical.

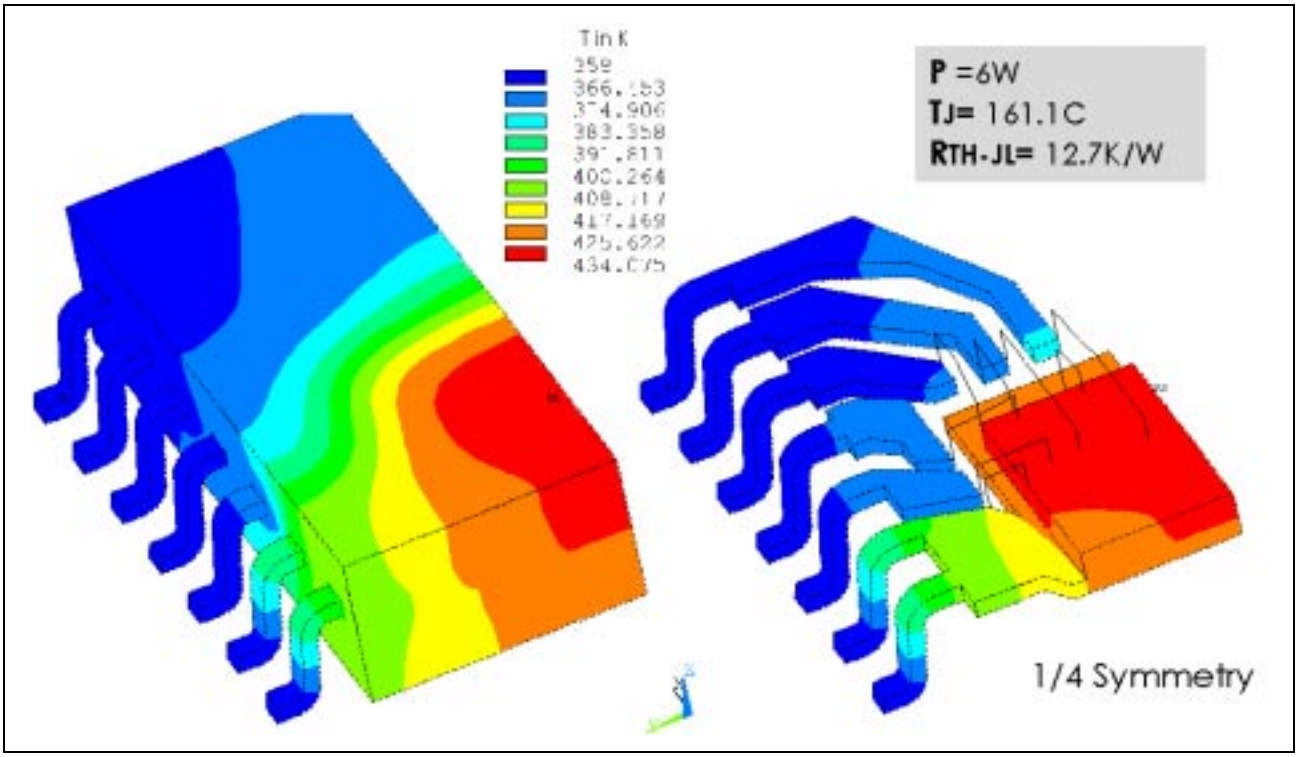


Figure 5 Temperature Distribution with Full Loading of all Switches with T_{Lead} = 85 °C (358K) and P_{HS} = 6 by 0.5 W, P_{LS} = 6 by 0.5 W

The greatest temperature difference in this case is approx. 75 °C. The static thermal resistance $R_{thj\text{-}Lead}$- is therefore only approx. 13 K/W.

Therefore: With a maximum permitted chip temperature of T_j = 150 °C, the **TLE 5208-6 G** works up to an environmental temperature of 85 °C. These values can be counted on for short periods, i.e. for applications with switching times of a few 100 ms, since the startup time constants of motors and the power-on time constants (inrush) of lights are normally less than 100 ms.

Since the thermal capacity of the PCB is not infinite, thermal resistance $R_{thPCB\text{-}A}$ for the PCB layout must be added to thermal resistance $R_{thj\text{-}Lead}$ in order to ascertain the environment for continuous operation. In the case of assembly on a 1.5 mm thick FR4 PCB without cooling surfaces in addition to Pins 6 to 9 and 20 to 23, it can be assumed that $R_{thPCB\text{-}A}$ = 30 K/W. This value can be reduced to approx. 20 K/W with cooling areas on the PCB.

Figure 6 shows another, particularly interesting scenario. In this case, the chip is placed under maximum asymmetric thermal load. All of the switches on one side of the chip generate 0.5 W dissipated power. Half-symmetry must therefore be used to illustrate this.

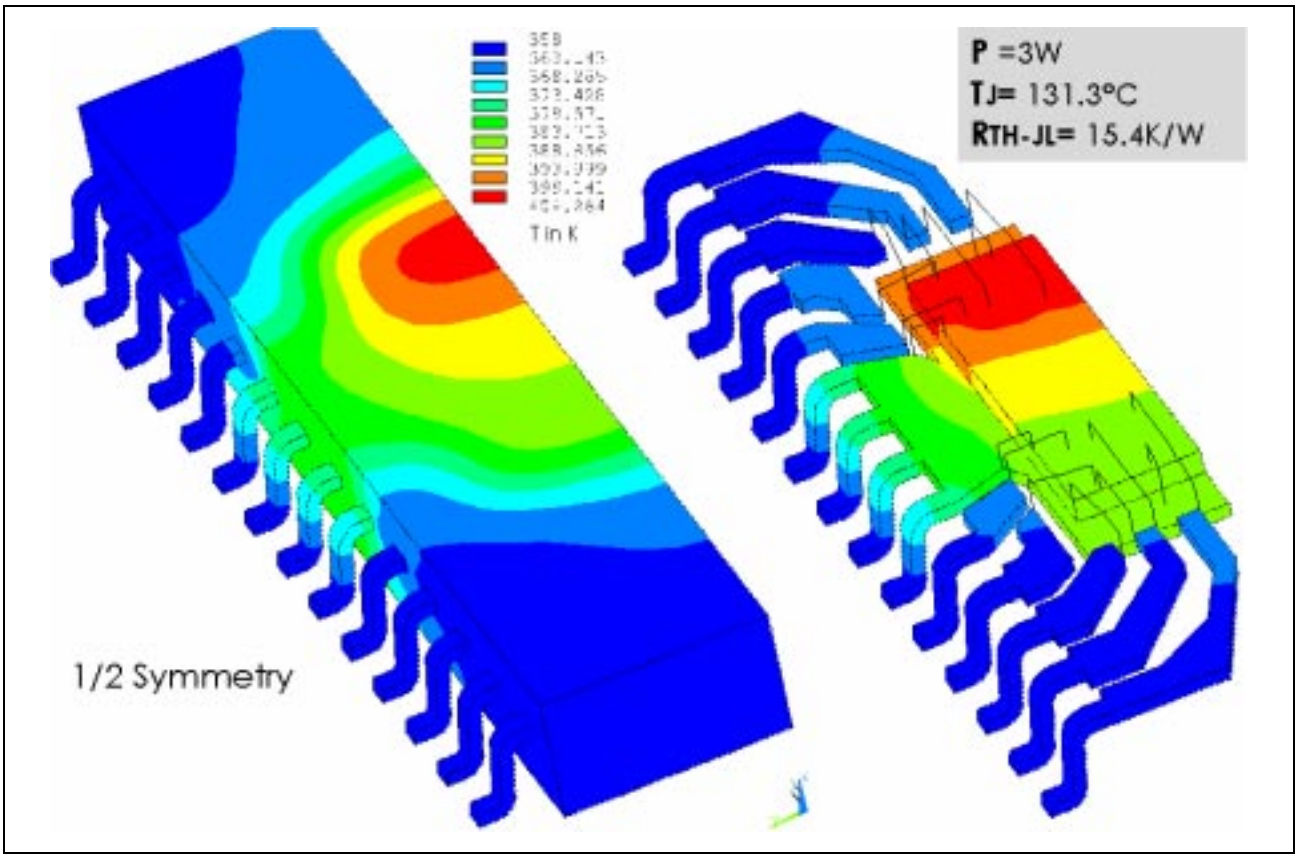


Figure 6 Temperature Distribution for Asymmetrical Operation with T_{Lead} = 85 °C (358K) and P_{HS} = 3 by 0.5 W, P_{LS} = 3 by 0.5 W

The greatest temperature difference is now only approx. 45 °C. The static thermal resistance $R_{thj\text{-}Lead}$ has risen to an acceptable 15 K/W. It is easy to see the lateral heat flow, firstly towards the center of the chip and then at right angles along the “cooling connections” out of the package.

As in the previous case, the temperature peaks are significantly lower for pulsed operation. For estimating purposes, the dyn. thermal resistance $Z_{thj\text{-}Lead}$ for single-pulse operation under load was calculated as per **Figure 6** and shown in **Figure 7**.

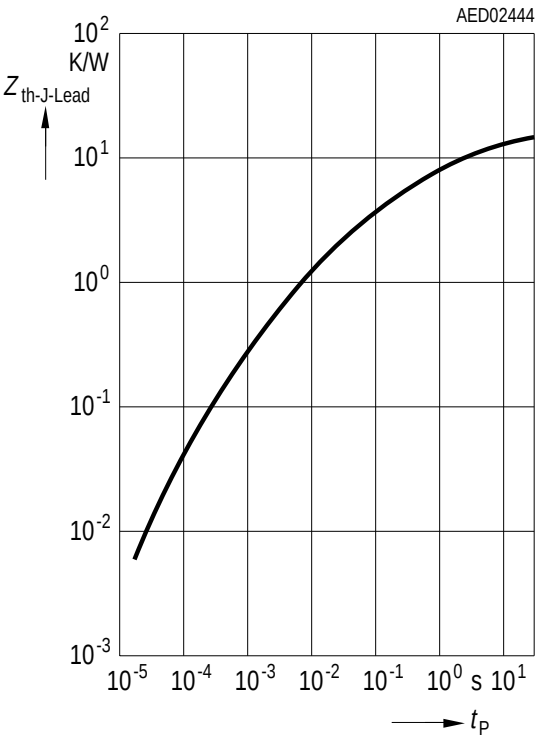


Figure 7 Transient Thermal Resistance of the TLE 5208-6 G for Single-Pulse Operation

Output Driver Levels

Every driver block from DRV 1 to 6 contains a low-side driver and a high-side driver. The output connections have been selected so that each HS driver and LS driver pair can be combined to form a halfbridge by short-circuiting adjacent connections. The full flexibility of the configuration can be achieved by dissecting the halfbridges into “quarter-bridges”. **Figure 8** shows examples of possible applications.

When commutating inductive loads, the dissipated power peak can be significantly reduced by activating the transistor located parallel to the internal freewheeling diode. A special, integrated “timer” for power ON/OFF times ensures there is no crossover current at the halfbridge.

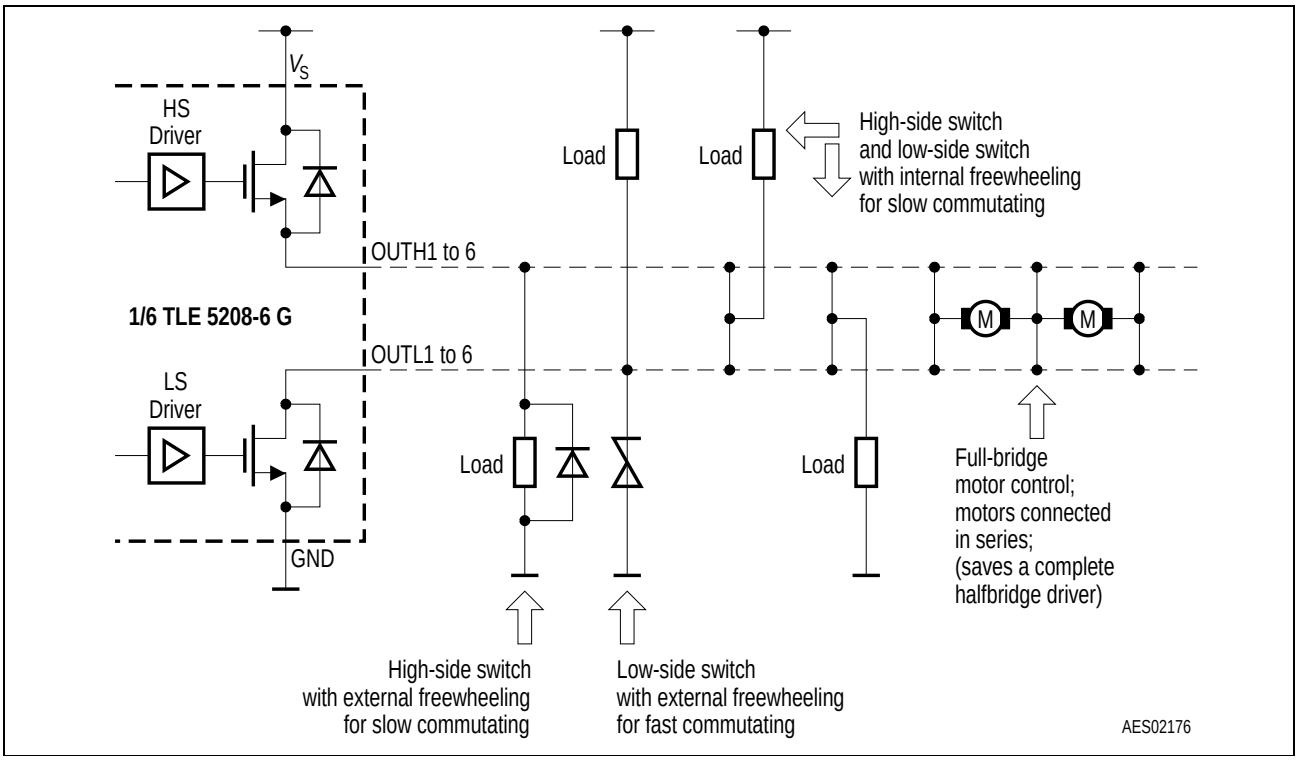


Figure 8 Configuration Examples for "Quarter" Bridges on the TLE 5208-6 G

The following detailed block schematic diagrams of the output levels are provided for further clarification. The low-side driver connection is shown in **Figure 8**.

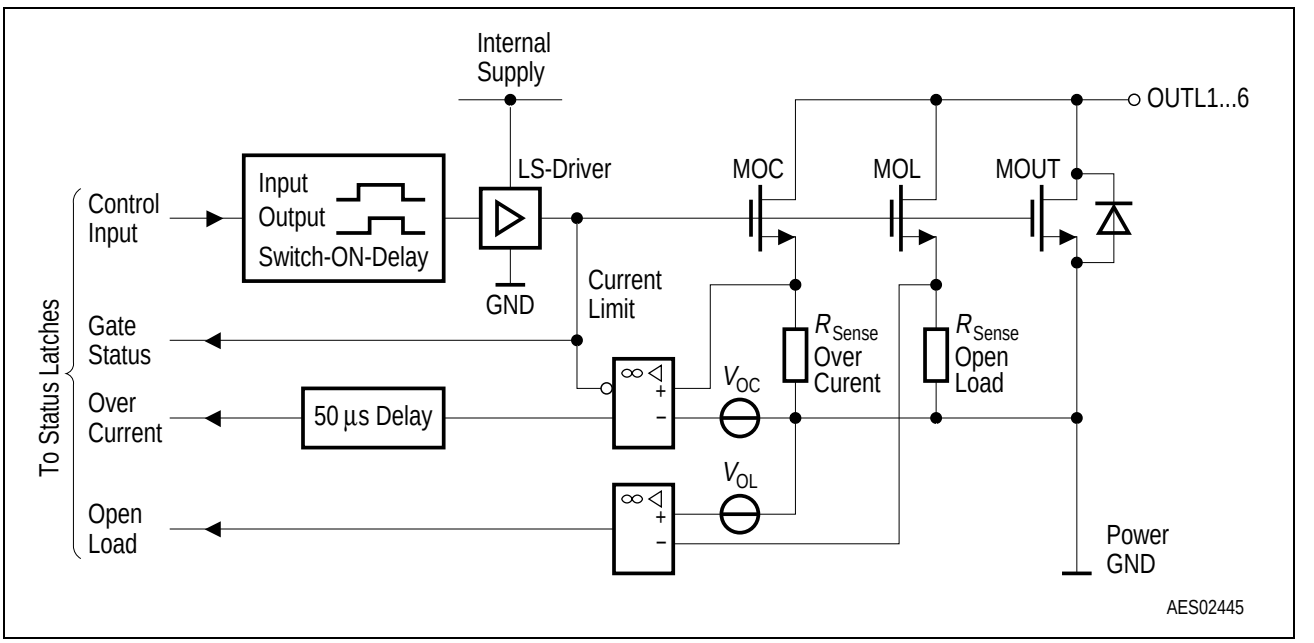


Figure 9 The Low-Side Driver Connection on the TLE 5208-6 G

The output transistor MOUT, a power MOS (D-MOS) transistor, has an R_{DSON} of typ. 1 Ω at 25 °C.

Its source connection is linked to the Power-GND connection. The drain connection provides the output OUTL1 to OUTL6. Two sense devices (transistor, resistor and comparator) are used to detect overloads and underloads.

In the event of overcurrent, the gate voltage is also restricted. Following a specified dead time of typ. 50 µs, the logic cuts off the output transistor, and stores the information “Overcurrent at Switch X” in the status register.

It is possible to override the cut-off after 50 µs by resetting the overcurrent ON/OFF bits. However, the current continues to be restricted. This function allows the power-on of e.g. lights, motors, and heavy capacitive loads, which have high inrush currents and relatively short conducting periods.

Furthermore, delayed power-on allows the low-side drivers to be adapted to the switching times of the HS switch. In the case of halfbridge operation, this ensures that the HS switch is turned off before the LS switch starts to conduct (suppression of crossover current).

In order to ensure reliable underload detection in the case of commutating, inductive loads, an identical underload dead time has been integrated for all channels (including the high-side switches). The timer for this dead time (typ. 300 µs is started with the positive edge of the CSN. Explanation: All commutation processes start with this edge (e.g. to drive a motor in reverse mode), if inductance is present. Commutation processes must be interpreted as underload by the underload detection system, since the current requires a finite period firstly to change the polarity and then to exceed the underload threshold. This dead time allows this “false information” to be suppressed, and its storage in the status register is prevented.

Like the LS driver, the high-side driver circuit shown in **Figure 10** contains an overcurrent read-out, an undercurrent read-out and a current limit. Only the sense resistors are now in the drain branch. The comparator inputs therefore have supply voltage V_S as a fixed reference potential.

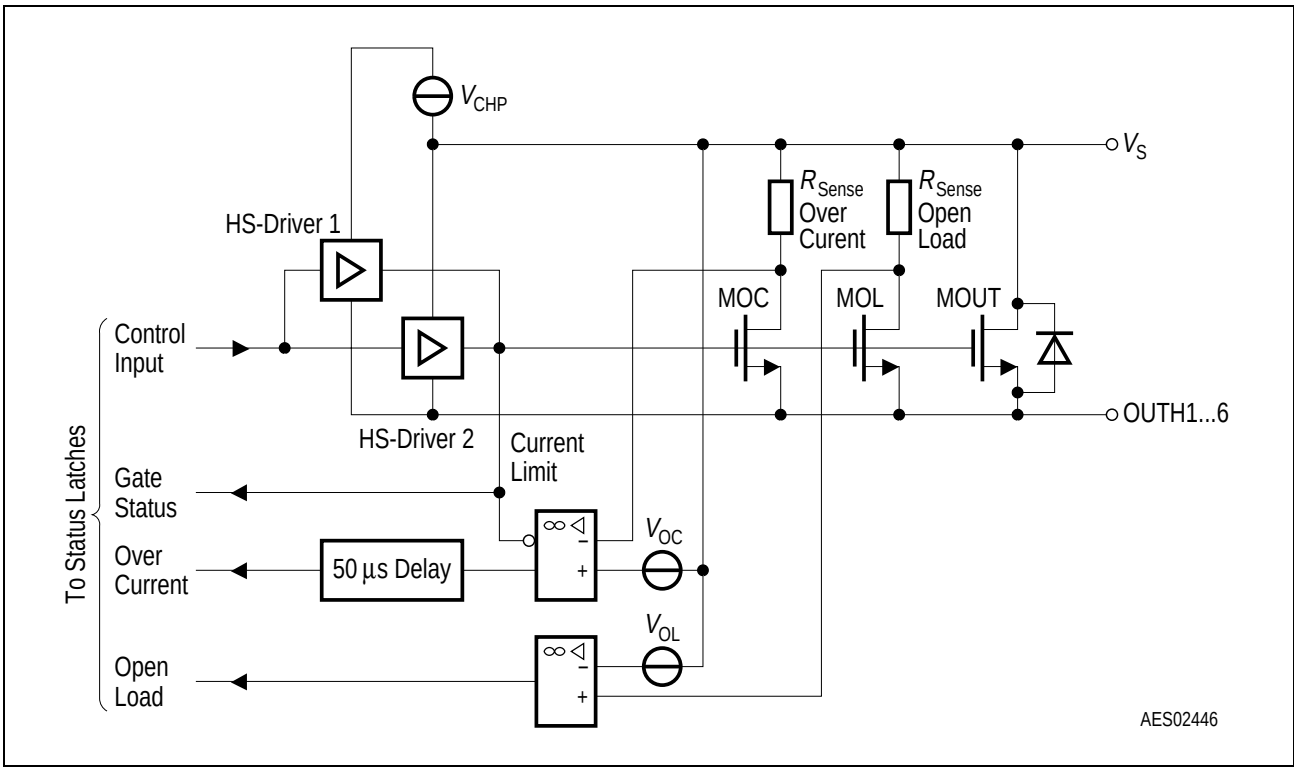


Figure 10 The High-Side Driver Circuit on the TLE 5208-6 G

The signal processing which takes place in logic is similar to that of the LS switch. However, gate control is now supplied by the internal charge pump voltage VCP, which is approx. 12 V greater than V_S.

Special circuit technology is used to provide “tristate-compatible” output levels. This characteristic is particularly important in the case of halfbridge/full bridge operation, e.g. if independent control is required for motors which are connected in series.

The start-up configuration of the **TLE 5208-6 G** also ensures that no uncontrolled switching of the output levels occurs in the whole of the undervoltage range for V_S and V_{CC}. All output transistors are switched to tristate status. The functional range of the supply voltages is therefore specified up to 0 V.

The most important data for the output drivers is summarized again in **Table 1**.

Table 1 The Main Parameters of the Output Driver

Parameter	Symbol	Value for T_j = – 40 to 150 °C			Unit
		min.	typ.	max.	
ON resistance	R_{DSON}	–	1	2.5	Ω
Tristate leak current	I_{QL}	–	–	1	mA
Cutoff current threshold	I_{SD}	1.0	–	2.0	A
Cutoff dead time	t_{dSD}	25	–	80	µs
Current limit	I_{OCL}	–	3.0	5	A
Underl. curr. threshold	I_{OCD}	10	–	100	mA
Underload dead time	t_{dOC}	200	–	400	µs

Programming the TLE 5208-6 G

The SPI interface is used to control the module or read out the status word. **Figure 11** shows a typical read/write cycle in the form of an oscillogram.

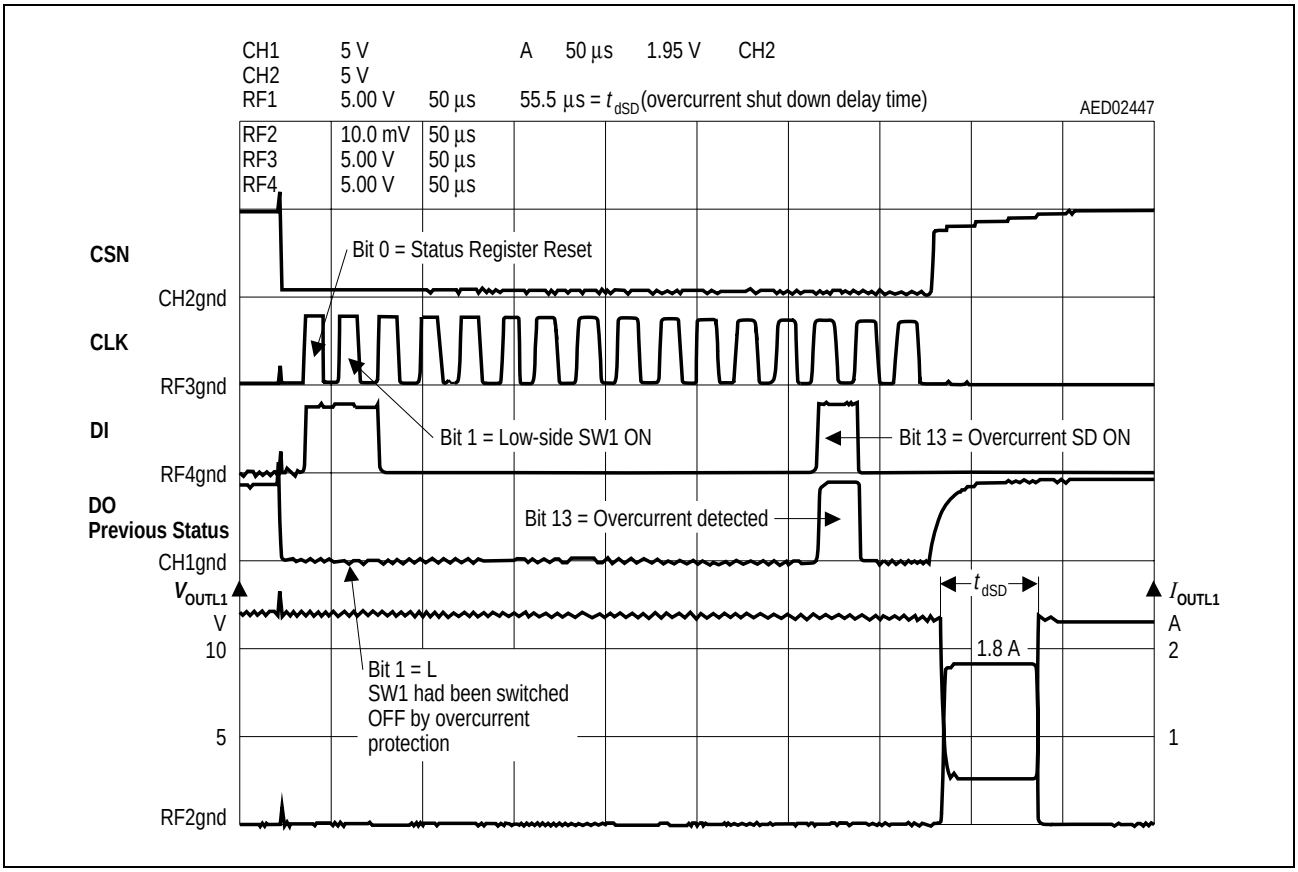


Figure 11 TLE 5208-6 G Read/Write Cycle

Read-in of the 16-bit long control word begins after the H-L edge of the CSN signal. Read-in of the control word at the DI input is synchronized with the CLK clock. The status word for the previous control word appears at the data output DO. When the CSN signal changes from L to H, the data which has been read in takes effect. The module is programmed. This is shown in **Figure 11** where the two lower lines represent the voltage and the current of LS Switch 1 (was programmed with Bit 1 = H at power-on; Bit 0 = H has also been read in). After approx. 50 µs the module cuts off the output because it is overloaded with more than 2 A, and Bit 13 = H (current cutoff active) was programmed at the same time. The exact timing is not detailed here. This data is specified in the TLE 5208-6 G Data Sheet.

Special software has been developed to provide simple control of an application board. This can be run under Windows® on any standard PC. The printer interface LPT1 or LPT2 can be used as an “SPI interface with inhibit”. Further details are provided below.

Figure 12 and **Figure 13** show the allocation of functions and switches to the control and diagnostics word

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OVLO on/off	not used	Overcurrent SD on/off	HS-Switch 6	LS-Switch 6	HS-Switch 5	LS-Switch 5	HS-Switch 4	LS-Switch 4	HS-Switch 3	LS-Switch 3	HS-Switch 2	LS-Switch 2	HS-Switch 1	LS-Switch 1	Status Register Reset

H = ON

L = OFF

Figure 12 The TLE 5208-6 G Control Word

Details are as follows:

- **Bit 0: Status Register Reset**

  Bit 0 = L All data remains stored in the status register.

  Bit 0 = H The status register is reset after every programming cycle.

- **Bits 1 to 12: Driver control:**

  Bit 1 = L LS Switch 1 OFF

  Bit 1 = H LS Switch 1 ON

  Bit 2 = L HS Switch 1 OFF

  Bit 2 = H HS Switch 1 ON

  and so on until

  Bit 12 = L HS Switch 6 OFF

  Bit 12 = H HS Switch 6 ON

- **Bit 13: Overcurrent lockout:**

  Bit 13 = L Overcurrent lockout after 50 µs is not active; the current is limited to typ. 3 A.

  Bit 13 = H Overcurrent lockout after 50 µs is active.

- **Bit 14: Not used**

- **Bit 15: Overvoltage lockout**

  Bit 15 = L Overvoltage lockout (OVLO) is not active.
  The module can be operated up to V_S = 40 V.

  Bit 15 = H Overvoltage lockout is active.
  All outputs are cut off if V_S = min. 34 V.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Power Supply failf	Underload	Overload	Status HS-Switch 6	Status LS-Switch 6	Status HS-Switch 5	Status LS-Switch 5	Status HS-Switch 4	Status LS-Switch 4	Status HS-Switch 3	Status LS-Switch 3	Status HS-Switch 2	Status LS-Switch 2	Status HS-Switch 1	Status LS-Switch 1	Temp. Prewarning

High Means Switch is ON

Low Means switch is OFF

Figure 13 The TLE 5208-6 G Status Word

The status word transmits the following information:

- **Bit 0: Overtemperature warning**

  If the chip temperature rises above typ. T_j = 145 °C, then Bit 0 is set to H.

  The information is stored in the status register.

  At typ. T_j = 175 °C, all output levels are cut off (emergency off).

  The data remains stored in all registers.

  If the chip temperature drops below typ. T_j = 125 °C, then Bit 0 is set to L.

  The information in the status register is overwritten (all-clear).

- **Bits 1 to 12: ON/OFF status indicator of the driver levels**

  Status bits of the switches; assigned in the same way as the control word.

  This has the advantage that a simple EX-OR comparison of the control and status word after two read-ins is sufficient to check the transmission path and the application.

  The driver status is inserted in the status word. Analysis is performed by measuring the gate voltage at the output transistors.

  L means: Output level is deactivated (inhibited)

  H means: Output level is active (conducting)

- **Bit 13: Overload/short-circuit indicator**

  “Overload” information is output here.

  H means that one or more of the 12 switches is or was overloaded. Status Bits 1 to 12 can be used to identify the switch concerned.

- **Bit 14: Underload/broken wire indicator**

  “Underload” information is output here.

  H means that underload has been detected on one or more of the 12 switches.

  The exact identification of the switch concerned is likewise given by status bits 1 to 12.

- **Bit 15: Supply voltage fault**

  “Overvoltage or undervoltage at V_S” information is output here.

  H means that overvoltage or undervoltage has been or is still being detected at V_S. Overvoltage is also indicated if Bit 15 of the control word has been set to L (OVLO not active).

All information is stored, unless Bit 0 of the control word is set and a new control cycle has been initiated (see Bit 0 of the control word). In the same way, the status register is deleted by turning V_{CC} on or off, or by deactivating the IC via the inhibit input (INH = L).

Applications

The following section is concerned with possible applications of the IC.

The most important information is the pin configuration (pinning) and the package dimensions, and these are shown in **Figure 14** and **Figure 15**.

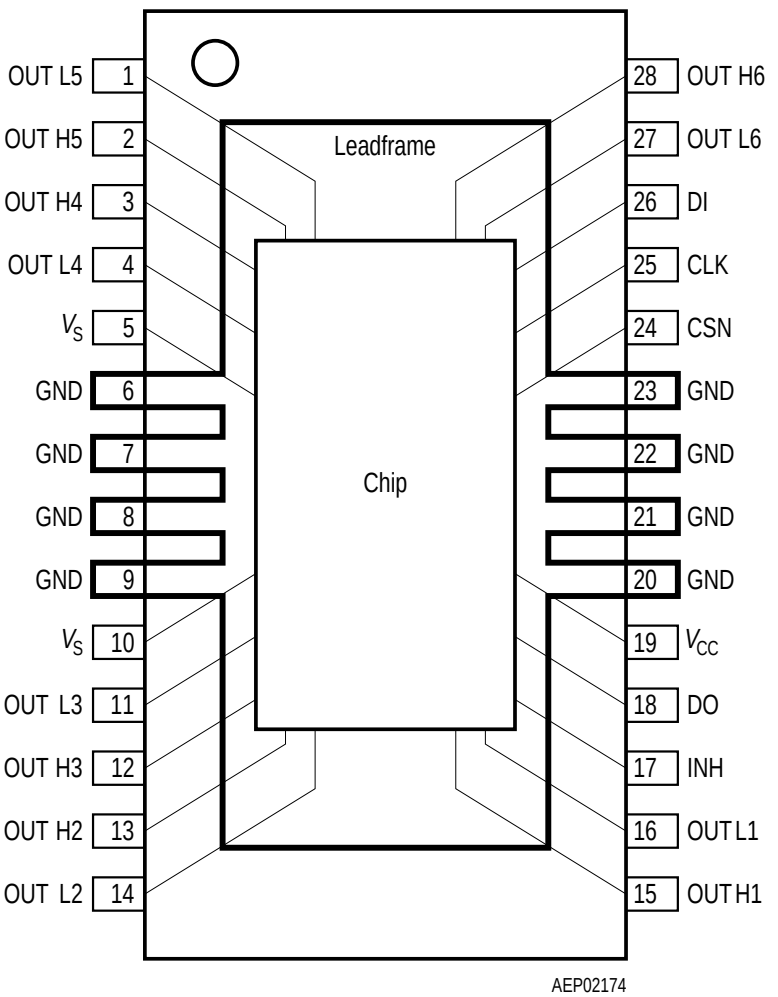
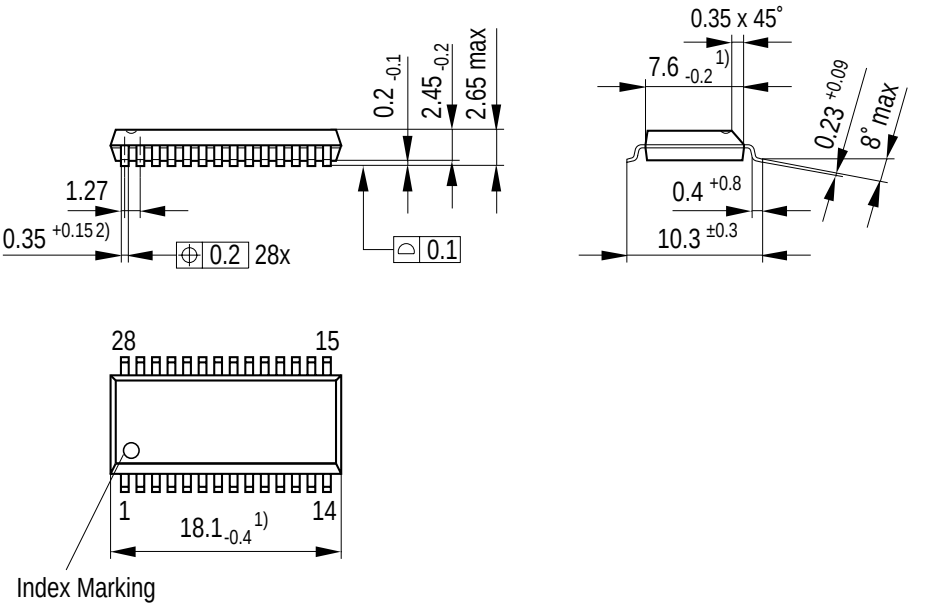


Figure 14 Pin Configuration

P-DSO-28-6
(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusions of 0.15 max rer side
2) Does not include dambar protrusion of 0.05 max per side

GPS05123

Figure 15 Package Outlines

The 4 connections of the serial interfaces (DI, DO, CLK and CSN) and the inhibit input are located close to each other on the same side of the package. This considerably simplifies PCB design.

In order to use the PCB as a heat sink, as many copper-clad surfaces as possible should be located beside the GND connections. Thermal resistance can also be significantly reduced by using through holes next to the IC.

Of the wide range of possible applications, the one shown in **Figure 16** and featuring a series of five motors is particularly interesting.

Five motors are required e.g. for vehicle air conditioning. Quasi-synchronous control of all 5 motors can be achieved via software, although only one motor is driven at any time, in a sort of time-slicing operation. The dissipated power is limited to very low values in this way.

Even the requirement to maintain a continuous brake on the “air intake motor” due to dynamic pressure (caused by the relative wind), can be satisfied by means of suitable software control.

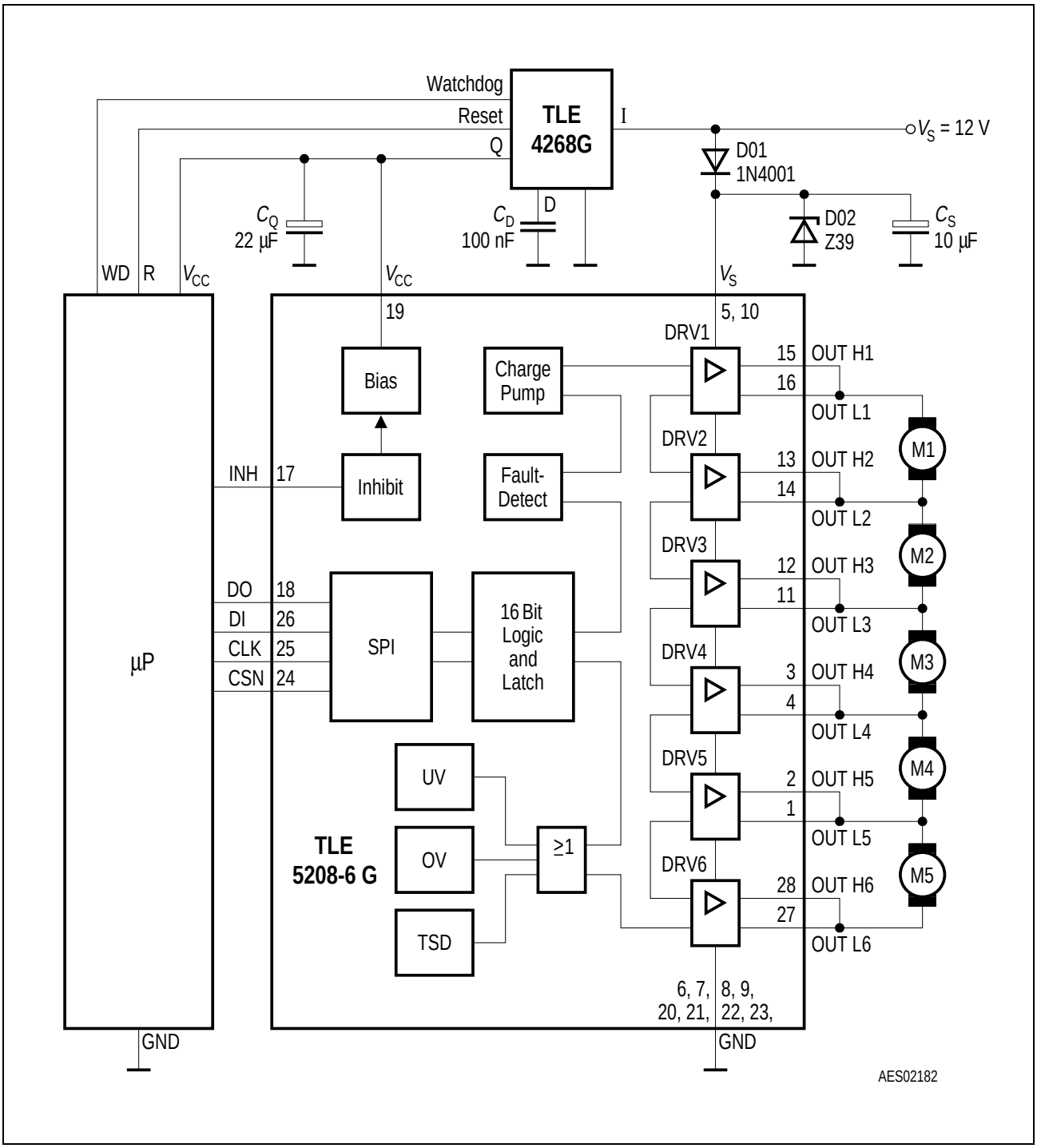


Figure 16 Application Circuit with TLE 5208-6 G and TLE 4268 G for Vehicle Air Conditioning

The SIEMENS low-drop voltage regulator **TLE 4268 G** can be used for the V_{CC} power supply. It has additional functions such as reset and watchdog for integrated controller management, and features excellent EMC stability. If this voltage regulator does not meet the application requirements, there is a wide range of different SIEMENS low-drop voltage regulators available.

The external configuration of the **TLE 5208-6 G** is extremely simple. Only one blocking capacitor C_S to V_S and one reverse-connection protected diode are required. The capacitor C_S has to store any reverse inductive energy, since the reverse-connection protected diode prevents the backflow to the power supply. For this reason C_S should not be too small.

If a Zener diode of e.g. 36 V is connected from V_S to GND then this rule no longer applies. C_S can be considerably smaller in this case (a few µF). The slew rate of the supply voltage dV_S/dt is now the determining parameter. C_S should be selected so that dV_S/dt remains clearly below 10 V/µs.

Another application for the **TLE 5208-6 G** could be in door control equipment. A single driver could be used to switch the two mirror motors, the window winder relay, and other loads with the remaining circuits (1 LS + 3 HS).

Multichannel light switches are often required in industrial electronics for large displays or power management functions with a large number of channels.

High power-on peak currents frequently occur in these applications. These may be up to an order of magnitude higher than the rated current. The TLE 5208-6 can switch load currents of up to 2 A per channel if the overcurrent lockout has been deactivated by setting Bit 13 to L. Once the power-on procedure has been completed, the overcurrent lockout can be reactivated via software control (Bit 13 to H), in order to protect the load (blocked motor etc.) and the IC against overload. If the current now rises above the cutoff threshold of typ. I_{SD} = 1.5 A during nominal operation, then the channel is disconnected after a dead time of typ. t_{dSD} = 50 µs. Figure 11 shows a typical cutoff process: Shortly after the CSN control signal changes from L to H, the OUTL1 output is switched to overload and disconnected after the time t_{dSD}.

The V_S operating voltage range can be extended up to 40 V by setting the overvoltage Bit 15 to L. This therefore satisfies all the main industrial requirements.

Application Board and Control Software

For the purposes of laboratory testing and as a development system, an application board is available with various loads switched by a TLE 5208-6 G, together with Windows® control software.

Application Board Configuration

- 2 motors in series
- 1 relay - slow commutating
- 1 relay - fast commutating (LS switch with Z-diode)
- A sub-application (5 V regulator TLE 5208-6 G) which can be switched by means of an HS switch on the TLE 5208-6 G
- A lighting load to demonstrate overcurrent programming
  For this lamps have been selected in a way that the TLE 5208-6 G can switch on just one lamp when overcurrent shut down is activated (OCSD-Bit 13 = H). By switching on the second lamp the overcurrent shut down is working. If the OCSD-Bit 13 is now set to ‘L’ the second lamp can be switched on too without any problem. After having performed this “inrush”, the overcurrent shut down can by again activated by seting the OCSD-bits
- An HS switch and an LS switch extending directly. An external load can be connected here for testing purposes.

Figure 16 shows the schematic circuit diagram and **Figure 18** shows the associated PCB for the application board.

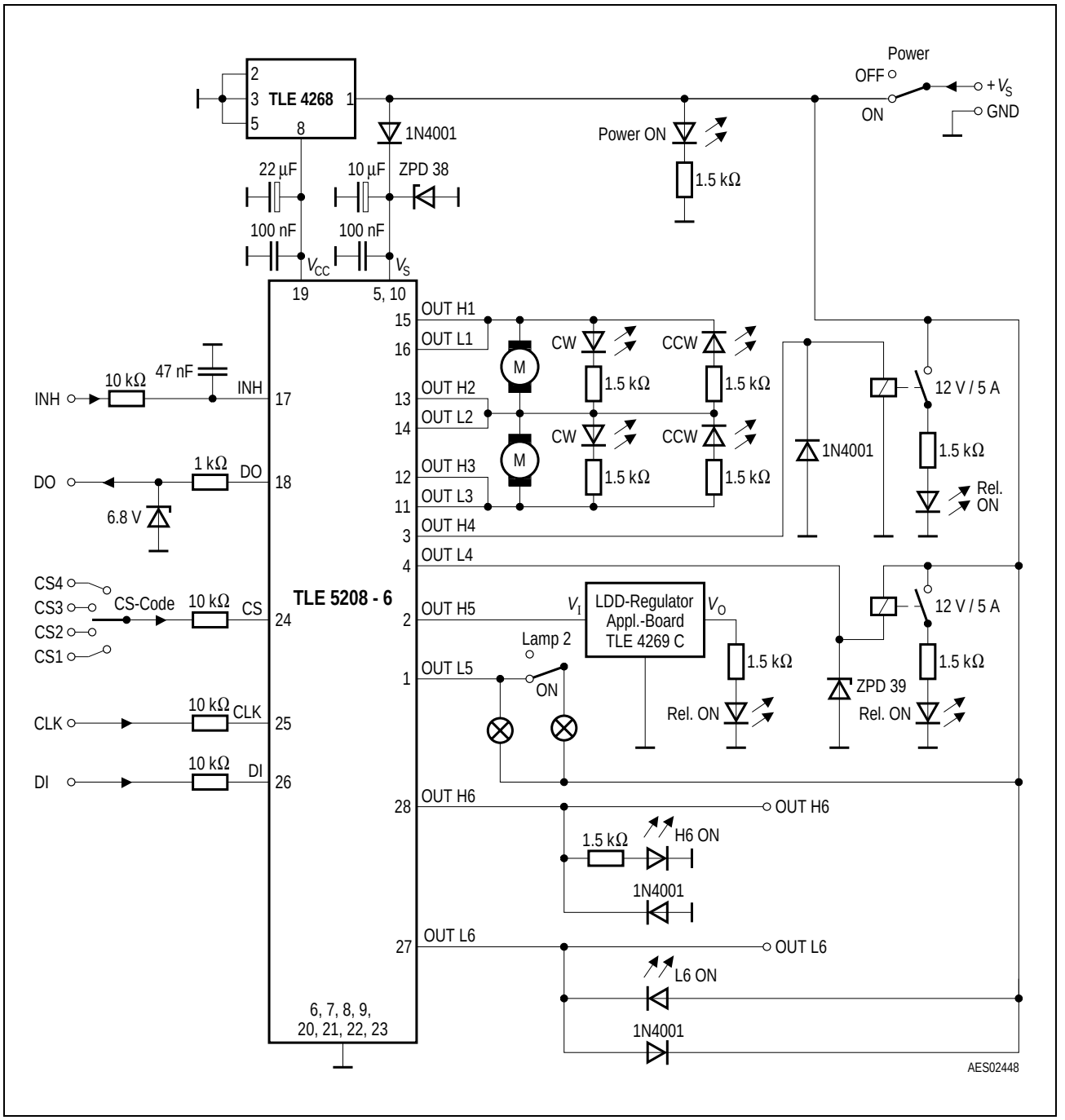


Figure 17 Schematic Circuit Diagram of the TLE 5208-6 Application Board

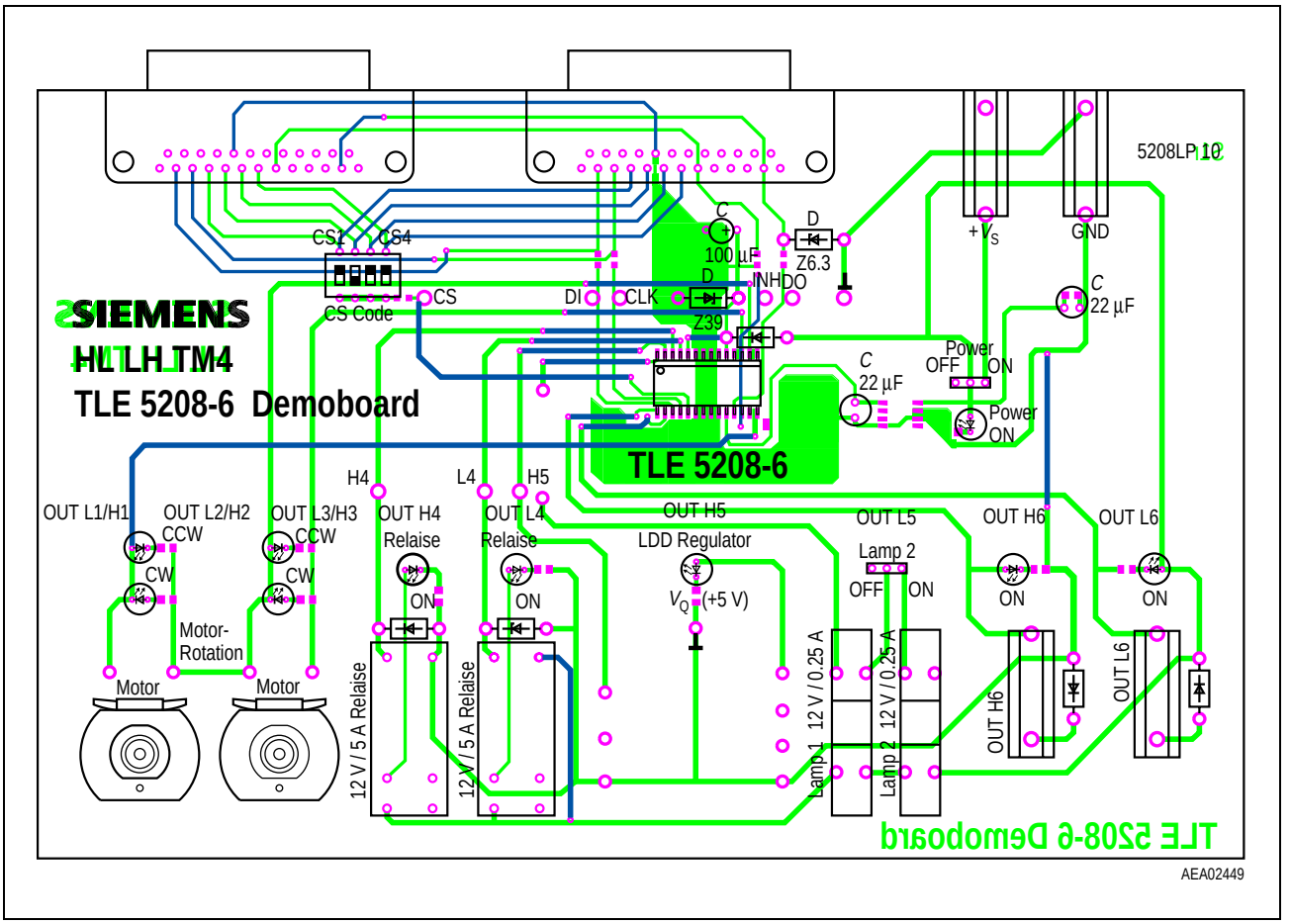


Figure 18 Layout of the TLE 5208-6 Application Board

The standard parallel interface on a PC is used to control and read the status word. Software running under Windows allows the simple definition of macros, which can be combined to create a sequence program. The standard screen masks are shown in **Figure 19**.

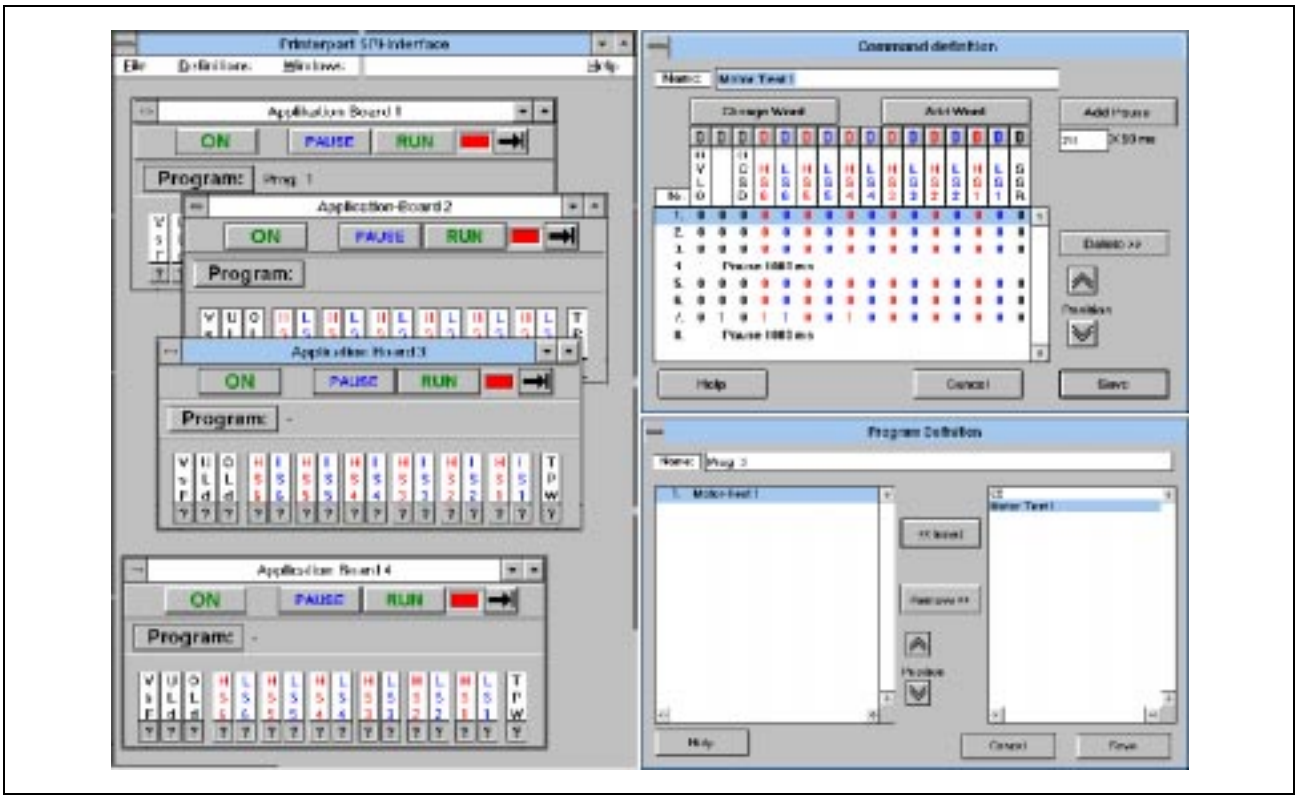


Figure 19 Standard Masks for the TLE 5208-6 G Control Software

The control software can address four boards via corresponding chip select lines. A small bus system can easily be constructed in this way.

The complete system can be disconnected via the INH button on the PC.

The only additional hardware required is a 12 V supply voltage and a standard PC with a printer interface. The documentation supplied with the application board contains lots of additional information to provide a better understanding of the IC. The application board and the control software can be obtained from SIEMENS sales offices.

Conclusion

The **TLE 5208-6 G** module has successfully bridged the gap between single switches and motor bridge applications.

The breakdown of the H bridge circuit into “quarter bridges”, i.e. individual low-side and high-side switches, was achieved for the first time with the high-current bridge driver IC **BTS 770/1** (**TrilithIC**), which is already in mass production. Today, this IC is often used in mixed switch/motor bridge applications. This is actually a multichip IC consisting of 3 chips (hence the name **TrilithIC**).

In contrast, the **TLE 5208-6 G** is a monolith, offering the only “double-six” combination of high-side and low-side switches in the world today.

This unique combination allows all possible loads to be controlled easily, and therefore sets a new standard in the field of power electronics.