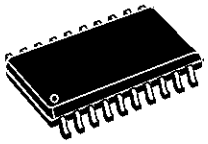
SGS-THOMSON MICROELECTRONICS

TEA7533

MONITOR AMPLIFIER

- 7 DIGITALLY PROGRAMMABLE GAINS IN STEPS OF 4.5dB
- ON/OFF POSITION
- LOW VOLTAGE (3.5V to 6.5V)
- POWER: >140mW at 5V; >250mW at 6.5V



SO20

ORDERING NUMBER: TEA7533FP

DESCRIPTION

This 20 pins IC is designed for monitoring and loudspeaker telephone set and provides:

a) signal amplification for monitoring (loudspeaker).
b) antiacoustic feedback (antilarsen).
c) antidistortion by automatic level adaptation.
d) antilarsen adjustment (full duplex).
e) antidistortion by automatic gain adaptation in current supply mode.
f) service audio inputs with internal dedicated switches.

FUNCTIONAL DESCRIPTION

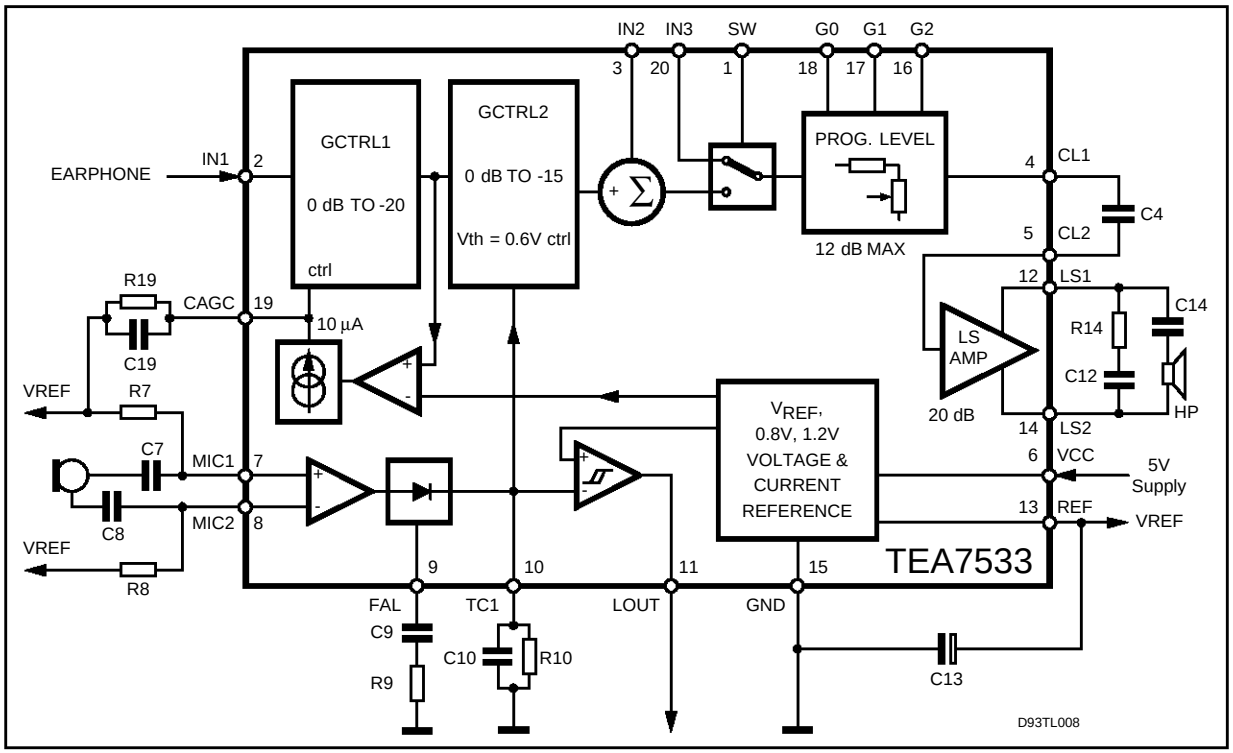
TEA7533 performs the following functions:

The circuit amplifies the incoming signal and feeds it to the loudspeaker. PG0, PG1 and PG2 inputs are used to set the loudspeaker gain in a range of 32dB to 5dB in 7 steps of 4.5dB.

The TEA7533 inputs (PG0, PG1, PG2) allows also the loudspeaker to be cut-off, thus ensuring privacy of communication.

- The antilarsen (antiacoustic feedback) system is incorporated.
- The maximum power available on a 50Ω impedance loudspeaker is 140mW at 5V and 250mW at 6.5V.

BLOCK DIAGRAM



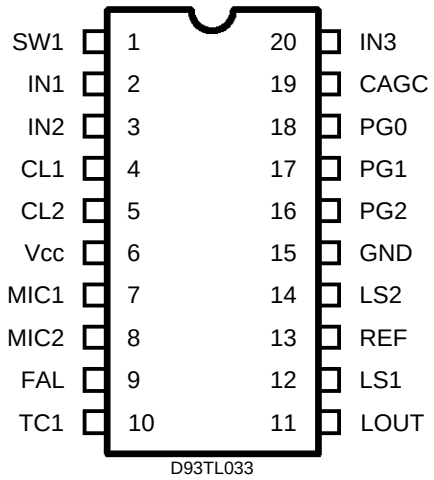
PIN DESCRIPTION

N°	Symbol	Description
1	SW	Switch control: IN2 or IN3
2	IN1	Audio Input AVG Controlled
3	IN2	2nd Audio input; No Anti-distortion Control
4	CL1	Intermediate Receive Output (Decoupling capacitor)
5	CL2	Intermediate Receive Input (Decoupling capacitor)
6	V_{CC}	Supply Voltage
7	MIC1	Microphone input 1
8	MIC2	Microphone input 2
9	FAL	Antilarsen Filter
10	TC1	Antilarsen Gain Set up
11	LOUT	Status Output, Digital Output.
12	LS1	Loudspeaker Output1
13	REF	Reference Voltage; (V_{CC} - 0.7V/2)
14	LS2	Loudspeaker Output2
15	GND	Ground
16	PG2	Digital Input; Loudspeaker Level Control
17	PG1	Digital Input; Loudspeaker Level Control
18	PG0	Digital Input; Loudspeaker Level Control
19	CAGC	Gain Control Filter Capacitor
20	IN3	3rd Audio Input

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
V_{CC}	Max. Supply Voltage	7	V
I_{CC}	Max Supply Current at t > 300ms at t ≤ 300ms	100 150	mA mA
V_{LOGIC}	Voltage Level (logic pins)	-0.6/V_{CC}+0.6	V
T_{op}	Operative Temperature Range	-20 to +70	°C
T_{stg}	Storage Temperature Range	-55 to +125	°C

PIN CONNECTION (Top view)



ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, R_{BIAS} = 60KΩ; V_{G0} = V_{G1} = V_{G2} = H; V_{in} = 0Vrms; V_{TG1} = 0V; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		3.5	5	6.5	V
I_{CC}	Supply Current	V_{CC} = 5V; PG0 = PG1 = PG2 = L V_{CC} = 5V; PG0 = PG1 = PG2 = H	– –	0.75 1.6	1 2.1	mA mA
V_{ref}	Voltage Reference	 V_{CC} = 5V	– 1.72	(V_{CC} - 0.7)/2 2.15	– 2.6	V
I_{ref}	Current Available at V_{ref}	Source Sink	– –	30 400	– –	µA µA
IN2 & IN3 AMPLIFIER SECTIONS						
G_O	Final Stage Gain (V_{LS1} - V_{LS2})/V_{CL2}		19	20	21	dB
G	Loudspeaker Amplifier Gain (V_{LS1} - V_{LS2})/IN3 (or IN2)	V_{TC1} = 0V; V_{IN} = 60mVrms V_{CAGL} = 0V				
		PG2, PG1, PG0				
G111	Gain max	H H H	30	31.5	33	dB
G110	Gain 1st step	H H L	25.5	27	28.5	dB
G101	Gain 2nd step	H L H	21	22.5	24	dB
G100	Gain 3rd step	H L L	16.5	18	19.5	dB
G011	Gain 4th step	L H H	12.0	13.5	15	dB
G010	Gain 5th step	L H L	7.5	9	10.5	dB
G001	Gain 6th step	L L H	3	4.5	6	dB
G000	Off step	L L L	-	-40	-30	dB
V_{OFF}	Output Offset	G = G111; R_{LOAD} = 50Ω	-50	-	50	mV
LS DIN	Loudspeaker Dinamic (V_{LS1}- V_{LS2})	R_{LOAD} = 50Ω V_{CC} = 3.5V; THD = 4% V_{CC} = 5V; THD = 4%	 4.5 6.5	 5 6.7	 - -	 Vpp Vpp
THD	Output Distortion	V_{CC} = 5V G = G111(32dB) SW = L; V_{OUT} = 2Vrms SW = H; V_{OUT} = 2Vrms	 - -	 - -	 2 2	 % %
IN1 AMPLIFIER SECTION						
G_1	Loudspeaker Amplifier Gain (V_{LS1} - V_{LS2}) / IN1	V_{CAG} (19) = V_{REF}; V_{TC1} = 0V V_{IN1} = 45mVrms	29.5	31.5	34.5	dB
THD1	Distortion	V_{IN} = 45mVrms	–	1	2	%
IN1 ANTIDISTORTION SECTION						
ALG1	Antilarsen Attenuation on IN1 Chain	V_{CAGC} = V_{REF}; V_{TC1} = 0.8V	–17	–15	–13	dB
ALTHD	Distortion with Antilarsen Active		–	4.5	6.0	%
CAGC THD	Distortion with AGC Control Active	V_{IN1} = 80mV V_{IN1} = 560mV	– –	– –	3 10	% %
PG	Logic Interface PG0, PG1, PG2, SW= L, IN3 = ON					
PGH	Logical Input High		0	-	0.4 x (V_{CC} - 0.7)	V
PGL	Logical Input Low		0.6 x (V_{CC} - 0.7)	-	V_{CC}	V
I_{PGL}	Input Current Low state	V_{IN} = 0V	-1	-	+1	µA
I_{PGH}	Input Current High State	V_{IN} = V_{CC}	-1	-	+1	µA
ANALOG INTERFACE						
I_{BIAS}	Biasing Current Analog Inputs	IN1, IN2, IN3, MIC1,MIC2	–	17	100	mA

ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
ANTILARSEN SECTION						
G_{MIC}	Microphone Amplifier Gain = $V_{FAL}/(V_{MIC1} - V_{MIC2})$	V_{IN} = 4.5mVrms; f = 5KHz	19.5	21	22.5	dB
$V_{TC1\,TH}$	TC1 Threshold for –3dB attenuation on IN1 chain		0.55	0.68	0.75	V
$V_{TC1\,LOW}$	TC1 Level with V_{mic} = 0 Vrms		0	0.07	0.2	V
TC1 H	High Thereshold of LOUT Comparator	V_{LOUT} < 0.4V	1.1	1.2	–	V
TC1 L	Low Thereshold of LOUT Comparator	V_{LOUT} > 4.1V	–	0.8	0.9	V
$I_{LOUT\,L}$	Output Current of Comparator LOUT	V_{TC1} = 1.5V; V_{LOUT} = 0.5V	5	20	–	µA
$I_{LOUT\,H}$		VTC1 = 0.6V; V_{LOUT} = 3.5V	–	–1	–0.5	µA
$V_{LOUT\,L}$	Output Voltage of Comparator LOUT	VTC1 = 1.5V	–	0.08	0.4	V
$V_{LOUT\,H}$		VTC1 = 0.6V	4.1	4.33	–	V

TEST CIRCUIT

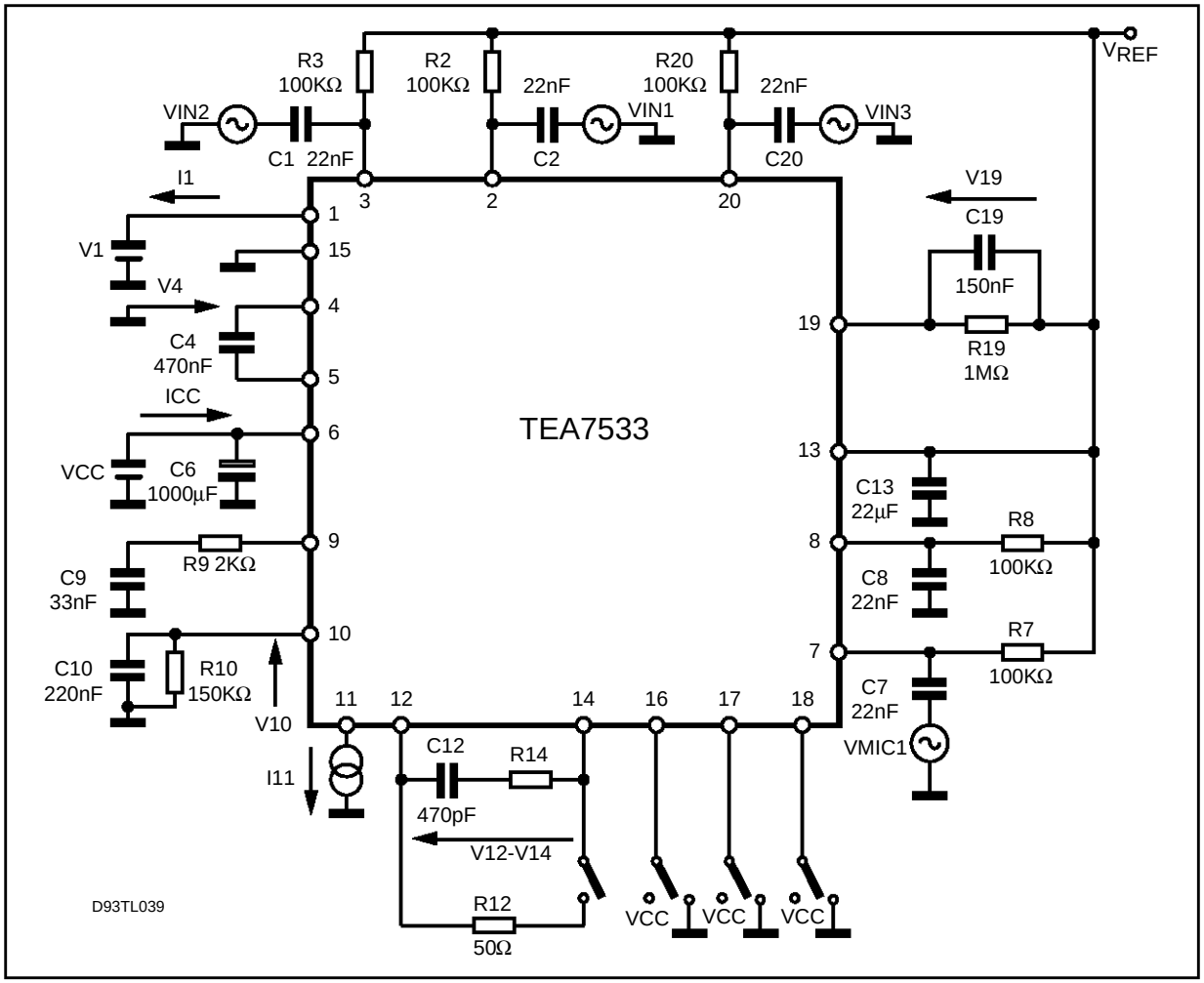


Figure 1: IN1 Channel - AGC Gain (Typical)

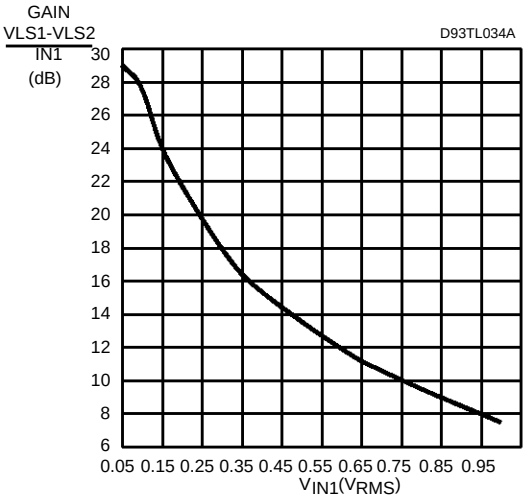


Figure 2: IN1 Channel ($V_{CAGC} – V_{REF}$)

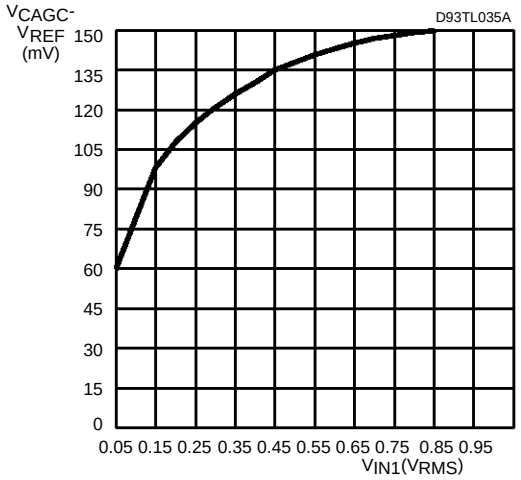


Figure 3: IN1 Channel – Distortion (Typical)

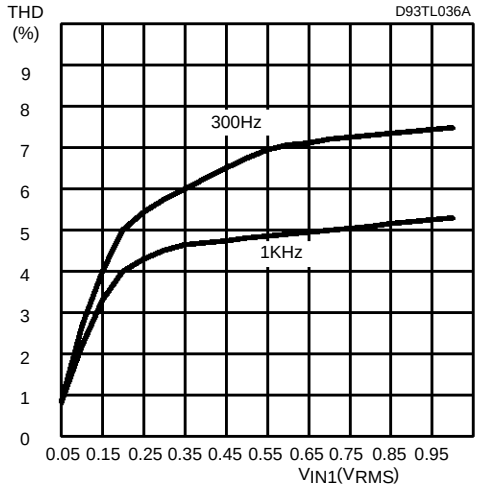


Figure 4: IN3 and IN2 Channels – Distortion

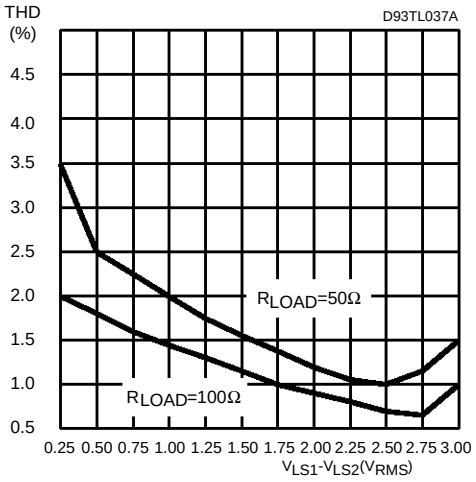
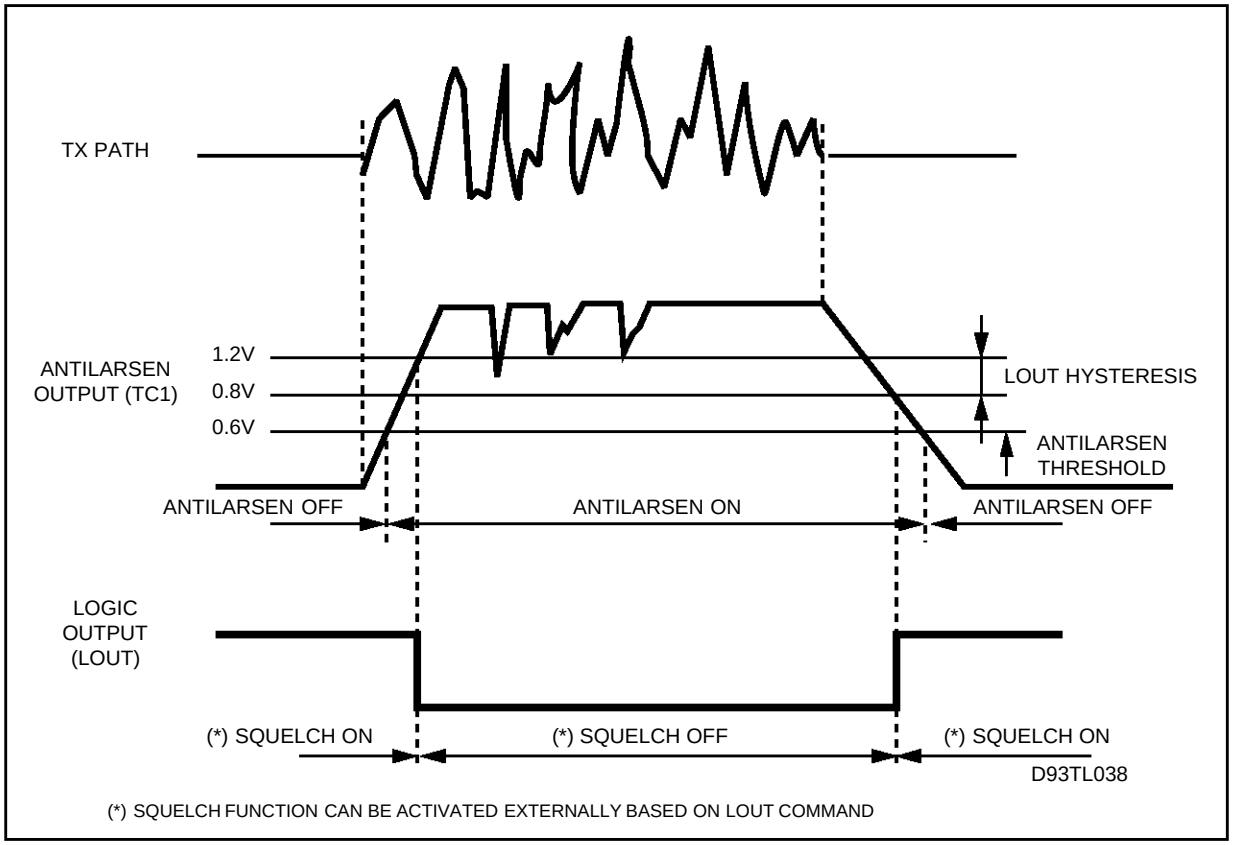


Figure 5: Time Diagram for TC1 (Antilarsen) and LOUT.



SO20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45^o (typ.)					
D	12.6		13.0	0.496		0.510
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.4		7.6	0.291		0.300
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8^o (max.)