Sound fader control circuit

TEA6320T

FEATURES

- Source selector for four stereo inputs and one mono input
- Interface for noise reduction circuits
- Interface for external equalizer
- Volume, balance and fader control
- Special loudness characteristic automatically controlled in combination with volume setting
- Bass and treble control
- Mute control at audio signal zero crossing
- Fast mute control via bus
- Fast mute control via pin
- I^2C-bus control for all functions
- Power supply with internal power-on reset

GENERAL DESCRIPTION

The sound fader control circuit TEA6320T is an I^2C-bus controlled stereo preamplifier for car radio hi-fi sound applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply voltage		7.5	8.5	9.5	V
I_{CC}	Supply current	V_{CC} = 8.5V	—	26	—	mA
$V_{o(RMS)}$	Maximal output voltage level	V_{CC} = 8.5V; THD ≤ 0.1%	—	2000	—	mV
G_V	Volume gain		-86	—	+20	dB
G_{step}	Step resolution (volume)		—	1	—	dB
G_b	Bass control		-15	—	+15	dB
G_t	Treble control		-12	—	+12	dB
G_{step}	Step resolution (bass, treble)		—	1.5	—	dB
(S+N)/N	Signal-plus-noise to noise ratio	V_O = 2.0V; G_V = 0dB; unweighted; RMS	—	105	—	dB
RR_{100}	Ripple rejection	$V_{r(RMS)}$ < 200mV; f = 100Hz; G_V = 0dB	—	75	—	dB
α_{cs}	Channel separation	250Hz ≤ f ≤ 10kHz; G_V = 0dB	90	96	—	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA6320T	32	SO	Plastic	SOT287

Sound fader control circuit — TEA6320T

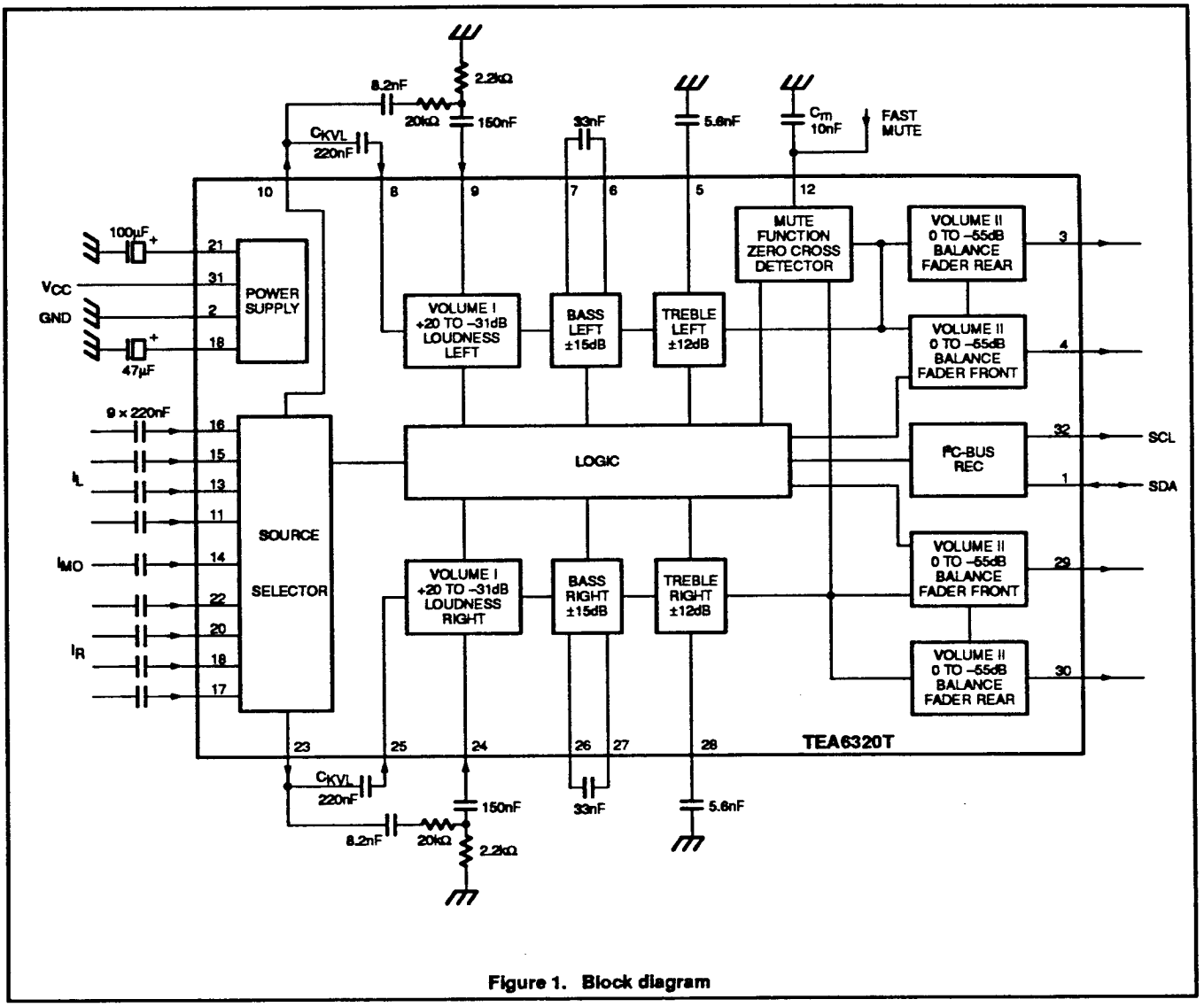


Figure 1. Block diagram

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	Serial data input/output
GND	2	Ground
OUTLR	3	Output left rear
OUTLF	4	Output left front
TL	5	Treble control capacitor left channel or input from an external equalizer
B2L	6	Bass control capacitor left channel or output to an external equalizer
B1L	7	Bass control capacitor, left channel
IVL	8	Input volume I, left control part
ILL	9	Input loudness, left control part
QSL	10	Output source selector, left channel
IDL	11	Input D left source
MUTE	12	Mute control
ICL	13	Input C left source
IMO	14	Input mono source
IBL	15	Input B left source
IAL	16	Input A left source
IAR	17	Input A right source
IBR	18	Input B right source
CAP	19	Electronic filtering for supply
ICR	20	Input C right source
V_{REF}	21	Reference voltage ($0.5V_{CC}$)
IDR	22	Input D right source
QSR	23	Output source selector right channel
ILR	24	Input loudness right channel
IVR	25	Input volume I, right channel
B1R	26	Bass control capacitor right channel
B2R	27	Bass control capacitor right channel or output to an external equalizer
TR	28	Treble control capacitor right channel or input from an external equalizer
OUTRF	29	Output right front
OUTRR	30	Output right rear
V_{CC}	31	Supply voltage
SCL	32	Serial clock input

PIN CONFIGURATION

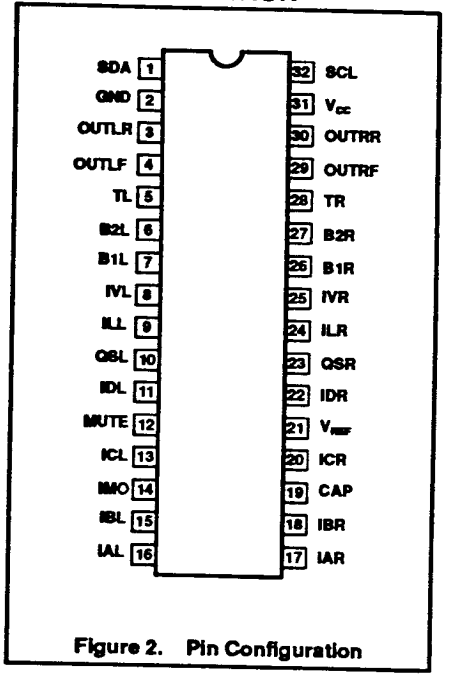


Figure 2. Pin Configuration

FUNCTIONAL DESCRIPTION

The source selector selects one of four stereo inputs or the mono input. The maximum input signal voltage is $V_{I(RMS)}$ = 2V. The outputs of the source selector and the inputs of the following volume control parts are available at pins. This offers the possibility of interfacing a noise reduction system.

The volume control function is split into two sections: volume I control block and volume II control block.

The control range of volume I is between +20dB and -31dB in steps of 1dB. The volume II control range is between 0dB and -55dB in steps of 1dB. Although the theoretical possible control range is 106dB (+20dB to -86dB), in practice a range of 86dB (+20dB to -66dB) is recommended. The gain/attenuation setting of the volume I control blocks is common for both channels.

The volume I control blocks work in combination with the loudness control. The filter is linear when the maximum gain for the volume I control (+20dB) is selected. The filter characteristic increases automatically over a range of 32dB down to a setting of -12dB. That means the maximum filter characteristic is obtained at -12dB setting of volume I. Further reduction of the volume does not further influence the filter characteristic (see Figure 5). The maximum selected filter characteristic is determined by external components. The proposed application gives a maximum boost of 17dB for bass and 4.5dB for treble. The loudness may be switched on or off via I²C bus control (Table 7).

The volume I control block is followed by the bass control block. A single external capacitor of 33nF for each channel in combination with internal resistors, provides the frequency response of the bass control (see Figure 3). The adjustable range is between -15dB and +15dB in steps of 1.5dB at 40Hz.

Both loudness and bass control result in a maximum bass boost of 32dB for low volume settings.

The treble control block offers a control range between -12dB and +12dB in steps of 1.5dB at 15kHz. The filter characteristic is determined by a single capacitor of 5.6nF for each channel in combination with internal resistors (see Figure 4).

The basic step width of bass and treble control is 3dB. The intermediate steps are obtained by switching 1.5dB boost and 1.5dB attenuation steps.

The bass and treble control functions can be switched off via the I²C bus. In this case the internal signal flow is disconnected. The connections B2L/B2R are outputs and TL/TR are inputs for inserting an external equalizer.

The last section of the circuit is the volume II block. The balance and fader functions are performed using the same control blocks. This is realized by four independently controllable attenuators, one for each output. The control range of these attenuators is 55B in steps of 1dB with an additional mute step.

The circuit provides three mute modes.

1. Zero crossing mode mute via bus using two independent zero crossing detectors (ZCM, see Tables 2 and 9 and Figure 14).
2. Fast mute via mute pin (see Figure 8).
3. Fast mute via bus either by general mute (GMU see Tables 2 and 9) or volume II block setting (see Table 4).

The mute function is performed immediately if ZCM is cleared (ZCM=0). If the bit is set (ZCM=1) the mute is activated after changing the GMU bit. The actual mute switching is delayed until the next zero crossing of the audio frequency signal. As the two audio channels (left and right) are independent, two comparators (window detectors) are required to control independent mute switches.

For avoiding a large delay of the muting switching when very low frequencies are processed, the maximum delay time is limited to typically 100ms by an integrated timing circuit and an external capacitor (C_m=10nF, see Figure 8). This timing circuit is triggered by reception of a new data word for the switch function which includes the GMU bit. After a discharge and charge period of an external capacitor the muting switch follows the GMU bit if no zero crossing was detected during that time.

The mute function can also be controlled externally. If the mute pin is switched to ground all outputs are muted immediately (hardware mute). This mute request overwrites all mute controls via the I²C bus for the time the pin is held low.

For the turn on/off behavior the following explanation is generally valid. To avoid AF-output caused by the input signal coming from preceding stages, which produce output during drop of V_{CC}. The mute has to be set, before the V_{CC} will drop. This can be achieved by I²C bus control or by grounding the mute pin.

The power supply should include a V_{CC} buffer capacitor, which provides a discharging time constant. In case the input signal does not disappear after turn off the input will become audible after a certain time. A 4.7kΩ resistor discharges the V_{CC} buffer capacitor, because the internal current of the IC does not discharge it completely.

The hardware mute position is not stored in the TEA6320T. The hardware mute function is favorable for use in RDS (Radio Data System) applications. The zero crossing mute avoids modulation plops. This feature is an advantage for mute during changing presets and/or sources (e.g., traffic announcement during cassette playback).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	Supply voltage		0	10	V
T_{amb}	Operating ambient temperature range		-40	+85	°C
T_{stg}	Storage temperature range		-65	+150	°C
V_{es}	Electrostatic handling	See note 1.			
V_{pin}	Voltage at pins: pin 1 to 2 and 3-32 to 2		0	V_{CC}	V

NOTES TO THE LIMITING VALUES TABLE:

1. Human body model: C = 100pF; R = 1.5kΩ; V ≥ 2kV.
   Charge device model: C = 200pF; R = 0Ω; V ≥ 500V.

CHARACTERISTICS

V_{CC} = 8.5V; R_S = 600Ω, R_L = 10kΩ, C_L = 2.5nF, AC coupled; f = 1kHz; T_{amb} = +25°C; gain control G_V = 0dB; bass linear; treble linear; fader off; balance in mid-position; loudness off; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply voltage		7.5	8.5	9.5	V
I_{CC}	Supply current		—	26	33	mA
V_{DC}	Internal DC voltage at inputs and outputs		3.83	4.25	4.68	V
V_{REF}	Internal reference voltage at pin 21		—	4.25	—	V
G_V	Maximum voltage gain	R_S = 0Ω; R_L = ∞	19	20	21	dB
$V_{o(RMS)}$	Output voltage level for P_{max} at the power output stage	THD ≤ 0.1%; See Figure 9	—	2000	—	mV
	For start of clipping	THD = 1%	2300	—	—	mV
		R_L = 2kΩ; C_L = 10nF; THD = 1%	2000	—	—	mV
$V_{i(RMS)}$	Input sensitivity	V_O = 2000mV; G_V = 20dB	—	200	—	mV
B	Roll-off frequencies	C_{KIN} = 220nF; C_{KVL} = 220nF; $Z_i = Z_{i\,min}$				
		Low frequency (-1dB)	60	—	—	Hz
		Low frequency (-3dB)	30	—	—	Hz
		High frequency (-1dB)	20000	—	—	Hz
		C_{KIN} = 470nF; C_{KVL} = 100nF; $Z_i = Z_{i\,typ}$				
		Low frequency (-3dB)	17	—	—	Hz
α_{cs}	Channel separation	V_i = 2V; frequency range 250Hz to 10kHz	90	96	—	dB
THD	Total harmonic distortion	Frequency range 20Hz to 12.5kHz				
		V_i = 100mV; G_V = 20dB	—	0.1	—	%
		V_i = 1000mV; G_V = 0dB	—	0.05	tbn	%
		V_i = 2000mV; G_V = 0dB	—	0.1	—	%
		V_i = 2000mV; G_V = -10dB	—	0.1	—	%
RR	Ripple rejection	$V_{r(RMS)}$ < 200mV				
		f = 100Hz	tbn	76	—	dB
		f = 40Hz to 12.5kHz	—	66	—	dB
(S+N)/N	Signal-plus-noise to noise ratio (see Figure 5)	unweighted; 20Hz to 20kHz RMS; V_O=2.0V	—	105	—	dB
		CCIR 468-2 weighted; quasi peak; V_O=2.0V				
		G_V = 0dB	—	95	—	dB
		G_V = 12dB	—	88	—	dB
		G_V = 20dB	—	81	—	dB
$P_{no(RMS)}$	Noise output power only contribution of TEA6320T; power amplifier for 6W	Mute position; Note 1	—	—	10	nW
α_B	Crosstalk (20 log $V_{bus(p-p)}$ / $V_{O(RMS)}$) between bus inputs and signal outputs	Note 2	—	110	—	dB
Source Selector						
Z_i	Input impedance		25	35	45	kΩ
α_S	Input isolation of one selected source to any other input	f = 1kHz	—	105	—	dB
		f = 12.5kHz	—	95	—	dB
$V_{i(RMS)}$	Maximum input voltage (RMS value)	THD < 0.5%; V_{CC} = 8.5V	—	2.15	—	V
		THD < 0.5%; V_{CC} = 7.5V	—	1.8	—	V
$V_{DC\,OFF}$	DC offset voltage at source selector out by selection of any inputs		—	—	10	mV
Z_O	Output impedance		—	80	120	Ω

CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Source Selector (continued)						
R_L	Output load resistance		10	—	—	kΩ
C_L	Output load capacity		0	—	2500	pF
G_V	Voltage gain, source selector		—	0	—	dB
Control Part (source selector disconnected; source resistance 600Ω)						
Z_I	Input impedance volume input		100	150	200	kΩ
	Input impedance loudness input		25	33	40	kΩ
Z_O	Output impedance		—	80	120	Ω
R_L	Output load resistance		2	—	—	kΩ
C_L	Output load capacity		0	—	10	nF
$V_{I(RMS)}$	Maximum input voltage	THD < 0.5%	—	2.15	—	V
V_{no}	Noise output voltage	CCIR 468-2 weighted; quasi peak				
		G_V = 20dB	—	110	220	µV
		G_V = 0dB	—	33	50	µV
		G_V = -66dB	—	13	22	µV
		Mute position	—	10	—	µV
G_C	Total continuous control range		—	106	—	dB
	Recommended control range		—	86	—	dB
G_{step}	Step resolution		—	1	—	dB
	Step error between any adjoining step		—	—	0.5	dB
ΔG_a	Attenuator set error	G_V = +20 to -50dB	—	—	2	dB
		G_V = -51 to -66dB	—	—	3	dB
ΔG_t	Gain tracking error	G_V = +20 to -50dB	—	—	2	dB
α_m	Mute attenuation	See Figure 8.	100	110	—	dB
$V_{DC\ OFF}$	DC step offset between any adjoining step	G_V = 0 to -66dB	—	0.2	10	mV
		G_V = 20 to 0dB	—	tbn	15	mV
	Between any step to mute	G_V = 0 to -66dB	—	—	10	mV
Volume / Control and Loudness						
G_C	Continuous volume control range		—	51	—	dB
G_V	Volume gain		-31	—	20	dB
G_{step}	Step resolution		—	1	—	dB
L_B	Maximum loudness boost	Loudness on; referred to loudness off; boost is determined by external components				
		f = 40Hz	—	17	—	dB
		f = 10kHz	—	4.5	—	dB
Bass Control						
G_b	Bass control, maximum boost	f = 40Hz	14	15	16	dB
	Maximum attenuation	f = 40Hz	14	15	16	dB
G_{step}	Step resolution (toggle switching)	f = 40Hz	—	1.5	—	dB
	Step error between any adjoining step	f = 40Hz	—	—	0.5	dB
$V_{DC\ OFF}$	DC step offset in any bass position		—	—	20	mV

CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Treble Control						
G_t	Treble control, maximum boost	f = 15kHz	11	12	13	dB
	Maximum attenuation	f = 15kHz	11	12	13	dB
	Maximum boost	f > 15kHz	—	—	15	dB
G_{step}	Step resolution (toggle switching)	f = 15kHz	—	1.5	—	dB
	Step error between any adjoining step	f = 15kHz	—	—	0.5	dB
$V_{DC\ OFF}$	DC step offset in any treble position		—	—	10	mV
Volume II, Balance- and Fader Control						
G_t	Continuous attenuation fader and volume control range		53.5	55	56.5	dB
G_{step}	Step resolution		—	1	2	dB
	Attenuation set error		—	—	1.5	dB
Mute Function (see Figure 8)						
a) Hardware Mute						
V_{SW}	Mute switch level ($2 \times V_{BE}$)		—	1.45	—	V
	Mute active:					
$V_{SW\ LOW}$	Input level		—	—	1.0	V
I_{CH}	Input current	$V_{SW\ LOW}$ = 1V	-300	—	—	µA
	Mute passive: level internally defined					
$V_{SW\ HIGH}$	Saturation voltage		—	—	V_{CC}	V
t_{DMU}	Delay until mute passive		—	—	0.5	ms
a) Zero Crossing Mute						
I_D	Discharge current		0.3	0.6	1.2	µA
I_{CH}	Charge current		-300	-150	—	µA
V_{SWDEL}	Delay switch level ($3 \times V_{BE}$)		—	2.2	—	V
t_{DEV}	Delay time	C_m = 10nF	—	100	—	ms
V_{WIND}	Window for audio signal zero crossing detection		—	30	40	mV
Muting at Power Supply Drop						
$V_{CC-DROP}$	Supply drop for mute active		—	V_{19}-0.7	—	V
Power On Reset (when reset is active the GMU bit – general mute – is set and the I²C bus receiver is in reset position)						
V_{CC}	Increasing supply voltage start of reset		—	—	2.5	V
	End of reset		5.2	6.0	6.8	V
	Decreasing supply voltage start of reset		4.2	5.0	5.8	V
Digital Part						
	I²C Bus terminals; See note 3.					
V_{IH}	Input voltage HIGH		3	—	9.5	V
V_{IL}	Input voltage LOW		-0.3	—	+1.5	V
I_{IH}	Input current HIGH		-10	—	+10	µA
I_{IL}	Input current LOW		-10	—	+10	µA
V_{OL}	Output voltage LOW	I_L = 3mA	—	—	0.4	V

NOTES TO THE CHARACTERISTICS TABLE:

1. The indicated values for output power assume a 6W power amplifier at 4Ω with 20dB gain and a fixed attenuator of 12dB in front of it. Signal-to-noise ratios exclude noise contribution of the power amplifier.
2. The transmission contains: total initialization with MAD and Subaddress for volume and 8 data words, see also definition of characteristics, clock frequency = 50kHz, repetition burst rate = 400Hz, maximum bus signal amplitude = $5V_{p-p}$.
3. The AC characteristics are in accordance with the I²C bus specification. Full specification of the I²C bus will be supplied on request.

I²C BUS PROTOCOL

I²C Bus Format

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA	A	P

S = Start condition
SLAVE ADDRESS (MAD) = 1000 0000
A = Acknowledge, generated by the slave
SUBADDRESS (SAD) = See Table 1
DATA = See Table 1
P = STOP condition

If more than one byte of DATA is transmitted, then auto-increment of the significant subaddress is performed.

Subaddress

Table 1. Second byte after MAD

FUNCTION		MSB 7	6	5	4	3	2	1	LSB 0
Volume/Loudness	V	0	0	0	0	0	0	0	0
Fader front right	FFR	0	0	0	0	0	0	0	1
Fader front left	FFL	0	0	0	0	0	0	1	0
Fader rear right	FRR	0	0	0	0	0	0	1	1
Fader rear left	FRL	0	0	0	0	0	1	0	0
Bass	BA	0	0	0	0	0	1	0	1
Treble	TR	0	0	0	0	0	1	1	0
Switch	S	0	0	0	0	0	1	1	1
							significant subaddress		

Definition of Third Byte

Table 2. Third byte after MAD and SAD

FUNCTION		MSB 7	6	5	4	3	2	1	LSB 0
Volume/Loudness	V	ZCM	LOFF	V5	V4	V3	V2	V1	V0
Fader front right	FFR	X	X	FFR5	FFR4	FFR3	FFR2	FFR1	FFR0
Fader front left	FFL	X	X	FFL5	FFL4	FFL3	FFL2	FFL1	FFL0
Fader rear right	FRR	X	X	FRR5	FRR4	FRR3	FRR2	FRR1	FRR0
Fader rear left	FRL	X	X	FRL5	FRL4	FRL3	FRL2	FRL1	FRL0
Bass	BA	X	X	X	BA4	BA3	BA2	BA1	BA0
Treble	TR	X	X	X	TR4	TR3	TR2	TR1	TR0
Switch	S	GMU	X	X	X	X	SC2	SC1	SC0

Function of the bits:

V0 to V5	Volume control
LOFF	Switch loudness on/off
FRR0 to FRR5	Fader control front right
FFL0 to FFL5	Fader control front left
FRR0 to FRR5	Fader control rear right
FRL0 TO FRL5	Fader control rear left
BA0 to BA4	Bass control
TR0 to TR4	Treble control
SC0 to SC2	Source selector control
GMU	Mute control for all outputs (general mute)
ZCM	Zero crossing mode
X	don't care bits (logic 1 during testing)

Table 3. Volume Setting

GV (dB)	DATA V5	V4	V3	V2	V1	V0
20	1	1	1	1	1	1
19	1	1	1	1	1	0
18	1	1	1	1	0	1
17	1	1	1	1	0	0
16	1	1	1	0	1	1
15	1	1	1	0	1	0
14	1	1	1	0	0	1
13	1	1	1	0	0	0
12	1	1	0	1	1	1
11	1	1	0	1	1	0
10	1	1	0	1	0	1
9	1	1	0	1	0	0
8	1	1	0	0	1	1
7	1	1	0	0	1	0
6	1	1	0	0	0	1
5	1	1	0	0	0	0
4	1	0	1	1	1	1
3	1	0	1	1	1	0
2	1	0	1	1	0	1
1	1	0	1	1	0	0
0	1	0	1	0	1	1
-1	1	0	1	0	1	0
-2	1	0	1	0	0	1
-3	1	0	1	0	0	0
-4	1	0	0	1	1	1
-5	1	0	0	1	1	0
-6	1	0	0	1	0	1
-7	1	0	0	1	0	0
-8	1	0	0	0	1	1
-9	1	0	0	0	1	0
-10	1	0	0	0	0	1
-11	1	0	0	0	0	0

Loudness on: the increment of the loudness characteristic is linear at every volume step in the range from +20dB to −11dB.

Table 3. Volume Setting (continued)

GV (dB)	DATA V5	V4	V3	V2	V1	V0
-12	0	1	1	1	1	1
-13	0	1	1	1	1	0
-14	0	1	1	1	0	1
-15	0	1	1	1	0	0
-16	0	1	1	0	1	1
-17	0	1	1	0	1	0
-18	0	1	1	0	0	1
-19	0	1	1	0	0	0
-20	0	1	0	1	1	1
-21	0	1	0	1	1	0
-22	0	1	0	1	0	1
-23	0	1	0	1	0	0
-24	0	1	0	0	1	1
-25	0	1	0	0	1	0
-26	0	1	0	0	0	1
-27	0	1	0	0	0	0
-28	0	0	1	1	1	1
-29	0	0	1	1	1	0
-30	0	0	1	1	0	1
-31	0	0	1	1	0	0

Loudness characteristic is constant in the range from -11dB to -31dB.

Table 3. Volume Setting (continued)

GV (dB)	DATA V5	V4	V3	V2	V1	V0
-28	0	0	1	0	1	1
⋮				⋮		
-31	0	0	0	0	0	0

Table 4. Fader Setting

GV (dB)	DATA FRR5 FRL5 FFL5 FFR5	FRR4 FRL4 FFL4 FFR4	FRR3 FRL3 FFL3 FFR3	FRR2 FRL2 FFL2 FFR2	FRR1 FRL1 FFL1 FFR1	FRR0 FRL0 FFL0 FFR0
0	1	1	1	1	1	1
-1	1	1	1	1	1	0
-2	1	1	1	1	0	1
-3	1	1	1	1	0	0
-4	1	1	1	0	1	1
-5	1	1	1	0	1	0
-6	1	1	1	0	0	1
-7	1	1	1	0	0	0
-8	1	1	0	1	1	1
-9	1	1	0	1	1	0
-10	1	1	0	1	0	1
-11	1	1	0	1	0	0
-12	1	1	0	0	1	1
-13	1	1	0	0	1	0
-14	1	1	0	0	0	1
-15	1	1	0	0	0	0
-16	1	0	1	1	1	1
-17	1	0	1	1	1	0
-18	1	0	1	1	0	1
-19	1	0	1	1	0	0
-20	1	0	1	0	1	1
-21	1	0	1	0	1	0
-22	1	0	1	0	0	1
-23	1	0	1	0	0	0
-24	1	0	0	1	1	1
-25	1	0	0	1	1	0
-26	1	0	0	1	0	1
-27	1	0	0	1	0	0
-28	1	0	0	0	1	1
-29	1	0	0	0	1	0
-30	1	0	0	0	0	1
-31	1	0	0	0	0	0
-32	0	1	1	1	1	1
-33	0	1	1	1	1	0
-34	0	1	1	1	0	1
-35	0	1	1	1	0	0
-36	0	1	1	0	1	1
-37	0	1	1	0	1	0
-38	0	1	1	0	0	1

Table 4. Fader Setting (continued)

GV (dB)	DATA FRR5 FRL5 FFL5 FFR5	FRR4 FRL4 FFL4 FFR4	FRR3 FRL3 FFL3 FFR3	FRR2 FRL2 FFL2 FFR2	FRR1 FRL1 FFL1 FFR1	FRR0 FRL0 FFL0 FFR0
-39	0	1	1	0	0	0
-40	0	1	0	1	1	1
-41	0	1	0	1	1	0
-42	0	1	0	1	0	1
-43	0	1	0	1	0	0
-44	0	1	0	0	1	0
-45	0	1	0	0	1	0
-46	0	1	0	0	0	1
-47	0	1	0	0	0	0
-48	0	0	1	1	1	1
-49	0	0	1	1	1	0
-50	0	0	1	1	0	1
-51	0	0	1	1	0	0
-52	0	0	1	0	1	1
-53	0	0	1	0	1	0
-54	0	0	1	0	0	1
-55	0	0	1	0	0	0
Mute	0	0	0	1	1	1
Mute	0	0	0	1	1	0
Mute	0	0	0	1	0	1
Mute	0	0	0	1	0	0
Mute	0	0	0	0	1	1
Mute	0	0	0	0	1	0
Mute	0	0	0	0	0	1
Mute	0	0	0	0	0	0

For a particular range the data are always the same, only the subaddress changes.

Table 5. Bass Setting

GV (dB)	DATA BA4	BA3	BA2	BA1	BA0
15	1	1	1	1	1
13.5	1	1	1	1	0
15	1	1	1	0	1
13.5	1	1	1	0	0
15	1	1	0	1	1
13.5	1	1	0	1	0
12	1	1	0	0	1
10.5	1	1	0	0	0
9	1	0	1	1	1
7.5	1	0	1	1	0
6	1	0	1	0	1
4.5	1	0	1	0	0
3	1	0	0	1	1
1.5	1	0	0	1	0
0 *	1	0	0	0	1
0 **	1	0	0	0	0
-1.5	0	1	1	1	1
-3	0	1	1	1	0
-4.5	0	1	1	0	1
-6	0	1	1	0	0
-7.5	0	1	0	1	1
-9	0	1	0	1	0
-10.5	0	1	0	0	1
-12	0	1	0	0	0
-13.5	0	0	1	1	1
-15	0	0	1	1	0
-13.5	0	0	1	0	1
-15	0	0	1	0	0
***	0	0	0	1	1
***	0	0	0	1	0
***	0	0	0	0	1
*** ****	0	0	0	0	0

* Recommended data word for step 0dB.
** Result of 1.5dB boost and 1.5dB attenuation.
*** The last four bass control data words mute the bass response.
**** The last bass control and treble control data words (00000) enable the external equalizer connection.

Table 6. Treble Setting

GV (dB)	DATA TR4	TR3	TR2	TR1	TR0
12	1	1	1	1	1
10.5	1	1	1	1	0
12	1	1	1	0	1
10.5	1	1	1	0	0
12	1	1	0	1	1
10.5	1	1	0	1	0
12	1	1	0	0	1
10.5	1	1	0	0	0
9	1	0	1	1	1
7.5	1	0	1	1	0
6	1	0	1	0	1
4.5	1	0	1	0	0
3	1	0	0	1	1
1.5	1	0	0	1	0
0 *	1	0	0	0	1
0 **	1	0	0	0	0
-1.5	0	1	1	1	1
-3	0	1	1	1	0
-4.5	0	1	1	0	1
-6	0	1	1	0	0
-7.5	0	1	0	1	1
-9	0	1	0	1	0
-10.5	0	1	0	0	1
-12	0	1	0	0	0
***	0	0	1	1	1
***	0	0	1	1	0
***	0	0	1	0	1
***	0	0	1	0	0
***	0	0	0	1	1
***	0	0	0	1	0
***	0	0	0	0	1
*** ****	0	0	0	0	0

* Recommended data word for step 0dB.

** Result of 1.5dB boost and 1.5dB attenuation.

*** The last eight treble control data words select treble cut.

**** The last treble control and bass control data words (00000) enable the external equalizer connection.

Table 7. Loudness Setting

CHARACTERISTIC	DATA LOFF
With loudness	0
Linear	1

Table 8. Selected Inputs

INPUTS	DATA SC2	SC1	SC0
IAL, IAR Stereo	1	1	1
IBL, IBR Stereo	1	1	0
ICC, ICR Stereo	1	0	1
IDL, IDR Stereo	1	0	0
IMO, Mono	0	X	X

Table 9. Mute Mode

GMU	ZCM	MODE
0	0	Direct mute off
0	1	Mute off delayed until the next zero crossing
1	0	Direct mute
1	1	Mute delayed until the next zero crossing

X = don't care bits (logic 1 during testing)

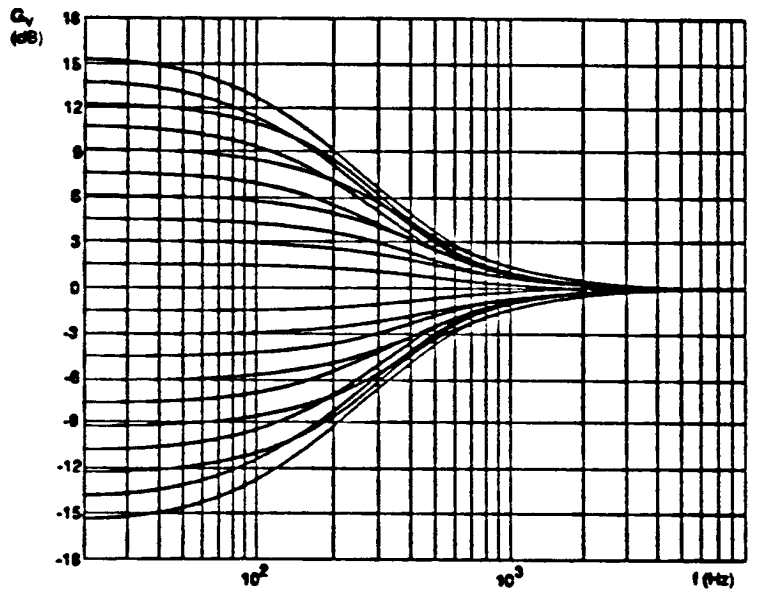


Figure 3. Bass control

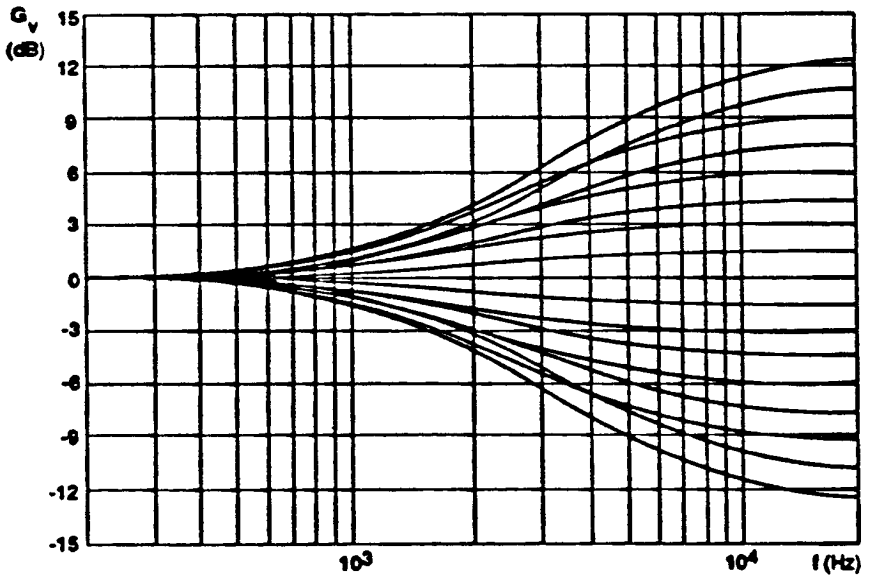


Figure 4. Treble control

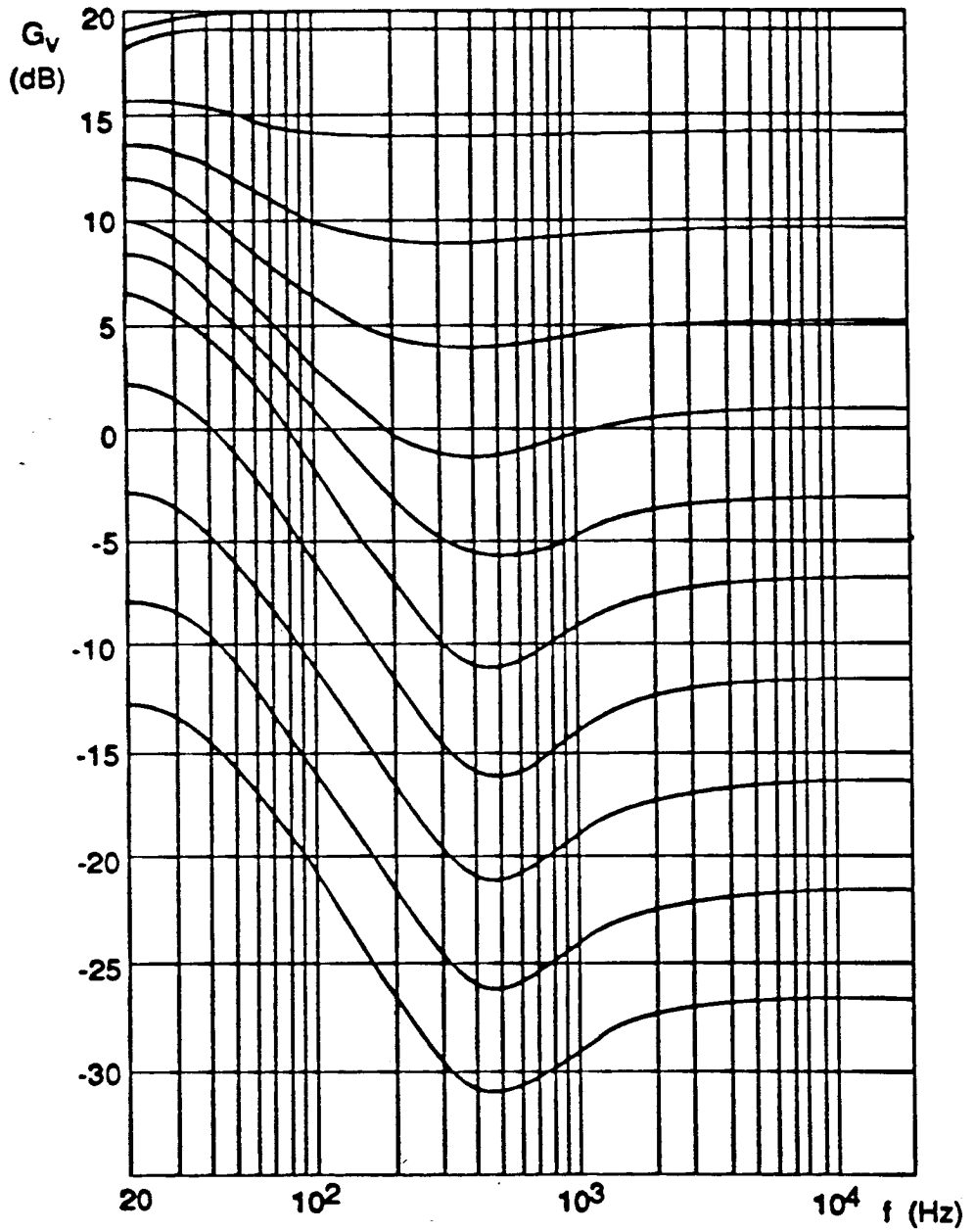


Figure 5. Volume control with loudness (including low roll-off frequency)

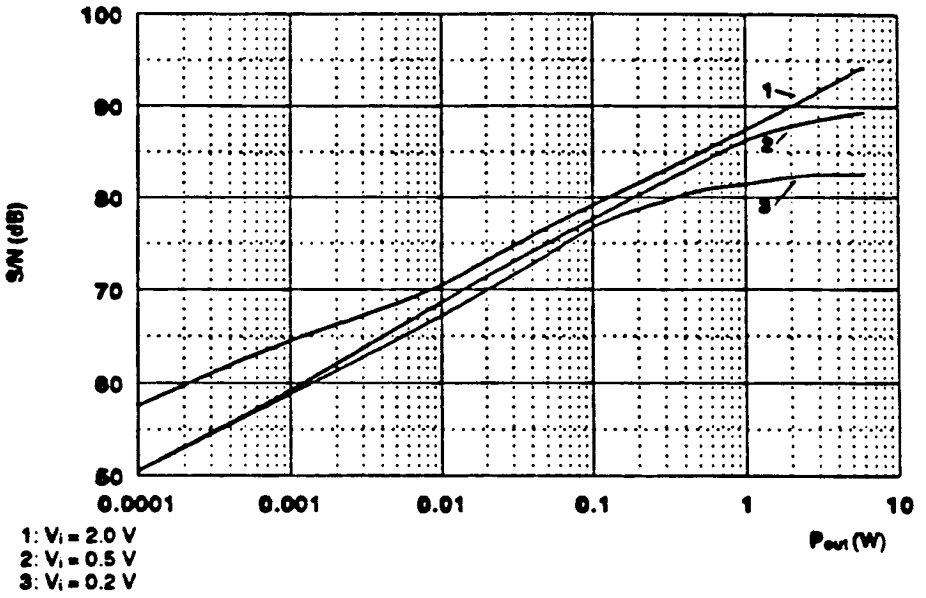


Figure 6a. Signal-to-noise ratio; noise weighted; CCIR468-2, quasi peak

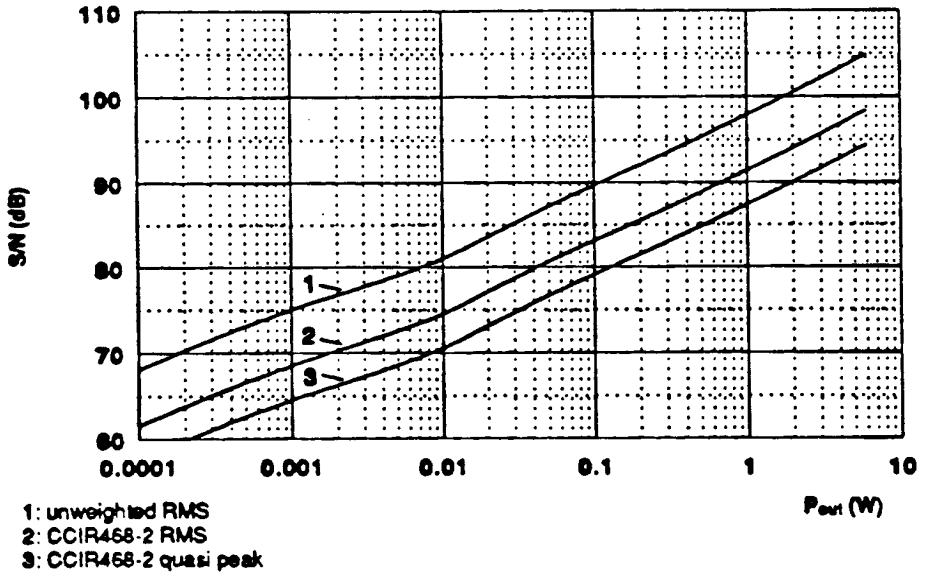


Figure 6b. Signal-to-noise ratio; V_i = 2V; P_{max} = 6W

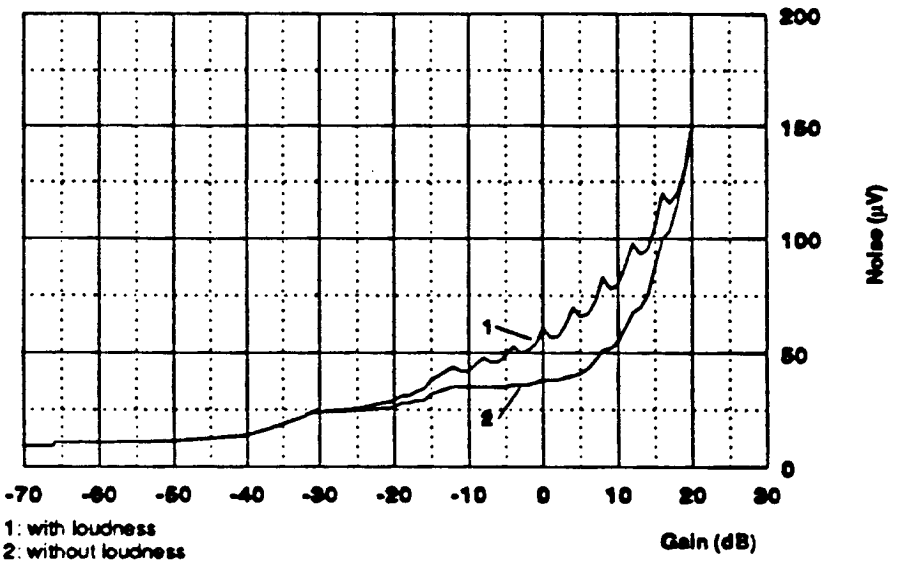
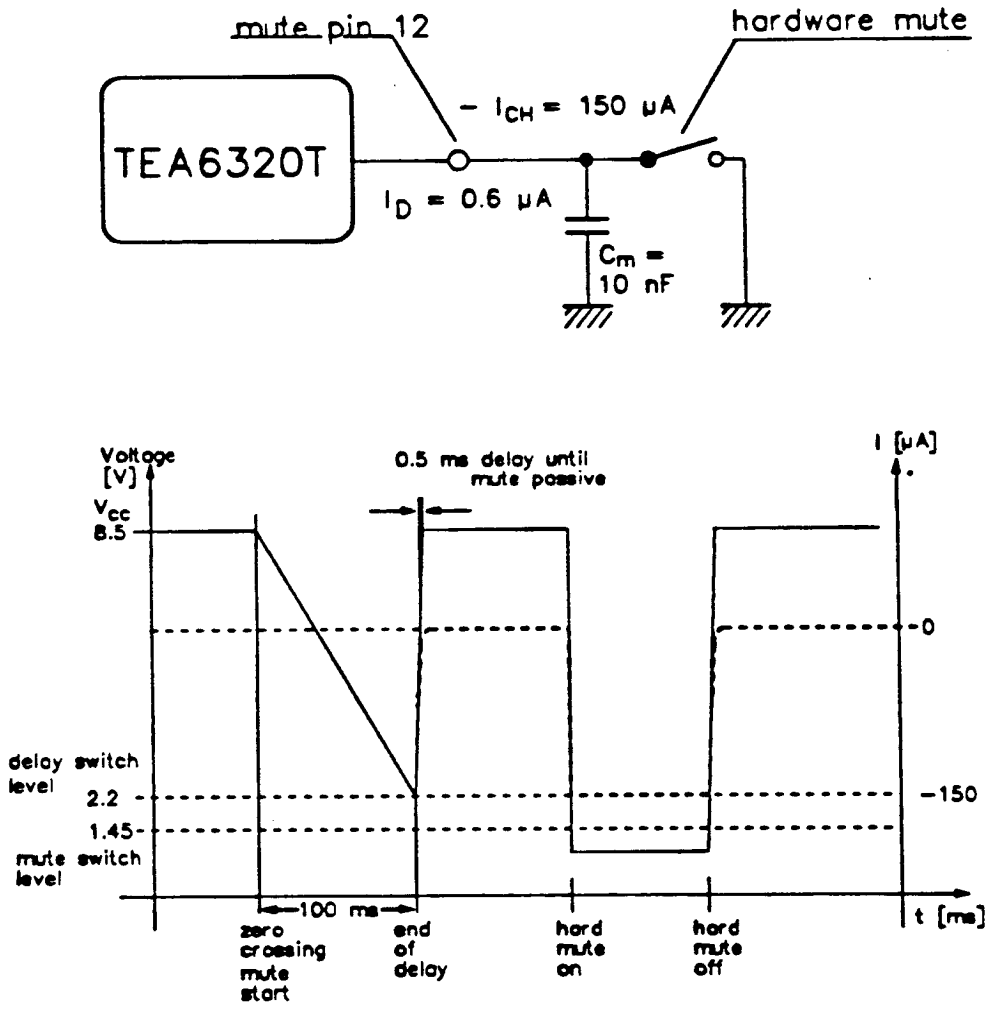


Figure 7. Noise output voltage; CCIR468-2, quasi peak



delayswitch level voltage is typically 2.2 V and is corresponding to $3xV_{BE}$

Figure 8. Notes to the mute function

In case the 20dB gain is not needed for the maximum volume position, it will give some profit to use the maximum boost gain and then increased attenuation in the last section, Volume II.

Therefore the loudness will be at the right place and a lower noise and offset voltage will be achieved.

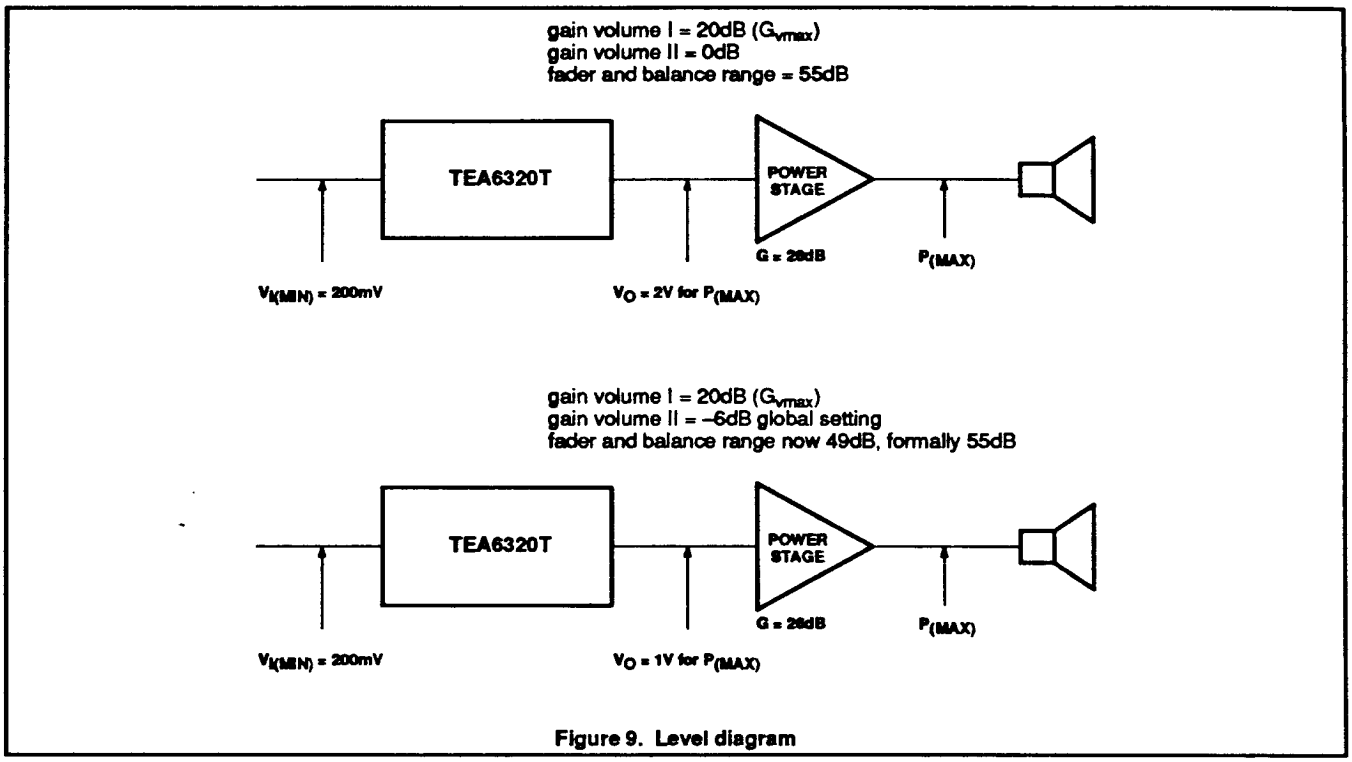


Figure 9. Level diagram

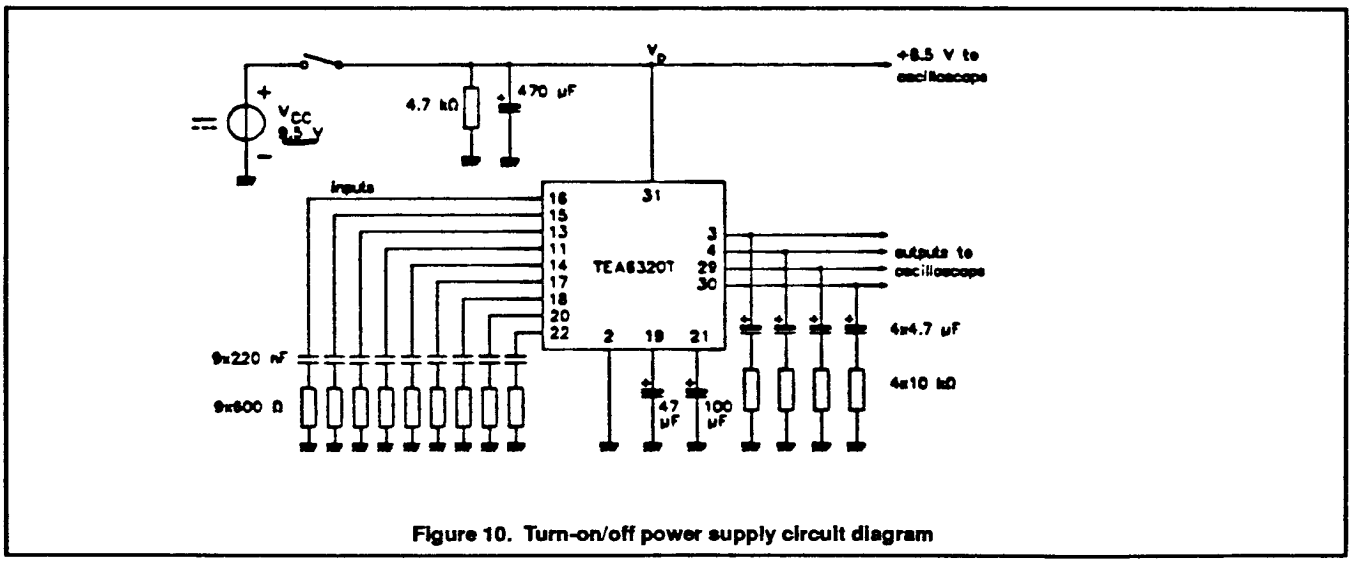


Figure 10. Turn-on/off power supply circuit diagram

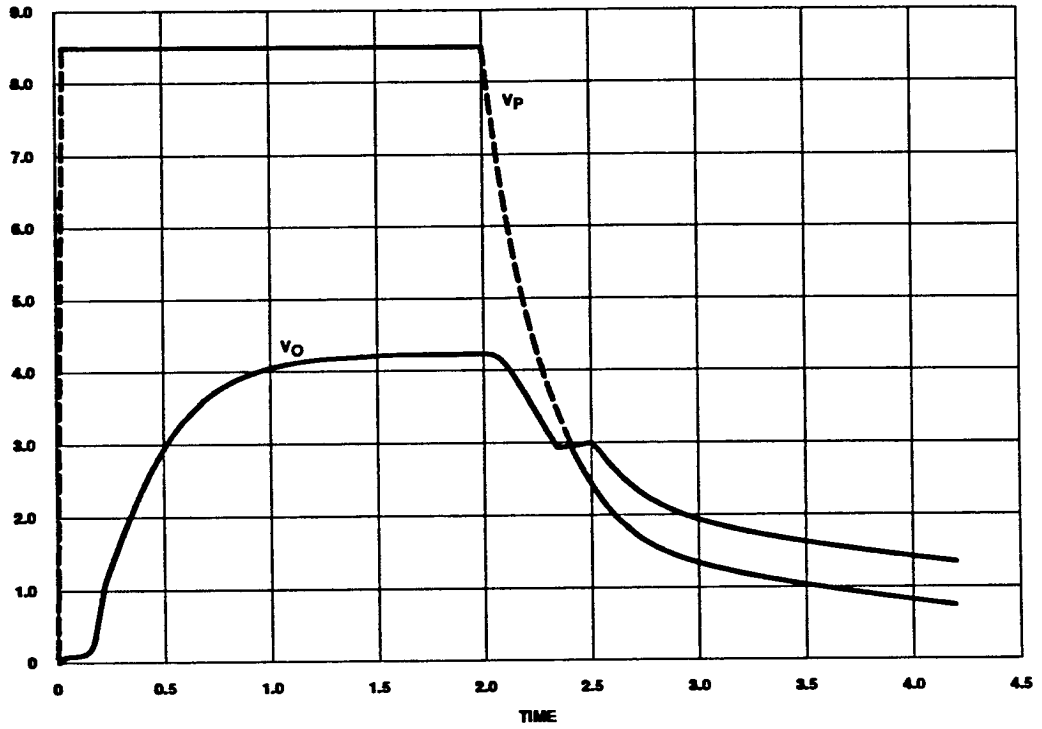


Figure 11. Turn-on/off behavior