

AN377/0594

# **APPLICATION NOTE**

1/21

# TEA5101A - RGB HIGH VOLTAGE AMPLIFIER BASIC OPERATION AND APPLICATIONS

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The aim of this Application Note is to describe the basic operation of the TEA5101A video amplifier and to provide the user with basic hints for the best utilization of the device and the realisation of high performance applications. Application examples are also provided to assist the designer in the maximum exploitation of the circuit.

#### GENERAL

The control of state-of-the-art color cathode ray tubes requires high performance video amplifiers which must satisfy both tube and video processor characteristics.

When considering tube characteristics (see Figures 13 and 14),we note that a 130V cutoff voltage is necessary to ensure a 5mA peak current. However 150V is a more appropriate value if the saturation effect of the amplifier is to be taken into account. As the dispersion range of the three guns is  $\pm$  12%, the cutoff voltage should be adjustable from 130V to 170V. The G2 voltage, from 700 to 1500V allows overall adjustment of the cutoff voltage for similar tube types.

A 200V supply voltage of the video amplifier is necessary to achieve a correct blanking operation. In addition, the video amplifier should have an output saturation voltage drop lower than 15V, as a drive voltage of 130V (resp. 115V) is necessary to obtain a beam current of 4 mA for a gun which has a cutoff point of 170V (resp. 130V).

**Note**: For all the calculations discussed above, the G1 voltage is assumed to be 0V.

The video processor characteristics must also be considered. As it generally delivers an output voltage of 2 to 3V, the video amplifier must provide a closed loop DC gain of approximately 40.

The video amplifier dynamic performances must also meet the requirements of good definition even with RGB input signals (teletext,home computer...), e.g. 1mm resolution on a 54cm CRT width scanned in 52 $\mu$ s. Consequently, a slew rate better than 2000V/ $\mu$ s, i.e. rise and fall times lower than 50ns, is needed. In addition, transition times must be the same for the three channels so as to avoid coloured transitions when displaying white characters. The bandwidth of a video amplifier satisfying all these requirements must be at least 7MHz for high level signals and 10MHz for small signals.

One major feature of a video amplifier is its capability to monitor the beam current of the tube. This function is necessary with modern video proces-

#### sors:

- for automaticadjustment of cutoff and also, where required, video gain in order to improve the long term performances by compensation for aging effects through the life of the CRT. This adjustment can be done either sequentially (gun after gun) or in a parallel mode.
- for limiting the average beam current

A video amplifier must also be flashover protected and provide high crosstalk performances. Crosstalk effects are mainly caused by parasitic capacitors and thus increase with the signal frequency. A crosstalk level of -20dB at 5MHz is generally acceptable.

Table 1 summarizes the main features of a high performance video amplifier.

**Table 1:** Main Features of a High Performance Video Amplifier

Maximum Supply Voltage	220V
Output voltage swing "Average"	100V
Output voltage swing "Peak"	130V
Low level saturation (refered to VG1)	15V
Closed loop gain	40
Transition time	50ns
Large signal bandwidth	7MHz
Small signal bandwidth	10MHz
Beam current monitoring	
Flash over protection	
Crosstalk at 5MHz	-20dB

The SGS-THOMSON Microelectronics TEA5101A is a high performance and large bandwidth 3 channel video amplifier which fulfills all the criteria discussed above. Designed in a 250V DMOS bipolar technology, it operates with a 200V power supply and can deliver 100V peak-to-peak output signals with rise and fall times equal to 50ns.

The 5101A features a large signal bandwidth of 8MHz, which can be extended to 10MHz for small signals (50 Vpp).

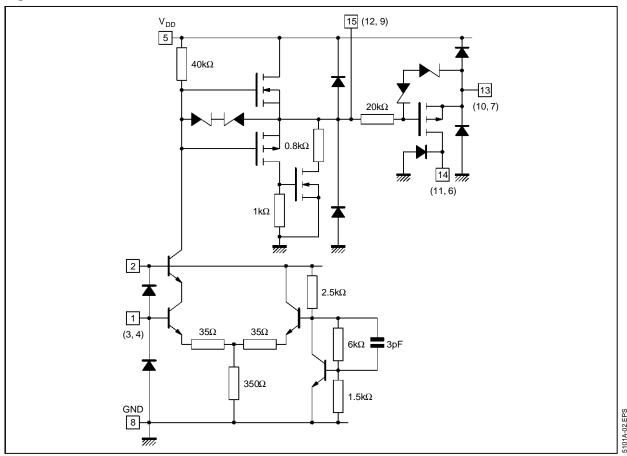
Each channel incorporates a PMOS transistor to monitor the beam current. The circuit provides internal protection against electrostatic discharges and high voltage CRT discharges.

The best utilization of the TEA5101A high performance features such as dynamic characteristics, crosstalk, or flashover protection requires optimized application implementation. This aspect will be discussed in the fourth part of this document.

#### I - DESCRIPTION

The complete schematic diagram of one channel of the TEA5101A is shown in Figure 1.

Figure 1



# I.1 - Input Stage

The differential input stage consists of the transistor  $T_1$  and  $T_2$  and the resistors  $R_4$ ,  $R_5$  and  $R_6$ .

This stage is biased by a voltage source  $T_3$ , $R_1$ , $R_2$  and  $R_3$ .

$$V_B(T_1) = (1 + \frac{R_2}{R_3}) \times V_B(T_3) \cong 3.8V$$

Each amplifier is biased by a separate voltage source in order to reduce internal crosstalk. The load of the input stage is composed of the transistor  $T_4$  (cascode configuration) and the resistor  $R_7$ . The cascode configuration has been chosen so as to reduce the Miller input capacitance. The voltage gain of the input stage is fixed by  $R_7$  and the emitter degeneration resistors  $R_5$ ,  $R_6$ , and the  $T_1$ ,  $T_2$  internal emitter resistances. The voltage gain is approximately 50dB.

Using a bipolar transistor T<sub>4</sub> and a polysilicon resistor R<sub>7</sub> gives rise to a very low parasitic capaci-

tance at the output of this stage (about 1.5pF). Hence the rise and fall times are about 50ns for a 100V peak-to-peak signal (between 50V and 150V).

# I.2 - Output Stage

The output stage is a quasi-complementary class B push-pullstage. This design ensures a symetrical load of the first stage for both rising and falling signals. The positive output stage is made of the DMOS transistor  $T_5$ , and the negative output stage is made of the transistors PMOS  $T_6$  and DMOS  $T_7$ . The compound configuration  $T_6$ - $T_7$  is equivalent to a single PMOS. A single PMOS transistor capable of sinking the total current would have been too large.

By virtue of the symetrical drive properties of the output stage the rise and fall times are equal (50ns for 100V DC output voltage).

# I.3 - Beam Current Monitoring

This function is performed by the PMOS transistor  $T_8$  in source follower configuration. The voltage on the source (cathode output) follows the gate voltage (feedback output). The beam current is absorbed via  $T_8$ . On the drain of  $T_8$ , this current will be monitored by the videoprocessor.

# I.4 - Protection Circuits

# I.4.1 - MOS protection

Four zener diodes  $DZ_{(1-4)}$  are connected between gate and source of each MOS in order to prevent the voltage from reaching the breakdown voltage. Hence the  $V_{GS}$  voltage is internally limited to  $\pm$  15V.

# I.4.2 - Protection against electrostatic discharges

All the input/outputpins of the TEA5101A are protected by the diodes  $D_1$ - $D_7$  which limit the overvoltage due to ESD.

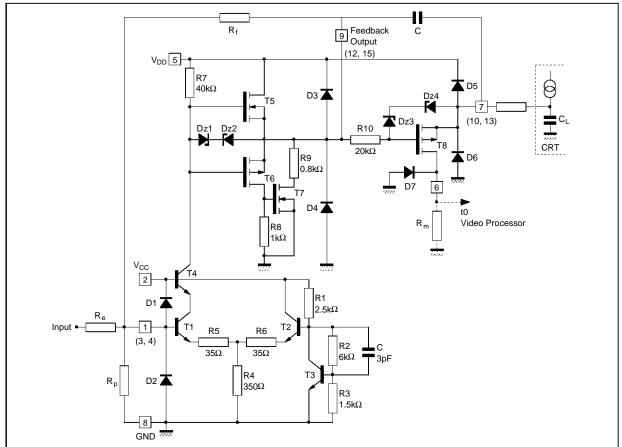
# I.4.3 - Flashover Protection

A high voltage and high current diode  $D_5$  is connected between each output and the high voltage power supply. During a flash, most of the current is generally absorbed by the spark gap connected to the CRT socket. The remaining current is absorbed by the high voltage decoupling capacitor through the diode  $D_5$ . Hence the cathode voltage is clamped to the supply voltage and the output voltage does not exceed this value.

# **II - FUNCTIONAL DESCRIPTION**

The schematic diagram of one TEA5101A channel with its associated external components is shown in Figure 2.

Figure 2



1010

# II.1 - Voltage Amplifier

# II.1.1 - Bias conditions V<sub>in</sub> = V<sub>ref</sub>

The bias point is fixed by the feedback resistor  $R_f$ , the bias resistor  $R_p$ , and by the internal reference voltage when  $V_{in} = V_{ref}$ .

If Vo is the output voltage (pin 9):

$$V_0 = (1 + \frac{R_f}{R_p}) \times V_{ref}$$
 (1)

In this state  $T_1$  and  $T_2$  are conducting. A current flows in  $R_7$  and  $T_4$  so  $T_5$  is on. The  $T_5$  drain current is fed to the amplifier input through the feedback resistor. The current in  $R_7$  is:

$$I(R_{7)} = \frac{V_{DD} - V_{O} - V_{GS}(T_{5)}}{R_{7}} \cong \ \frac{V_{DD} - V_{O}}{R_{7}}$$

and the current in  $T_5$  and  $R_f$  is :

$$I(T_{5)} = \frac{V_O - V_{ref}}{R_f} \cong \ \frac{V_O}{R_f}$$

Thus the total current absorbed by each channel of the TEA5101A is:

$$\frac{V_{DD}}{R_7} + V_0 \times (\frac{1}{R_f} - \frac{1}{R_7})$$

The cathode (pin 7) output voltage is:

$$V_O + V_{GS}(T_8) = V_O$$

The beam current is absorbed by  $T_8$  and  $R_m$ . The voltage developed across  $R_m$  by this current is fed to the videoprocessor in order to monitor the beam current.

# II.1.2 - Dynamic operation

The TEA5101A operates as a closed loop amplifier, with its voltage gain fixed by the resistors  $R_{\rm f}$  and  $R_{\rm e}$ .

Since the open loop gain A is not infinite, the resistor  $R_p$  and the input impedance  $R_{in}$  must be considered. Hence the voltage gain is

$$G = -\frac{R_f}{R_e} \times \frac{1}{1 + \frac{1}{A} (1 + \frac{R_f}{R_p /\!\!/ R_e /\!\!/ R_{in}})}$$
 (2)

# II.1.2.1 - Input voltage V<sub>in</sub> < V<sub>ref</sub> (black picture)

In this case the current flowing in  $R_7$  and  $T_1$  decreases whilst the collector voltage of  $T_4$  and the output voltage both increase. In the extreme case,  $I(T_1) = I(R_7) = 0$  and  $V_{OD}$ - $V_{DD}$ - $V_{GS}(T_5)$ 

In order to charge the tube capacitor the voltage is fed to the cathode output in two ways:

- through the PMOS (with a VGS difference) for the low frequency part
- through the capacitor C for the high frequency part (output signal leading edge)

To correctly transmit the rising edge, the value of

the capacitor C must be high compared to  $C_L$ . With the current values used (C = 1nF, $C_L$  = 10pF), the attenuation is very small (0.99)

# II.1.2.2 - Input voltage $V_{in} > V_{ref}$ (white picture)

In this case, the current in  $R_7$  and  $T_1$  increases with an accompanying drop of  $T_4$ 's collector voltage until  $T_1$  and  $T_4$  are saturated. At this point:

$$V_O \cong V_C(T_4) \cong V_{CC}$$

During a high to low transition (i.e. black-white picture), the beam current is absorbed in two ways:

- through the capacitor C and the compound PMOS T<sub>6</sub>-T<sub>7</sub> for the high frequency part (falling edge)
- through the PMOS T<sub>8</sub> and the resistor R<sub>m</sub> for the low frequency part.

# II.2 - Beam Current Monitoring II.2.1 - Stationary state

The beam current monitoring is performed by the PMOS  $T_8$  and the resistor  $R_m$ . When measuring low currents (leakage, quasi cutoff), the  $R_m$  value is generally high. When measuring high currents (drive, average or peak beam current),  $R_m$  is generally bypassed by a lower impedance.

It should be noted that the current supplied by the three guns flows through this resistor. Hence, with too large a value for the resistor R<sub>m</sub>, the cathode voltage of the tubes will become too high for the required operating current values. This is a fundamental difference between the TEA5101A and discrete video amps. In discrete video amps, the current monitoring transistor is a high voltage PNP bipolar which may saturate. In this case the beam current can flow through the transistor base and it is no longer monitored by the video processor. This effect does not occur with the TEA5101A.

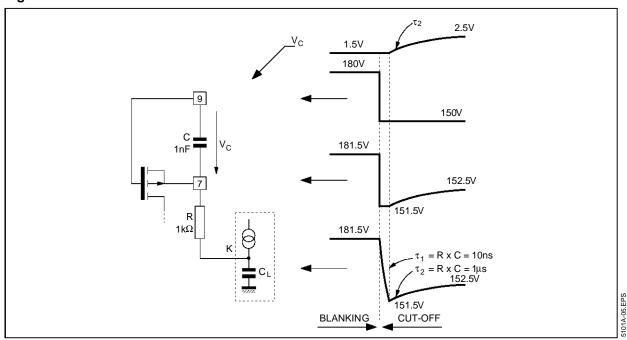
# II.2.2 - Transient phase : low current measurements

The cut-off adjustment sequence is generally as follows:

In a first step, the cathode is set to a high voltage (180V) in order to blank the CRT and to measure the leakage current. In a second step, the tube is slighly switched on to measure a very low current (quasi cut-off current). This operation is performed by setting the cathode voltage to about 150V and adjusting it until the proper current is obtained. The maximum time available to do this operation is generally about  $52\mu s$ .

Figure 3 shows the simplified diagram of the TEA5101A output, the voltages during the different steps, and the stationary state the system must reach for correct adjustment.

Figure 3



During the blanking phase, the tube is switched off, the PMOS is switched off and its  $V_{GS}$  voltage is equal to the pinch-off voltage (about 1.5V). The voltages at the different nodes are shown in figure 3 (V(9) = 180V, V(k) = 181.5V). The falling edge of the cutoff pulse is instantaneously transmitted by the capacitor C. When the stationary state is reached, the cathode voltage will be 152.5V if the voltage on pin 9 is 150V, as the VGS voltage of the conducting PMOS is about 2.5V.

We can see that the voltage on C must increase by an amount of  $\Delta Vc$  = 1V. This charge is furnished by the tube capacitor which is discharged by an amount of  $\Delta VC_L$  = 29V with a time constant equal to R x C<sub>L</sub> (10 ns). By considering the energy balance, we can calculate the maximum charge  $\Delta Vmax$  that  $C_L$  can furnished to C

$$\Delta V_{max} = \sqrt{\frac{C_L}{C}} \; x \; \Delta V_{CL} \cong \; \; 3V$$

Since this voltage is greater than  $\Delta V_C$ , the capacitor C can be charged and the stationary state is

reached without any contribution being required from the tube current, i.e. the whole tube current can flow through the PMOS and the adjustment can be performed correctly.

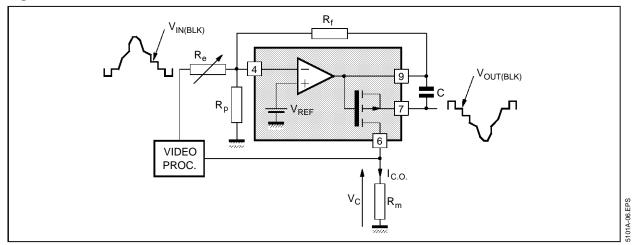
Considering higher voltage and beam current swings, the margin is greater because:

- the voltage swing across the tube capacitor is greater
- the tube current is higher and the picture is not disturbed even if part of the beam current is used to charge the capacitor C.

# **III - EXTERNAL COMPONENTS CALCULATION**

The implementation of the TEA5101A in an application requires the determination of external component values. These components are  $R_f$ ,  $R_e$ ,  $R_p$  and  $R_m$  (see Figure 4). The dissipated power in the IC and in the feedback resistor  $R_f$  must also be calculated in order to correctly choose the power ratings of the heatsink and resistors.

Figure 4



# III.1 - Components Value Calculation

From equations 1 and 2 in section II-1, both the value of the DC output voltage and the voltage gain depend directly on the resistor Rf. Hence Rf must be determined first before calculating the value of Re and Rp in order to obtain the correct gain and DC output voltage.

#### III.1.1 - Feedback resistor Rf

The value of Rf must be as low as possible in order to obtain the optimum dynamic performance from the TEA5101A(see section IV-1). A typical value of R<sub>f</sub> is 39 k $\Omega$ .

#### III.1.2 - Input resistor Re

The voltage gain is calculated from the following formula (see section II-1):

$$G = -\frac{R_f}{R_e} \frac{1}{1 + \frac{1}{A} (1 + \frac{R_f}{R_p /\!\!/ R_e /\!\!/ R_{in}})}$$

Since the open loop gain A is high enough (50dB), we can approximate the calculation:

$$G @ -\frac{R_f}{R_s}$$

where R<sub>e</sub> is generally implemented as a variable value for channel gain adjustment.

If the gain adjustment range 
$$G_{min}$$
,  $G_{max}$  is known: 
$$R_{e\ min} = \frac{R_f}{G_{max}} \ and \ R_{e\ max} = \frac{R_f}{G_{min}}$$

With  $G_{min} = 15$  and  $G_{max} = 80$ :

 $R_e$  will be made of a  $2.2k\Omega$  potentiometer and  $470\Omega$ fixed resistor.

#### III.1.3 - Bias resistor R<sub>p</sub>

R<sub>p</sub> must be chosen in such a way that the black

level output voltage VouT(BLK) is equal to the cutoff voltage, which is a characteristic of the tube currently used, when the DC black level input voltage V<sub>IN(BLK)</sub> is the mean value of the adjustment range of the video processor. This is the optimum condition to ensure a correct adjustment during the lifetime of the tube. Rp can be calculated by considering the TEA5101A as an operational amplifier and applying the usual formula:

and applying the usual formula : 
$$R_p = \frac{V_{ref}}{\frac{V_{out} \left(BLK\right) - V_{ref}}{R_f}} + \frac{V_{in} \left(BLK\right) - V_{ref}}{R_e}$$
 - If  $V_{in}(BLK) = V_{ref}$  R  $P_p = \frac{V_{ref}}{V_{out} \left(BLK\right) - V_{ref}} \times R_f$  For a 150V black level : 
$$R_p = 1k\Omega \qquad \qquad \text{with} \quad R_f = 39k\Omega$$
 - If  $V_{in} \left(BLK\right) \neq V_{ref}$  : 
$$V_{in} \left(BLK\right) = 2.7V$$
 R  $P_p = 1.2k\Omega \qquad \qquad \text{with} \qquad R_f = 39k\Omega$  Or 
$$V_{in} \left(BLK\right) = 6.7V$$
 Or 
$$V_{in} \left(BLK\right) = 6.7V$$
 With  $R_f = 39k\Omega$ 

# III.1.4 - Current measurement resistor R<sub>m</sub>

for a 150V black level

R<sub>m</sub> must be determined by taking into account the quasi cutoff current Ico and the input voltage VC of the video processor.

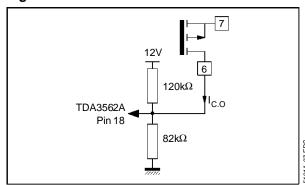
 $R_e = 1.5k\Omega$ 

$$R_m = \frac{V_C}{I_{CO}}$$

- With the videoprocessor TEA5031D ( $V_C = 2V$ ):  $R_m = 120k\Omega$  with  $I_{CO} = 16\mu A$ 

- With the videoprocessor TDA3562A (Vc = 0.5V) which requires a DC biased input "Black current stabilization" (pin 18), the schematic diagram is the following:

Figure 5



The DC bias is 
$$12 \times \frac{82}{120 + 82} = 5V$$

The quasi cutoff current is

$$0.5 \left(\frac{1}{120} + \frac{1}{82}\right) \times 1 \times 10^{-3} = 10 \mu A$$

# III.2 - Dissipated Power in External Components

The only components dissipating power are the TEA5101A and the feedback resistor. The dissipated power has a constant static component and a dynamic component which increases with frequency. The theoretical calculation is not sufficiently accurate to determine the correct dissipated power. The best way consists of measuring the power in different configurations of the circuit: steady state (no input), sinusoidal input, and in situ (in a TV set with a video input signal). The measurement method will be described first and then the results and calculations will be discussed.

# III.2.1 - Measurement method

The dissipated power can be determined by measuring the average supply current IDD (principally high voltage supply current V<sub>DD</sub>) and by subtracting the power dissipated in the external components from the calculated power delivered by this supply voltage.

The power delivered by the high voltage power supply is :  $P = V_{DD} \times I_{DD}$ 

The power dissipated in the external components (principally the feedback resistor R<sub>f</sub>) is:

- for the static part: 
$$P_{SR} = \frac{3 \times V^2}{R_f} = \frac{3 \times V^2}{R_f$$

- for the dynamic part: 
$$P_{DR} = \frac{3 \times V^2_{OUT} (RMS)}{R_f}$$

When the IC is driven by a sinusoidal signal (capacitive drive) the measurement and calculation are straightforward:

- Vour(AVG) = Vour(DC)  
- Vour(RMS) = 
$$\frac{\text{Vour}(\text{peak to peak})}{2 \times \sqrt{2}}$$

With Vout (DC) = 100V and

 $V_{OUT}$  (peak to peak) = 100V and  $R_f = 39k\Omega$ 

Psr = 0.8W

 $P_{DR} = 0.1W$ 

Measurements are more difficult to carry out when the IC is working in a TV set. Vout(AVG) can be measured with an oscilloscope (difference of level between AC and DC coupling) and VOUT (RMS) can be measured by connecting an RMS voltmeter to the feedback resistor. In this case we have the following results (see section 2.2.3):

- Vout (AVG) = 130V and PsR = 1.3W

- Vout (RMS) = 32V and PDR = 80mW

In each case, the term PDR can be neglected as a reasonable approximation. Hence, the power dissipated by the IC will be:

$$P_i = V_{DD} \times I_{DD} - \frac{3V^2_{OUT}(AVG)}{R_f}$$

and the power dissipated in Rf will be:

$$P_r = \frac{V^2_{OUT} (AVG)}{R_f}$$

# III.2.2 - Results

# III.2.2.1 - Static power

Table 2 shows the measured values of  $I_{DD}$  and the calculated power for three values of Vout and for  $V_{DD} = 200V$ 

Table 2

V <sub>OUT</sub> (V)	I <sub>DD</sub> (mA)	P <sub>i</sub> (W)	P <sub>r</sub> (W)
50	16	3	0.065
100	15	2.2	0.25
150	14.6	1.2	0.6

We can see that the static power dissipated in the IC decreases with V<sub>OUT</sub> increasing, but obviously the power dissipated by Rf increases as Vout increases.

#### III.2.2.2 - Measurement with sinusoidal input

Table 3 summarizes the results obtained from practical measurements as functions of V<sub>OUT</sub>(DC) and of the frequency (the three channels are driven simultaneously).

We can see that when driving the IC with a HF sinusoidal signal, care must be taken to avoid excessive temperature increase.

Table 3

V <sub>оит</sub> (V)	I <sub>DD</sub> 1MHz (mA)	I <sub>DD</sub> 7MHz (mA)	V <sub>OUT</sub> (PP) 1MHz (V)	V <sub>OUT</sub> (PP) 7MHz (V)	P <sub>i</sub> 1MHz (W)	P <sub>i</sub> 7MHz (W)	P <sub>r</sub> (W)
50	20.7	44.6	66	50	3.9	8.7	0.065
100	20	59.5	100	80	3	11	0.25
150	18	45	100	67	1.7	8.2	0.6

#### III.2.2.3 - Measurement in a TV set

We have determined the worst cases of dissipation in a TV set. These trials have been carried out on one particular TV set, and may not be representative for all TV sets. In this particular TV set, the worst cases of dissipation occur with noise signal (from HF tuner) and with a multiburst pattern (0.8 to 4.8MHz) in RGB mode.

Table 4 summarizes the results in these two cases when the brightness control is set to min and max value (the contrast control is set to max).

Table 4

	V <sub>OUT</sub> (AVG) (V)	I <sub>DD</sub> (mA)	V <sub>DD</sub> (V)	P <sub>i</sub> (W)	P <sub>r</sub> (W)
Bright.max Noise	148	22.2	218	3.15	0.56
Bright.min	188	23.3	224	2.5	0.9
Bright.max Multiburst	131	23.6	213	3.7	0.44
Bright.min	158	22	221	2.9	0.64

# III.2.3 - Design of heatsink and external components

# III.2.3.1 - Heatsink

As discussed above, the power dissipated in the IC in a TV set can reach about 4W. In this case, a  $12^{\circ}$ C/W heatsink seems to be sufficient. Such a heatsink will give  $T_i = 115^{\circ}$ C for  $T_{room} = 60^{\circ}$ C.

The resulting margin guarantees correct reliability.

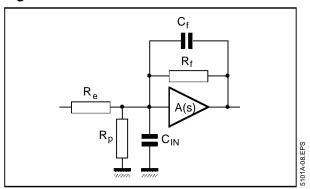
### III.2.3.2 - Feedback resistors

1 Watt type feedback resistors must be used, as they may need to dissipate 0.9W when the TV set is working and up to 1W when the TV is blanked ( $V_{OUT} = 200V$ ), for example when the security of the scanning processor is activated.

# IV - APPLICATION HINTS IV.1 - Dynamic Performances

Figure 6 shows the simplified schematic diagram of the TEA5101A in AC mode.

Figure 6



 $C_{\mbox{\scriptsize f}}$  is the parasitic capacitor between the input and the output.

C<sub>in</sub> is the parasitic capacitor between the input and ground. The voltage gain versus frequency can be deduced from the formula (2) in chapter II section 1.2:

$$G(s) = \frac{R_f}{R_e (1 + R_f C_f s)} \cdot \frac{1}{1 + \frac{1}{A(s)} \left(1 + \frac{R_f}{R_{eq}} \frac{1 + R_{eq} C_{in} s}{1 + R_f C_f s}\right)}$$
with Peg-Pa//Pa//Pip and A(s) open loop gain

with Req=Rp//Re//Rin and A(s) open loop gain

A(s) is a second order function such as

AO

$$1 + bs + as^2$$

with  $a = 9 \times 10^{-16} \text{ s}^2$ ,  $b = 60 \times 10^{-9} \text{ s}$ , AO = 400

$$\begin{aligned} & \text{Assuming R}_{eq} \ x \ C_{in} = R_f \ x \ C_f, \ we \ find: \\ & G(s) = -\frac{R_f}{R_e \ (1 + R_f \ C_f \ s)} \ x \frac{1}{1 + \frac{B}{AO}} \ x \frac{1}{1 + \frac{B}{AO + B}} \ bs + \frac{B}{AO + B} \ as^2 \end{aligned}$$

with B = 1 + 
$$\frac{R_f}{R_{eq}}$$

We see that the closed loop amplifier is equivalent to a combination of a second order circuit and a first order one. The latter comprises the feedback resistor and the parasitic capacitor between input and output.

With the current values :  $R_f$  = 39k $\Omega$ ,  $R_e$  = 2k $\Omega$ ,  $R_{in}$  = 14k $\Omega$ ,  $R_p$  = 1.2k $\Omega$ ,  $C_f$  = 0.5pF,  $C_{in}$  = 15pF

we have  $R_{eq} \times C_{in} = 10$ ns,  $R_f \times C_f = 20$ ns, B = 56The second order circuit characteristics are : Natural frequency :

$$F_n = \frac{1}{2 \times \pi \times a} \times \frac{AO + B}{B} = 15MHz$$

damping factor:

$$z = \frac{b}{2 \times a} \times \frac{B}{AO + B} = 0.35$$

The cut off frequency of the first order circuit is:

$$f_C = \frac{1}{2 \times \pi R_f \times C_f} = 8MHz$$

The amplifier response is thus the combination of the responses of these two circuits. The contribution of the parasitic capacitor  $C_f$  to the frequency response is very important. If the value of  $C_f$  is too high, the contribution of the first order circuit will be of overriding importance and the resulting bandwidth of the amplifier will be too small. If the value of  $C_f$  is too low, the response curve will have a peak (due to the second order circuit). A "ringing" effect will be present on pulse-type signals and an instability and oscillation can occur at some frequencies.

This capacitor is generally too high. It consists of:

- the self parasitic capacitor of the feedback resistor
- the parasitic capacitor due to the PCB layout.

Practically, the best bandwidth performances are achieved by:

- the smallest input-output capacitor and the smallest capacitor between an input and ground
- using a feedback resistor with the smallest possible value but large enough to yield a sufficiently high gain.
- using a feedback resistor with small parasitic capacitance (typ 0.2pF). Some resistors have 0.5 or 0.8 pF parasitic capacitor.

The parasitic capacitors discussed above are usually the ones which need to be taken into account. However any other parasitic capacitor or inductor can modify the frequency response. For instance, a too large capacitor value between the feedback output and ground can create a dominant pole and cause a potential risk of oscillation.

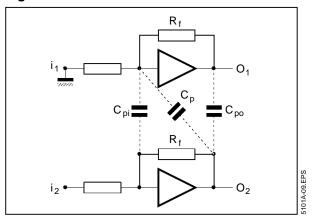
# IV.2 - Crosstalk

Figure 7 shows the different parasitic links inducing crosstalk.

The crosstalk can be caused by:

- parasitic coupling between the inputs (C<sub>pi</sub>)
- parasitic coupling between the outputs (Cpo)
- parasitic coupling between an output and a near input of another channel (C<sub>p</sub>).

Figure 7



Parasitic coupling may be capacitive or be caused by HF radiations.

The third type of parasitic coupling is predominant since it involves the addition by feedback at relatively high level(output) signals to relatively low level (input) signals. For example, a 0.1pF  $C_P$  parasitic capacitor between an output and the input of another channel will act as a differenciator with the feedback resistor  $R_f = 39k\Omega$ .

The transfer function of this integrator will be  $R_f x C_p x s$  (0.2j at 8MHz) and thus the crosstalk will be -14dB at 8MHz. The parasitic coupling between inputs and outputs must be minimized to achieve an acceptable crosstalk (-20dB at 5MHz). This can be done by crossing only the input wires and separating the input and output leads. High voltage components and wires must be laid out as far as possible from small signal wires, even if this results in a larger circuit board.

HF radiations from the feedback resistor must not induced a voltage signal at the input of another channel. This can be achieved by :

- spacing out the feed back resistors
- mounting these resistors in the same direction and strictly aligned one under another.
- mounting these resistors 1cm above the PC board
- using ground connections to insulate the input wires

# **IV.3 - Flashover Protection**

A picture tube has generally several high voltage discharges in its lifetime. This is due to the fact that the vacuum is not perfect coupled with the presence of metallic particles evaporated from the electrodes. Hence, short circuits (very brief fortunately) can occur between two electrodes, one of which is usually the anode (at EHT potential). An overvoltage can be induced on the cathodes or on the

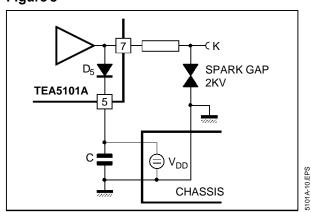
supplies even if a flash occurs on an electrode other than a cathode, because of the possibility of flashes in series or overvoltages due to inductive links on the video board or on the chassis. These overvoltages can destroy an IC particularly the video amplifier which is the most vulnerable since it is directly connected to the tube.

The tube manufacturers have made much progress in technology in order to reduce the frequency of flashes and their associated energy (increased quality of vacuum, internal resistance for "soft flash" tubes). Nevertheless, some protection measures are suggested by the tube manufacturers:

- connect spark gaps on each electrode (1 to 3kV or 12kV for focus)
- connect the spark gaps to a separated ground directly connected to the chassis ground by a non inductive link
- connect the cathodes or grids by protective resistors. These resistors must be able to withstand 12kV (20kV for focus)instantaneous voltages without breakdown and without any change of value following successive flashes. These resistors must be of a non-capacitive type. 1/2W (1W for focus) hot molded carbon type resistors are well suited for this application.
- the grid and cathode connections on the PC board must be as short as possible and spaced well away from other connections in order to avoid parasitic inductions.

Furthermore, the TEA5101A has been provided with an additional effective feature to improve the flashover protection. As described in section I-4, a protection device has been included comprising a high voltage high current diode which is connected between each output and the high voltage power supply. The equivalent diagram of this protection is shown in Figure 8.

Figure 8

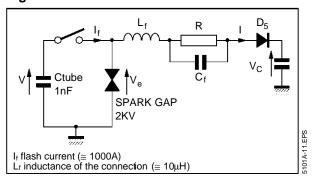


The flash current is diverted to the ground through the diode and the decoupling capacitor C.

Two kinds of flashes can occur:

1) low resistance flashes during which the spark gaps are activated since the cathode voltage exceeds the breakdown value of the spark gap. In this case the equivalent diagram is the following:

Figure 9



Ctube previously charged to 28kV is instantaneously discharged during

$$\Delta t = C_{tube} \times \Delta \frac{V}{I_f} = 30 \text{ns}$$

Since the voltage across the spark gap falls almost instantaneously to 2000V, the peak current I flowing into the diode is (assuming  $V_C$  is held by good decoupling):

$$I = \frac{V_e \times \Delta t}{L_f} = 6A$$

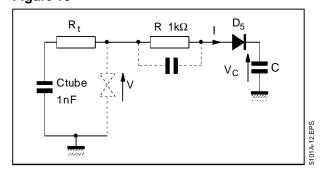
To ensure a variation of  $V_{\text{C}}$  less than 10V, C must be

$$C > \frac{I \times \Delta_t}{\Delta V_C}$$
 eg  $C > 18nF$ 

The decoupling must have good HF characteristics.

2) high resistance flashes in which the spark gaps are not activated. In this case the equivalent diagram is the following:

Figure 10



If V < 2 kV, I < 
$$\frac{2000}{R}$$
 , I < 2A and  $R_t \cong 12 k\Omega$ 

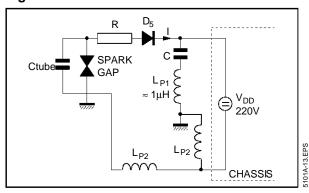
The time constant of the flash is  $R_t \times C_{tube} = 12 \, \mu s$ , the decaytime is approximatevely 30  $\mu s$ . The value of C must be

$$C > \frac{\Delta_t \times I}{\Delta V_C} \quad eg \quad C > 6 \mu F$$

in order to ensure a VC variation less than 10V.

The total decoupling will be made up by a  $10\mu\text{F}$  electrolytic capacitor connected in parallel with a 22nF plastic film capacitor with good HF properties. It must be placed very close to the TEA5101A to be efficient. Otherwise, the equivalent diagram will be the following (case of low resistance flash).

Figure 11



$$\Delta V_C = \frac{I \ x \ \Delta_t}{C} + \frac{L_{P1} \ x \ I}{\Delta_t}$$

 $\Delta V_C = 210V$  with  $L_{p1} = 1 \mu H$  and  $L_{p2} = 0$ 

In this case the  $V_{DD}$  voltage can rise to a dangerous value (+210V increase) and the protection is not efficient.

If the connection between the socket ground and the chassis ground is inductive ( $L_{p2} \neq 0$ ), the effect is the same.

However in this case, all the TV IC's, and not only the TEA5101A, will be exposed to destructive overvoltages.

# IV.4 - Output Swing

The simplified diagram of this function is shown in Figure 12 (see Chapter II and chapter III ).

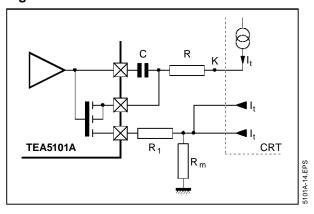
The current delivered by a CRT is given by the

characteristic curves (Figures 13 and 14).

The minimum value of  $V_k$  (due to all the voltage drops in the resistors and in the amplifier) is given by the equation (see Figure 12):

$$V_k = (R + R_{on} + R1 + 3 \times R_m) \times I_t = R_{eq} \times I_t$$
 (1) with  $R_{on}$ : on state PMOS resistance

Figure 12



To find the maximum available current  $It_{max}$ , we can draw the curves of the equation (1) on the tube characteristics.  $I_{tmax}$  will be given by the intersection point of the curves. Since the tube characteristics are:  $I_t v_s V_{cutoff} + V_{G1} - V_k$  the equation (1) must be changed to

$$I_{t} = \frac{V_{\text{CUTOFF}} + V_{\text{G1}} - V_{k}}{R_{\text{eq}}}$$
 (2)

Assuming  $V_{G1}$ = 0, we can draw the curves of equation (2) for several values of  $V_{cutoff}$  (eg 150V and 200V) and several values of  $R_{eq}$  (eg 5k,10k,15k,20k) (see Figures 13 and 14). We can see from these curves that  $R_{eq}$  must have the following values to allow the tube to source 4mA per gun :

$$R_{eq} \le 5k\Omega$$
 for a 150V cutoff point or  $R_{eq} \le 15k\Omega$  for a 200V cutoff point

As  $R_{on}$  value is approximatively 1.7k $\Omega$ , the measurement resistor must be as low as possible.

Working with higher cutoff point would be an alternative solution. But a 200V cutoff point seems to be too high a value since in this case the supply voltage would be greater than 200V and would affect reliability performances.

Figure 13

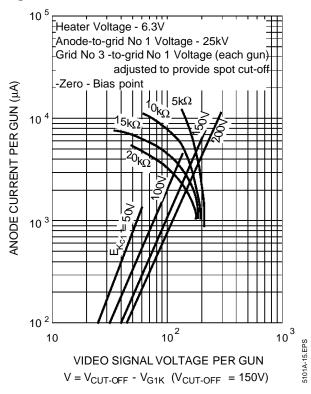
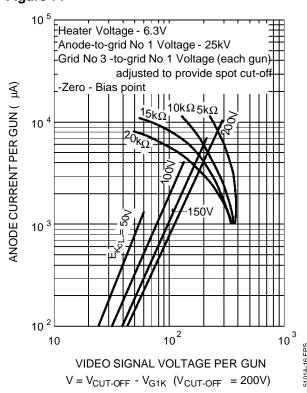


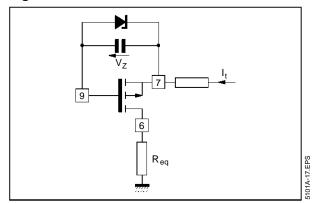
Figure 14



Another solution consists of connecting a zener diode as shown in Figure 15. With this device the

high current operation of the TEA5101A is similar to that of a discrete amplifier (with PNP) operation.

Figure 15



For low currents, if the zener voltage is greater than the  $V_{GS}$  voltage, the zener diode is biased off and the beam current flows through the measurement resistor. When the cathode voltage (pin 7) drop is limited because of the pin 6 voltage and when the pin 9 voltage continues to decrease, the zener diode is switched on when  $V_7 - V_9 = V_Z$ . In this case the beam current is absorbed by the voltage amplifier and the tube can provide larger current values. Nevertheless, the pin 7 output voltage will follow the pin 9 voltage with a  $V_Z$  difference.

Since the pin 9 voltage is internally limited to 14V, the output voltage will be limited to 22V with a 8V zener diode.

The CRT bias voltages shown on the previous curves are referenced to the  $G_1$  voltage. The TEA5101Ais referenced to ground. We can choose to work with a  $G_1$  voltage greater than ground and thus the low level saturation is not taken into account. In this case, the cutoff points must be increased. When choosing  $V_{G1}=12V$ , the cutoff points will be adjusted to 170V (instead of 150V). Since the power supply is 200V, 30V are available to ensure correct blanking operation. The DC output voltage must be increased by 12V from its previous value.

Note that all the phenomena described in this section concern a static or quasi-static (15kHz) operation (e.g. white picture or rather large white pattern on a black background). When current peaks occur (e.g white characters insertion or straight luminance transition), the peaks will be absorbed by the coupling capacitor and the voltage amplifier, and hence the tube will be able to source a greater current.

# **IV.5 - Low Current Measurements**

We have seen in section II-2.2 how the beam current monitoring works (see Figure 3). We have



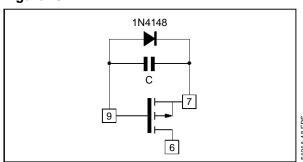
seen that the capacitor C must charge again after the blanking phase.

This charge is generally furnished by the tube capacitor independently from the beam current. However, if during the blanking phase, the output voltage is too low (e.g. the PMOS is reverse biased (-20V) because of a too high leakage current or when measuring with an oscilloscope probe), the  $\Delta VC$  required to charge C again will be greater than the maximum charge available from the tube capacitor. Hence the beam current will have to charge C in a first step.

Since this current is rather low during the cutoff adjustement phase, a long time will be spent to charge C. The current absorbed by the PMOS and fed to the videoprocessor will not be equal to the beam current and the cutoff adjustement will not be correct.

Hence the reverse voltage across the capacitor C must be limited by a diode connected as follows:

Figure 16



With this configuration, the voltage across C will be -0.6V max. Since this voltage must be 2.5V in the stationary state (see section II-2.2), the voltage across C must be increased by 3.1V and this charge can be supplied by  $C_L$ . We can also slightly decrease the value of C. However if C is too low, the HF behaviour will be impaired.

# V - APPLICATION EXAMPLES V.1 - Application Description

Figures 17 and 18 show two applications, one for a 45AX tube and the videoprocessor TDA3562A (application 1), the other designed for S4 type tube and the videoprocessor TEA5031D (application 2). In these two applications, the nominal gain is 28dB and the output black level is 150V. The quasi cutoff currents are respectively  $10\mu A$  and  $16\mu A$  for applications 1 and 2.

These applications are implemented using the same PC board especially designed to allow different options for tube biasing, power supply decoupling and connections. This PC board allows also two different tube sockets (jedec B8274 or B10277)

to be connected. Both beam current monitoring modes (sequential and parallel) are possible.

The layout and the electrical diagram of the PC board are shown in Figures 19 and 20.

### V.2 - Performance Evaluation

As seen in chapter IV, the dynamic performances (bandwidth, crosstalk) of the TEA5101A is very dependent on the PCB layout. Consequently, the evaluation board has been designed to obtain the best results.

To evaluate the performance, the best way is to work outside of the TV set by driving the amplifier by an HF generator (or a network analyser) while simulating the load conditions fixed by the CRT, since AC performances are directly determined by the load.

#### V.2.1 - Measurement conditions

The schematic diagrams of the AC measurements are shown in Figures 21 and 22. The conditions are as follows:

- BIASING :  $V_{OUTDC}$  = 100V by choosing  $R_{11}$  =  $R_{21}$  =  $R_{31}$  = 1.5k $\Omega$  and  $V_{DD}$  = 200V
- AC GAIN = 50 by adjusting P10, P20, P30
- LOADING:
- by a 8.2pF capacitor and the probe capacitor (2pF), the sum is equivalent to the capacitance of a CRT with the socket and the spark gaps
- the  $1M\Omega$  resistors connected between each output and  $V_{DD}$  allow the conduction of the beam current monitoring PMOS transistor in such a way that  $VA_{DC} = VB_{DC} = 100V$ .
- DRIVING by a  $1\mu F$  capacitor, the HF generator being loaded by  $50\Omega$ .
- the dynamic power dissipated in the IC will increase with frequency. To avoid the temperature increasing, it is necessary to do very quick measurements or to use a low R<sub>th</sub> (7°C/W) heatsink in forced convection configuration. Such conditions are not present in a TV set since the driving signal will be a video signal instead of a pure HF signal.

### V.2.2 - Results

# V.2.2.1 - Bandwidth

The curves Figures 23 and 24 show the frequency responses of one channel with  $100V_{pp}$  and  $50V_{pp}$  output voltages.

The bandwidths are approximatively 8MHz at  $100V_{pp}$  and up to 10MHz at  $50V_{pp}$ .

#### V.2.2.2 - Crosstalk

The curves Figures 25, 26 and 27 show the crosstalk for this application. The crosstalk is almost the same for the six different combinations of the three channels. The worst value is -24dB at 5MHz.

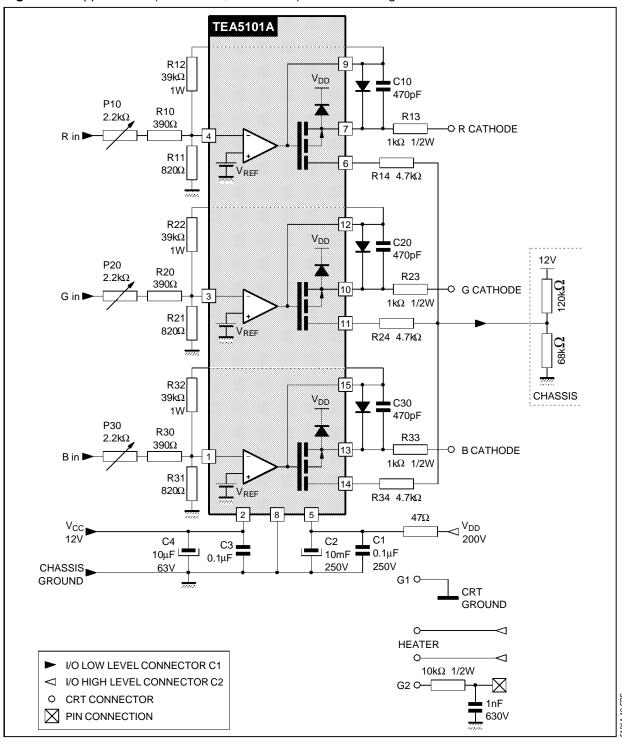


Figure 17: Application 1 (45AX Tube, TDA3562A) - Electrical Diagram

**TEA5101A** R12  $39k\Omega$  $V_{DD}$ **■** C10 1W 1nF P10 R10  $2.2k\Omega$ R13  $390\Omega$ R CATHODE 1kΩ 1/2W R11 R CUT-OFF  $820\Omega$  $\sum V_{REF}$ R14  $4.7k\Omega$ R15 100kΩ R22  $39k\Omega$  $V_{DD}$ C20 1W 1nF P20 R20 R23  $2.2k\Omega$ 390Ω G CATHODE 1kΩ 1/2W R21 ► G CUT-OFF 820Ω  $\sum \mathsf{V}_{\mathsf{REF}}$ R24  $4.7k\Omega$ R25 100kΩ R32  $39k\Omega$  $V_{DD}$ **C**30 1W 1nF P30 R30 R33  $2.2k\Omega$  $390\Omega$ OB CATHODE 1kΩ 1/2W R31 ► B CUT-OFF 820W  $V_{\mathsf{REF}}$ R34  $4.7k\Omega$ R35  $100k\Omega$  $47\Omega$  $V_{CC}$  $V_{DD}$ 12V C4 C2 C1 200V C3 **•** = 0.1μF 10μF L 0.1μF **T** 🖵 10μF 63V 250V CHASSIS 250V GROUND G1 ♀ CRT GROUND **HEATER** R1 100kΩ I/O LOW LEVEL CONNECTOR C1 10kΩ 1/2W ✓ I/O HIGH LEVEL CONNECTOR C2 G2 🗢 CRT CONNECTOR 2 x 22nF PIN CONNECTION 630V

Figure 18: Application 2 (PIL24 Tube, TEA5031D) - Electrical Diagram

**COMPONENT SIDE** 4R7 — 0.1µ 250V G2 22n/630 22n/630 VDD HEATER HEATER 100K 1/2W 2K2 G INPUT 12V B INPUT GND R INPUT R CUTOFF B CUTOFF G CUTOFF **COPPER SIDE** TEA 5101 A डा

Figure 19: TEA5101A Evaluation Board Layout and Components View

**TEA5101A** R12  $39k\Omega$  $V_{DD}$ **C**10 1W 1nF P10 R10 R13  $2.2k\Omega$ 390Ω R CATHODE 1kΩ 1/2W R11 R CUT-OFF  $1.5 k\Omega$  $\prod V_{\mathsf{REF}}$ R14  $4.7k\Omega$ R15 120kΩ R22  $39 \mathrm{k}\Omega$  $V_{DD}$ C20 1W 1nF P20 R20 R23  $2.2k\Omega$  $390\Omega$ G CATHODE  $1k\Omega$  1/2W R21 G CUT-OFF  $1.5 k\Omega$  $\prod \mathsf{V}_{\mathsf{REF}}$ R24 4.7kΩ R25 120kΩ R32  $39k\Omega$  $V_{DD}$ **C**30 1W P30 R30 R33  $2.2k\Omega$  $390\Omega$ ○ B CATHODE 1kΩ 1/2W R31 ► B CUT-OFF  $1.5k\Omega$  $V_{\mathsf{REF}}$ R34  $4.7k\Omega$ R35  $120k\Omega$  $47\Omega$  $V_{CC}$  $V_{DD}$ 12V C4 C2 C1 0.1μF 200V C3 10μF 📥 0.1μF **T** 10μF 250V 63V CHASSIS 250V G1 ♀ **GROUND** CRT GROUND **HEATER** R1  $100k\Omega$ I/O LOW LEVEL CONNECTOR C1  $10k\Omega$  1/2W ✓ I/O HIGH LEVEL CONNECTOR C2 G2 ○—[ CRT CONNECTOR 2 x 22nF = 2 x 22 = 630V N PIN CONNECTION

Figure 20: TEA5101A Evaluation Board Electrical Schematic Diagram

Figure 21: Bandwidth Measurement Configuration

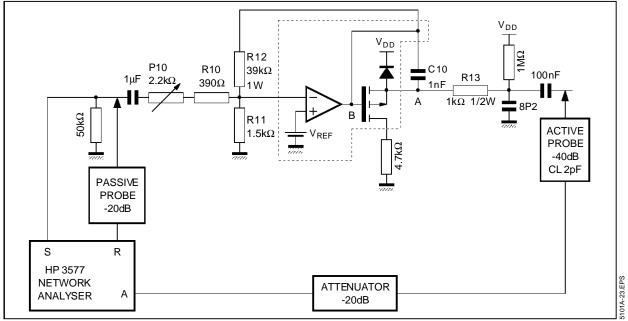


Figure 22: Crosstalk Measurement Configuration

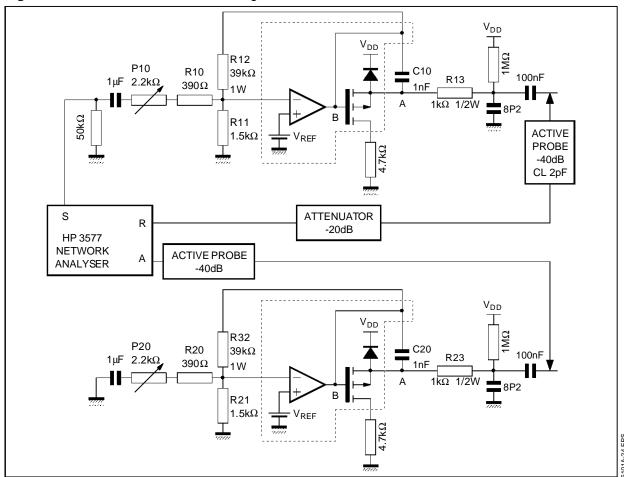


Figure 23: Frequency Response of R Channel (100V<sub>PP</sub>)

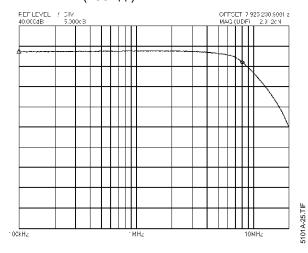


Figure 25: Crosstalk between R Channel and G and B Ones

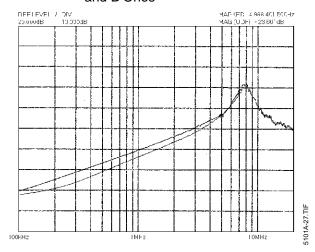


Figure 24: Frequency Response of R Channel (50V<sub>PP</sub>)

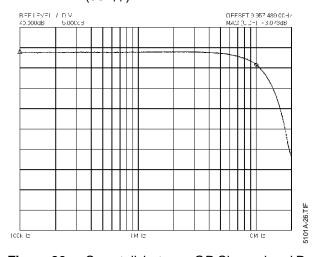


Figure 26: Crosstalk between GR Channel and R and B Ones

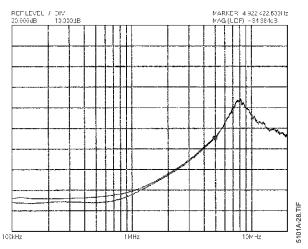
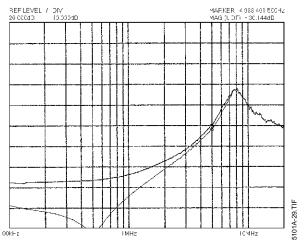


Figure 27: Crosstalk between B Channel and R and G Ones



#### V.2.2.3 - Transition times

The curves Figure 28 show respectively the R, G, B rise and fall times of respectively 49ns and 48ns with a  $100V_{pp}$  output voltage (between 50 and 150V).

The difference between rise times of the three channels is less than 1ns.

The difference between fall times of the three channels is less than 2ns.

The delay time at rising output is 48ns.

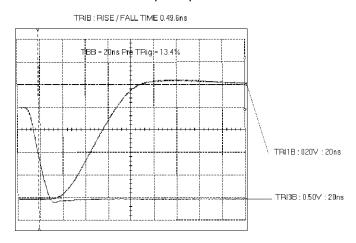
The delay time at falling output is 50ns.

The difference between the delay times is less than 2ns.

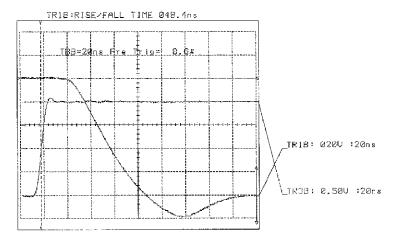
The slew rate is about 2000V/μs.

These results verify the high performance available from the TEA 5101A video amplifier which make it very suitable for high end applications.

Figures 28A and 28B: TEA5101AR Channel Step Response







5101A-31.TIF

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