DATA SHEET

TDA9829T
Downconverter for DVB

Product specification
File under Integrated Circuits, IC02

1998 Nov 09

Philips
Semiconductors

PHILIPS

FEATURES

- 5 V supply voltage
- Gain controlled IF-amplifier
- Mixer for DVB-IF downconversion
- VCO for Quadrature Amplitude Modulation (QAM) carrier recovery
- External VCO control
- Internal and external AGC
- DVB output level adjust via AGC adjust
- High level DVB operational output amplifier
- Mute switch for DVB output
- Tuner AGC with adjustable takeover point (TOP)
- AFC detector without extra reference circuit
- Stabilizer circuit for ripple rejection and to achieve constant output signals.

GENERAL DESCRIPTION

The TDA9829T is an integrated circuit for DVB-IF processing.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	note 1	4.5	5.0	5.5	V
I_P	supply current		81	96	111	mA
$V_{3\text{-}4(rms)}$	input sensitivity (RMS value)	–1 dB DVB signal at output	–	100	150	µV
$\Delta\varphi_{SSB}$	VCO phase noise	f = 100 kHz; free-running	103	107	–	dBc/Hz
α_{mute}	mute attenuation	note 2	–	36	–	dB
$I_{12(sink)}$	sink current	maximum tuner gain reduction; see Fig.3	1.5	2	2.6	mA
$CR_{stps(US)}$	control steepness $\Delta I_{14}/\Delta f_{IF}$ for USA	f_{IF} = 43.75 MHz; notes 3 and 4; see Fig.4	0.7	0.98	1.3	µA/kHz
$V_{11(p\text{-}p)}$	output voltage (peak-to-peak value)	C_L < 15 pF; R_L > 5 kΩ; with internal AGC	1.8	2.1	2.4	V
B_{-1dB}	–1 dB bandwidth	C_L < 15 pF; R_L > 5 kΩ	11	12	–	MHz
α_H	suppression of in-band harmonics	V_o = 2.0 V (p-p)	30	35	–	dB
PSRR	power supply ripple rejection at pin 11	see Fig.5	26	36	–	dB

Notes

1. Performance may be decreased at V_P = 4.5 V.
2. This parameter is not tested during production and is only given as application information for designing the television receiver.
3. To match the AFC output signal to different tuning systems a current source output is provided. The test circuit is given in Fig.4. The AFC-steepness can be changed by the resistors at pin 14.
4. Depending on the ratio $\Delta C/C_0$ of the LC resonant circuit of VCO ($Q_0 > 50$; $C_0 = C_{int} + C_{ext}$; see Table 2).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9829T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

BLOCK DIAGRAM

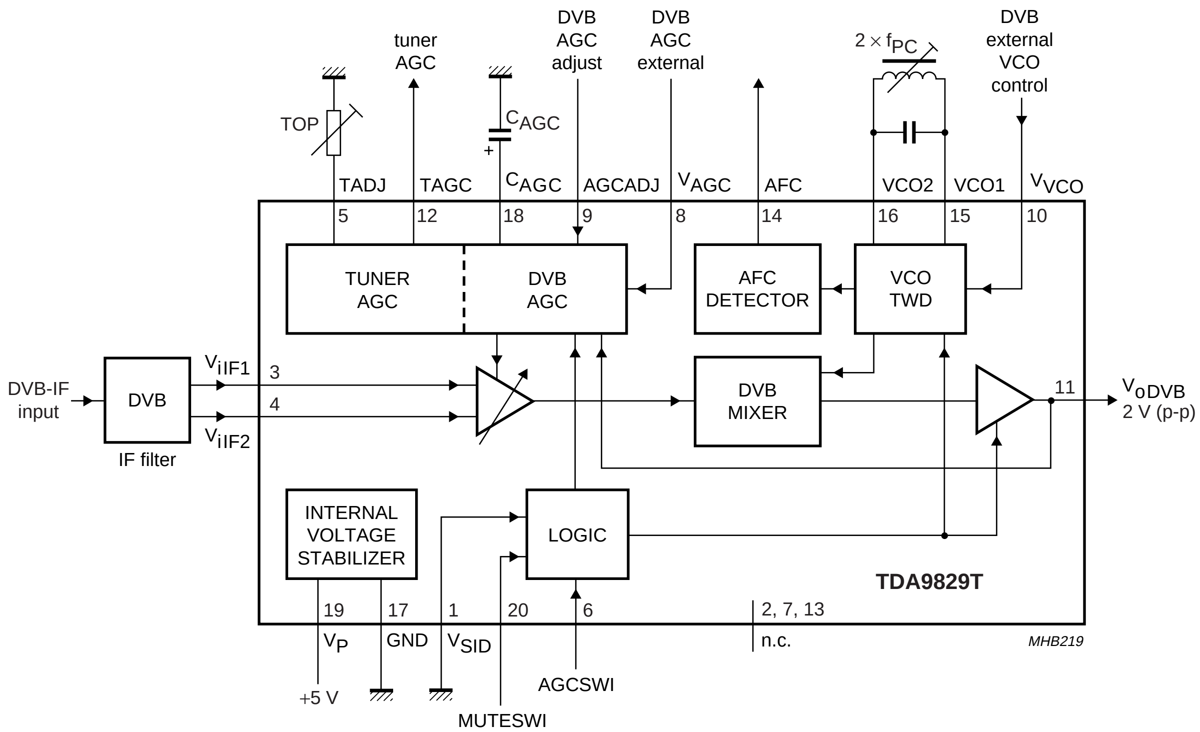


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{SID}	1	SIF down input
n.c.	2	not connected
V_{iIF1}	3	IF differential input signal voltage 1
V_{iIF2}	4	IF differential input signal voltage 2
TADJ	5	tuner AGC takeover adjust (TOP)
AGCSWI	6	AGC switch input
n.c.	7	not connected
V_{AGC}	8	AGC voltage input
AGCADJ	9	AGC adjust input
V_{VCO}	10	VCO control voltage
V_{oDVB}	11	DVB output
TAGC	12	tuner AGC output
n.c.	13	not connected
AFC	14	AFC output
VCO1	15	VCO1 reference circuit
VCO2	16	VCO2 reference circuit
GND	17	ground
C_{AGC}	18	AGC capacitor
V_P	19	supply voltage (+5 V)
MUTESWI	20	mute switch input

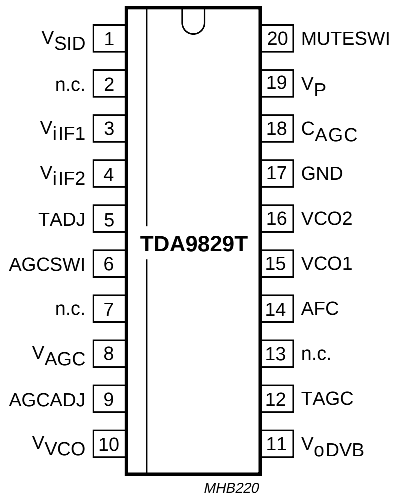


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Vision IF amplifier

The vision IF amplifier consists of three AC-coupled differential amplifier stages. Each differential stage comprises a feedback network controlled by emitter degeneration to control the IF gain.

VCO, Travelling Wave Divider (TWD) and AFC

The VCO operates with a resonance circuit (with L and C in parallel) at double the IF frequency plus symbol frequency. The VCO is controlled by integrated variable capacitors. The control voltage required to tune the VCO from its free-running frequency to its actual frequency is fed to the capacitors. This control voltage is amplified and converted into a current which represents the AFC output signal. At centre frequency the AFC output current is equal to zero.

The oscillator signal is divided-by-two with a TWD which generates a differential output signal for downconverting the IF signal.

DVB mixer

The gain controlled DVB-IF signal is downconverted to the symbol frequency by use of a four quadrant multiplier. The conversion signal is provided by the VCO and TWD.

DVB AGC and tuner AGC

The AGC detector charges/discharges the AGC capacitor to the required voltage for setting the IF and tuner gain in order to keep the DVB signal at a constant level.

A peak detector is used for the DVB AGC. The peak value of (digital) the QAM signal is detected and controlled to a constant value by the variable gain IF amplifier.
The detector bandwidth is adapted to the symbol frequency (3 to 11 MHz). The external AGC time constant is given by the IF AGC capacitor at pin 18.

The AGC capacitor voltage is transferred to an internal IF control signal, and is fed to the tuner AGC to generate the tuner AGC output current (open-collector output).
The tuner AGC takeover point can be adjusted. This allows the tuner and the SWIF filter to be matched to achieve the optimum IF input level.

The DVB output signal (V_{oDVB}) can be adjusted in a range of ±3 dB by a control voltage (ΔV_{adj}) at pin 9. The internal AGC can be switched off at pin 6 and the IF gain can be controlled by an external voltage at pin 8. The tuner AGC is active in both instances.

DVB output amplifier

The output amplifier for the DVB signal has a high bandwidth and delivers a 2 V (p-p) signal. The amplifier can be switched to a mute state forced by the signal at pin 20.

Internal voltage stabilizer

A band gap circuit internally generates a voltage of approximately 1.25 V, independent of supply voltage and temperature. A voltage regulator circuit, connected to this voltage, produces a constant voltage of 3.6 V which is used as an internal reference voltage.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage (pin 19)	maximum chip temperature of 125 °C	0	5.5	V
V_n	voltage at pins 1 to 10, 13, 14 and 18 to 20		0	V_P	V
$t_{sc(max)}$	maximum short-circuit time		–	10	s
V_{12}	tuner AGC output voltage		0	13.2	V
T_{stg}	storage temperature		–25	+150	°C
T_{amb}	operating ambient temperature		–20	+70	°C
V_{es}	electrostatic handling voltage	machine model class B	–300	+300	V

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	85	K/W

CHARACTERISTICS

V_P = 5 V; T_{amb} = 25 °C; see Table 1 for input frequencies; input level $V_{iIF(3–4)}$ = 10 mV (RMS value); measurements taken in Fig.8; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin 19)						
V_P	supply voltage	note 1	4.5	5.0	5.5	V
I_P	supply current		81	96	111	mA
IF amplifier (measured at f_{IF} = 43.75 MHz; pins 3 and 4)						
$\Delta V_{(3-4)(rms)}$	input sensitivity (RMS value)	–1 dB DVB signal at output	–	100	150	μV
$V_{i(3-4)(rms)}$	maximum input signal level (RMS value)	1 dB DVB signal at output	140	200	–	mV
ΔG_{IF}	total gain control IF amplifier		59	64	–	dB
	tilt for Δf ±3 MHz	f_s = 6.9 MHz; 40 dB gain	–	0.5	1	dB
$R_{i(3-4)(diff)}$	input resistance (differential)	note 2	–	2.2	–	kΩ
$C_{i(3-4)(diff)}$	input capacitance (differential)	note 2	–	1.7	–	pF
DVB mixer and VCO (pins 10, 15 and 16); see notes 4 and 5 and Table 1						
$f_{VCO(max)}$	maximum oscillator frequency	$2(f_{IF} + f_s)$	125	130	–	MHz
$f_{VCO(US)}$	VCO frequency for USA	$2(f_{IF} + f_s)$	–	97.5	–	MHz
$f_{VCO(EU)}$	VCO frequency for Europe	$2(f_{IF} + f_s)$	–	86.0	–	MHz
$V_{ref(rms)}$	oscillator voltage swing between pins 15 and 16 (RMS value)		–	60	–	mV
$\Delta\varphi_{SSB}$	VCO phase noise	f = 100 kHz; free-running	103	107	–	dBc/Hz
V_{VCO}	VCO control range (pin 10)	see Figs 6 and 7	0	–	V_P	V
$R_{i(VCO)}$	VCO control input resistance (pin 10)		50	63	76	kΩ
$CR_{stps(VCO)}$	control steepness $\Delta f_s/\Delta V_{10}$	see Figs 6 and 7				
		DVB (USA)	–	0.29	–	MHz/V
		DVB (Europe)	–	0.40	–	MHz/V
DVB output amplifier (pins 11 and 20)						
$V_{o(DVB)(p-p)}$	DVB output signal (QAM) (peak-to-peak value)		1.8	2.1	2.4	V
$I_{bias(int)}$	DC internal bias current for emitter-follower (pin 11)		1.9	2.3	2.7	mA
$I_{sink(max)}$	maximum AC and DC output sink current (pin 11)		1.5	–	–	mA
$I_{source(max)}$	maximum AC and DC output source current (pin 11)		2.0	–	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
α_{mute}	mute attenuation	note 2	–	36	–	dB
$V_{i(mute)}$	mute switch input voltage (pin 20)	DVB mute; note 3	1.3	–	V_P	V
		DVB no mute	0	–	0.8	V
I_{IL}	LOW-level input current (pin 20)	V_{20} = 0 V	180	230	280	μA
DVB AGC detector (pins 8, 9 and 18)						
t_{resp}	response to an increasing amplitude step in the IF input signal	note 6	–	0.25	–	ms/dB
	response to a decreasing amplitude step in the IF input signal	note 6	–	0.25	–	ms/dB
I_{ch}	charging current (pin 18)		–	200	–	μA
I_{dch}	discharging current (pin 18)		–	200	–	μA
$\Delta V_{i(AGC)}$	AGC adjust input voltage range (pin 9)		1	2.5	4.5	V
$\Delta R_{i(AGC)}$	AGC adjust input resistance (pin 9)		8	10	12	kΩ
ΔAGC_{stps}	AGC adjust steepness	2 V < V_9 < 3 V	–	–5	–	dB/V
$V_{AGC(ext)}$	external AGC voltage for DVB (pin 8)	see Fig.3	1	–	4.5	V
$R_{i(AGC)(ext)}$	external AGC input resistance (pin 8)		40	–	–	kΩ
Tuner AGC (pin 12)						
$V_{i(min)(rms)}$	IF input signal voltage for minimum starting point of tuner takeover (RMS value)	input at pins 3 and 4; R_{TOP} = 22 kΩ; I_{TAGC} = 0.4 mA	–	2	5	mV
$V_{i(max)(rms)}$	IF input signal voltage for maximum starting point of tuner takeover (RMS value)	input at pins 3 and 4; R_{TOP} = 0 Ω; I_{TAGC} = 0.4 mA	50	100	–	mV
V_o	permissible output voltage	from external source; note 2	–	–	13.2	V
V_{sat}	saturation voltage	I_{TAGC} = 1.5 mA	–	–	0.2	V
$\frac{\Delta V_{TOP,12}}{\Delta T}$	variation of takeover point by temperature	I_{TAGC} = 0.4 mA	–	0.03	0.07	dB/K
I_{sink}	sink current	see Fig.3				
		no tuner gain reduction; V_{TAGC} = 13.2 V	–	–	5	μA
		maximum tuner gain reduction	1.5	2	2.6	mA

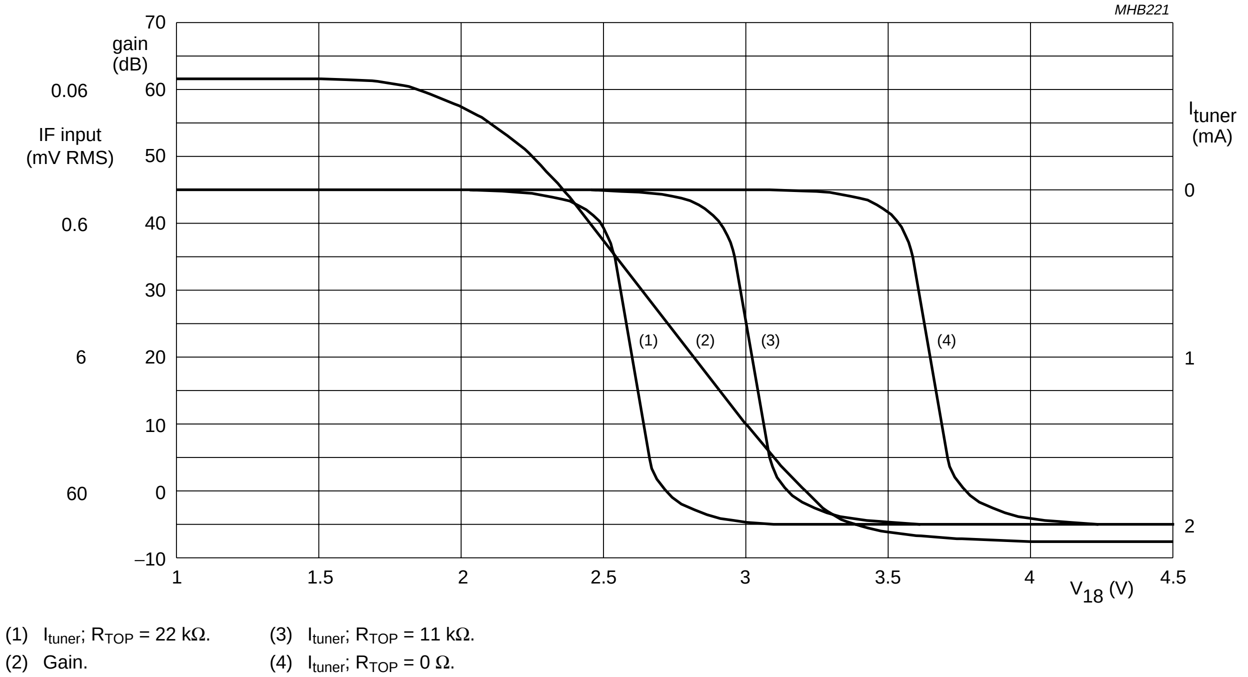
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔG_{IF}	IF slip by automatic gain control	tuner gain current from 20 to 80%	–	6	8	dB
AFC circuit (pin 14); see notes 7 and 8 and Fig.4						
$CR_{stps(US)}$	control steepness $\Delta I_{14}/\Delta f_{IF}$ for USA	f_{IF} = 43.75 MHz	0.7	0.98	1.3	μA/kHz
$CR_{stps(EU)}$	control steepness $\Delta I_{14}/\Delta f_{IF}$ for Europe	f_{IF} = 36.15 MHz	0.45	0.70	0.95	μA/kHz
DVB output signal (IF input to DVB output)						
$V_{o(p-p)}$	output voltage (pin 11) (peak-to-peak value)	C_L < 15 pF; R_L > 5 kΩ; with internal AGC	1.8	2.1	2.4	V
$V_{O(DC)}$	DC output voltage		–	2.5	–	V
B_{-1dB}	–1 dB bandwidth	C_L < 15 pF; R_L > 5 kΩ	11	12	–	MHz
B_{-3dB}	–3 dB bandwidth		–	17	–	MHz
$\alpha_{C(DVB)}$	fundamental input signal and IF harmonics		35	40	–	dB
α_H	suppression of in-band harmonics	V_o = 2.0 V (p-p)	30	35	–	dB
PSRR	power supply ripple rejection at pin 11	see Fig.5	26	36	–	dB

Notes

1. Performance may be decreased at V_P = 4.5 V.
2. This parameter is not tested during production and is only given as application information for designing the television receiver.
3. Mute state also can be achieved by leaving pin 20 open-circuit.
4. Resonance circuit of VCO: Q_0 > 50; C_{ext}, C_{int} and L see Table 2.
5. Temperature coefficient of external LC-circuit is equal to zero.
6. Response speed valid for an IF input level range of 200 μV up to 70 mV.
7. To match the AFC output signal to different tuning systems a current source output is provided. The test circuit is given in Fig.4. The AFC steepness can be changed by the resistors at pin 14.
8. Depending on the ratio $\Delta C/C_0$ of the LC resonant circuit of VCO (Q_0 > 50; $C_0 = C_{int} + C_{ext}$; see Table 2).

Table 1 Input frequencies, symbol frequencies and VCO frequencies

SYMBOL	DESCRIPTION	DVB (Europe)	DVB (USA)	UNIT
f_s	Symbol frequency	6.9	5.0	MHz
f_{IF}	IF frequency	36.15	43.75	MHz
f_{VCO}	VCO frequency	86.0	97.5	MHz



(1) I_{tuner}; R_{TOP} = 22 kΩ.
(2) Gain.
(3) I_{tuner}; R_{TOP} = 11 kΩ.
(4) I_{tuner}; R_{TOP} = 0 Ω.

Fig.3 Typical IF and tuner AGC characteristic.

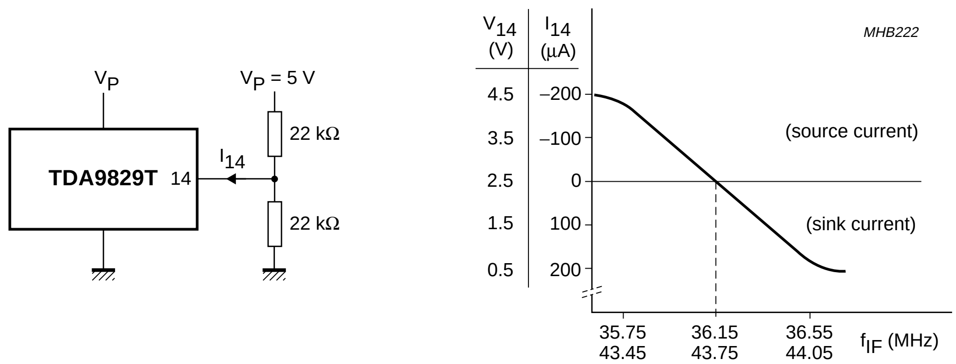


Fig.4 Measurement conditions and typical AFC characteristic.

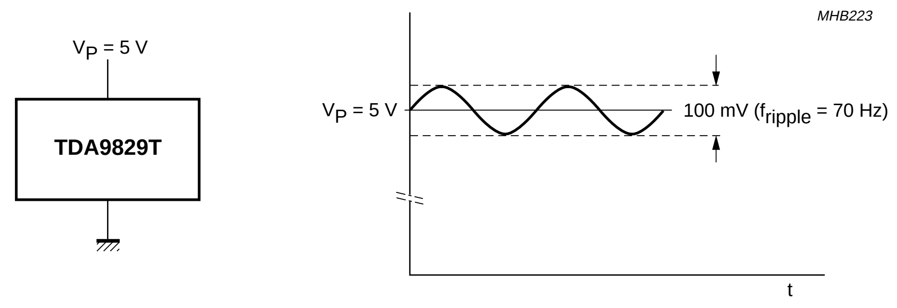


Fig.5 Ripple rejection condition.

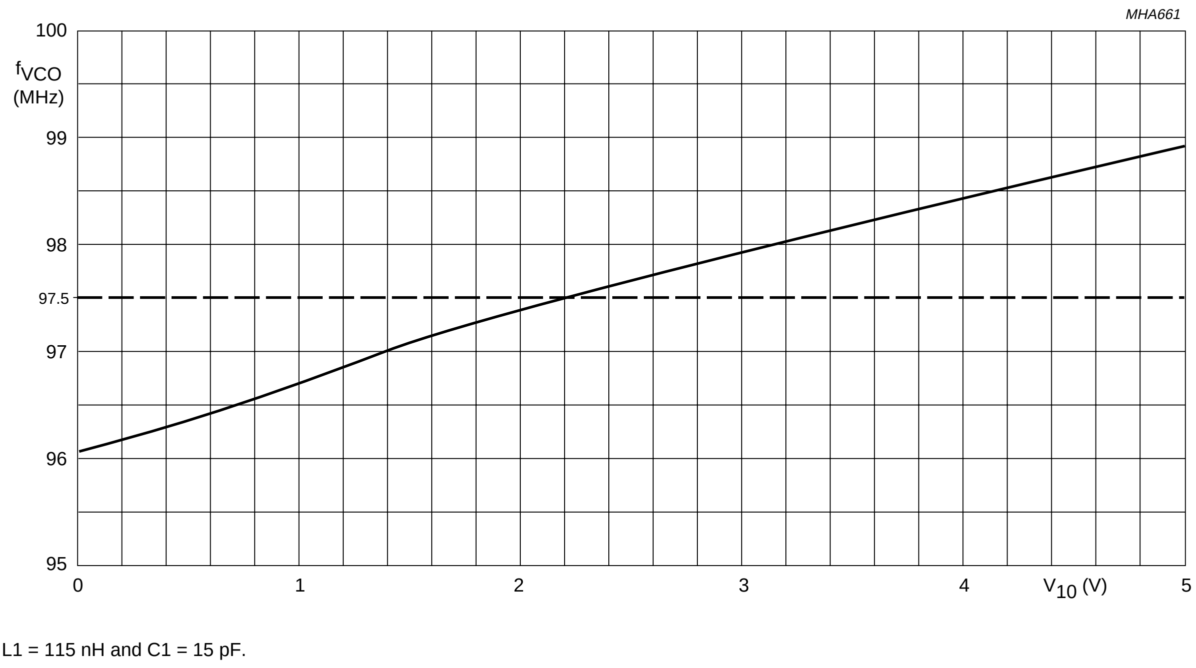
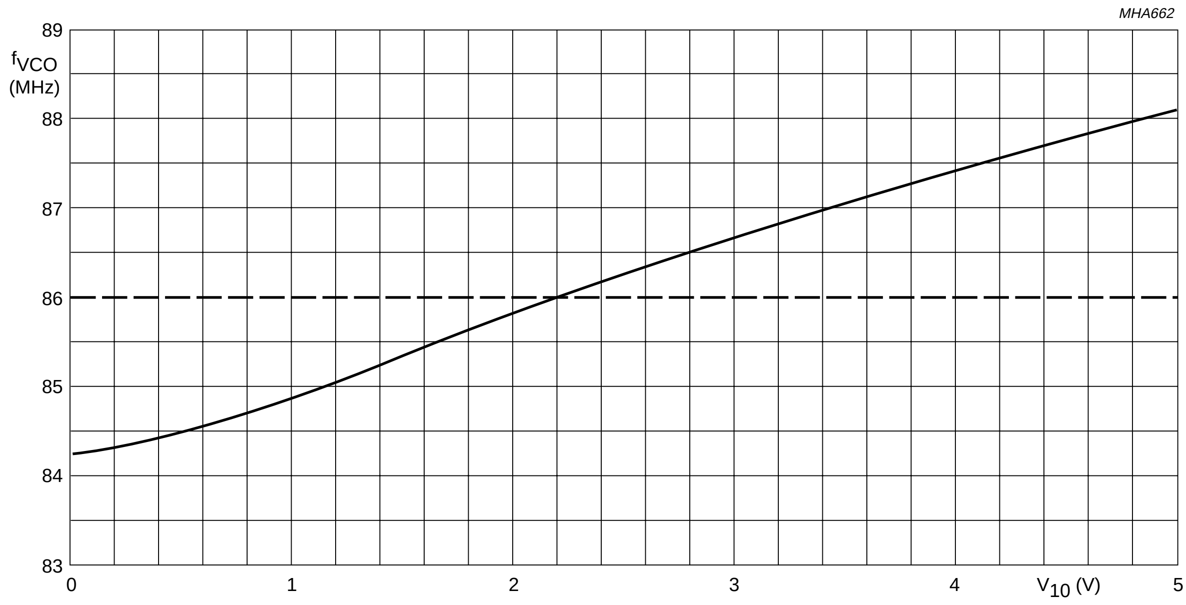


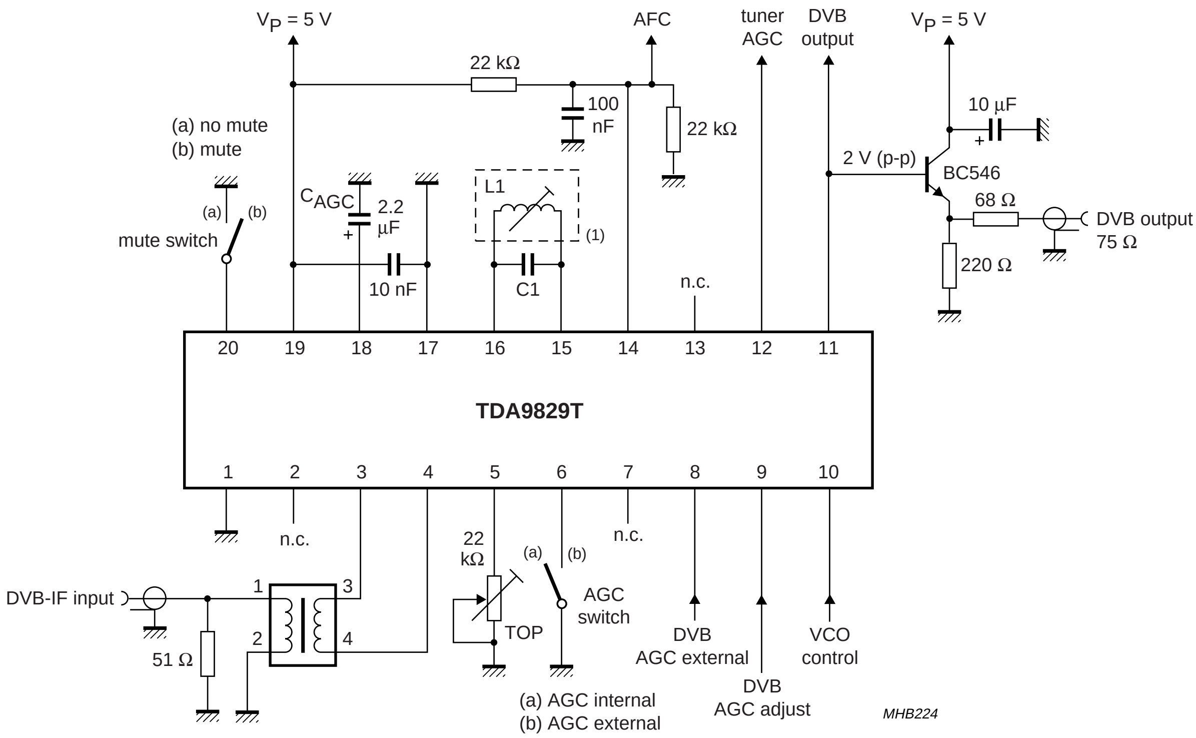
Fig.6 VCO control characteristic for DVB (USA).



L1 = 248 nH and C1 = 5.6 pF.

Fig.7 VCO control characteristic for DVB (Europe).

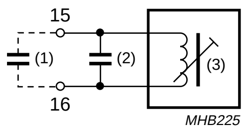
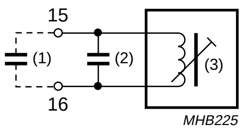
TEST CIRCUIT



(1) See Table 2.

Fig.8 Test circuit.

Table 2 Test circuit values

PARAMETER	Europe	USA
IF frequency	36.15 MHz	43.75 MHz
VCO frequency	86.0 MHz	97.5 MHz
Oscillator circuit	 (1) C(VCO) = 8.2 pF. (2) C1 = 5.6 pF. (3) L1 = 248 nH.	 (1) C(VCO) = 8.2 pF. (2) C1 = 15 pF. (3) L1 = 115 nH.
Toko coil	5KM 369SNS - 2010Z	5KM 369SNS - 1647Z
Philips ceramic capacitor	2222 632 39478	2222 632 33129

INTERNAL PIN CONFIGURATIONS

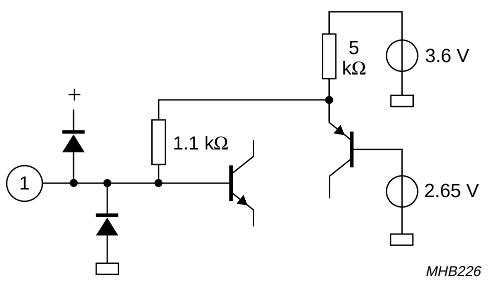


Fig.9 Pin 1; V_{SID}.

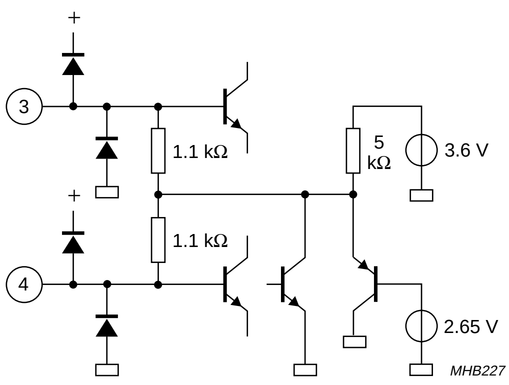


Fig.10 Pin 3; V_{iIF1} and pin 4; V_{iIF2}.

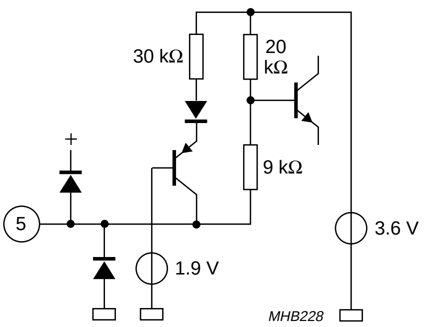


Fig.11 Pin 5; TADJ.

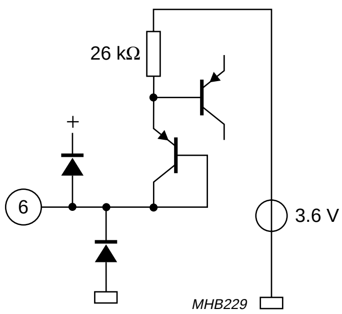


Fig.12 Pin 6; AGCSWI.

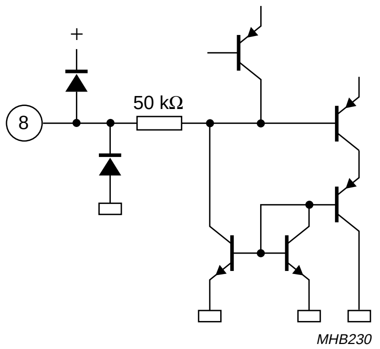


Fig.13 Pin 8; V_{AGC}.

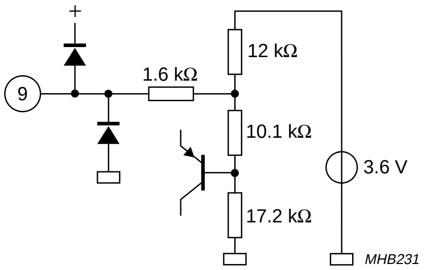


Fig.14 Pin 9; AGCADJ.

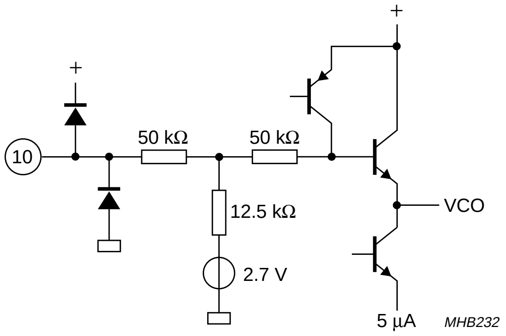


Fig.15 Pin 10; V_{VCO}.

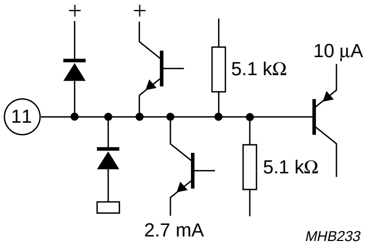


Fig.16 Pin 11; V_{oDVB}.

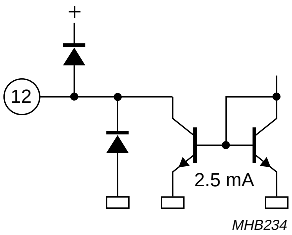


Fig.17 Pin 12; TAGC.

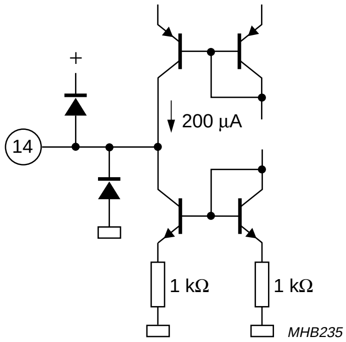


Fig.18 Pin 14; AFC.

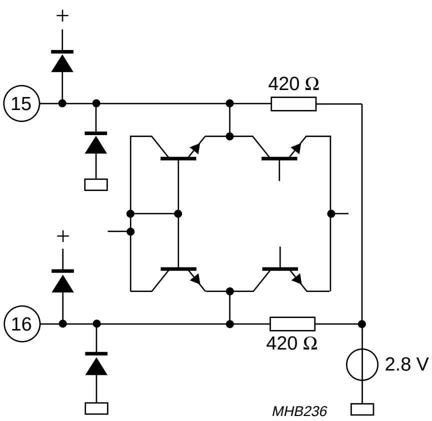


Fig.19 Pin 15; VCO1 and pin 16; VCO2.

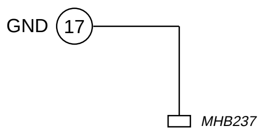


Fig.20 Pin 17; GND.

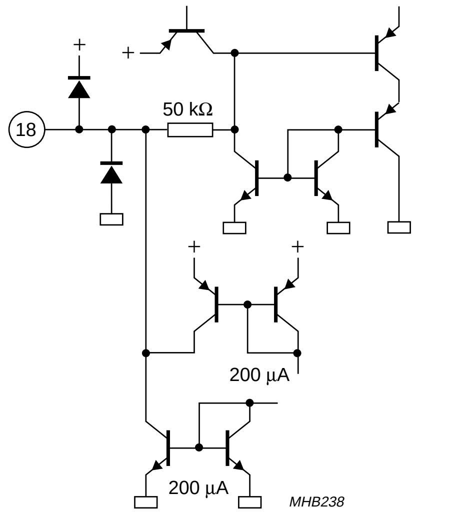


Fig.21 Pin 18; C_{AGC}.

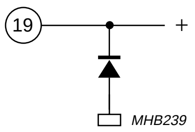


Fig.22 Pin 19; V_P.

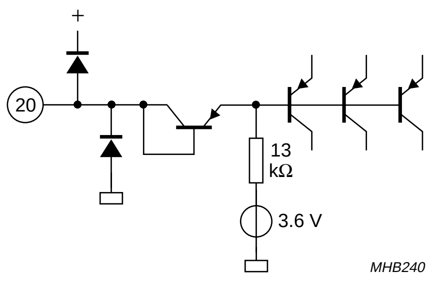
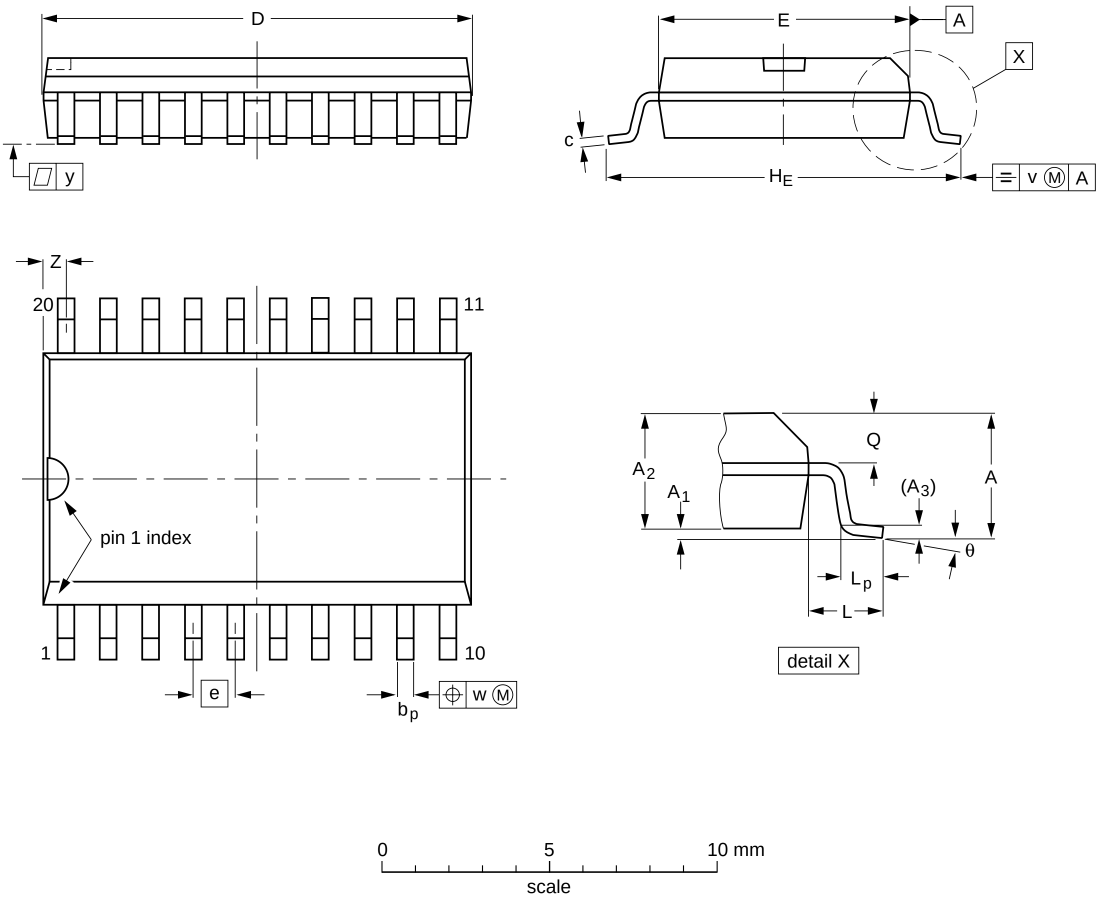


Fig.23 Pin 20; MUTESWI.

PACKAGE OUTLINE

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~95-01-24~~ 97-05-22

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
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Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
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Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113, Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 160 1010, Fax. +43 160 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6, 220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

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Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor, 51 James Bourchier Blvd., 1407 SOFIA, Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS, Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre, 72 Tat Chee Avenue, Kowloon Tong, HONG KONG, Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S, Tel. +45 32 88 2636, Fax. +45 31 57 0044

Finland: Sinikalliontie 3, FIN-02630 ESPOO, Tel. +358 9 615800, Fax. +358 9 61580920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex, Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG, Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS, Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor, 254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025, Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division, Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510, Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14, Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053, TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3, 20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL, Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR, Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905, Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB, Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND, Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO, Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc., 106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI, Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA, Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW, Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762, Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

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South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale, 2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000, Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Al. Vicente Pinzon, 173, 6th floor, 04547-130 SÃO PAULO, SP, Brazil, Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA, Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM, Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH, Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1, TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd., 209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260, Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL, Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7, 252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes, MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409, Tel. +1 800 234 7381

Uruguay: see South America

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Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD, Tel. +381 11 625 344, Fax.+381 11 635 777

For all other countries apply to: Philips Semiconductors, International Marketing & Sales Communications, Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

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