INTEGRATED CIRCUITS



Preliminary specification File under Integrated Circuits, IC02 1995 Sep 05



TDA9806

FEATURES

- 5 V supply voltage
- Gain controlled wide band VIF-amplifier (AC-coupled)
- True synchronous demodulation with active carrier regeneration (very linear demodulation, good intermodulation figures, reduced harmonics, excellent pulse response)
- Separate video amplifier for sound trap buffering with high video bandwidth
- VIF AGC detector for gain control, operating as peak sync detector for B/G
- Tuner AGC with adjustable takeover point (TOP)
- AFC detector without extra reference circuit
- AC-coupled limiter amplifier for sound intercarrier signal
- Alignment-free FM-PLL demodulator with high linearity, switchable de-emphasis for FM
- Stabilizer circuit for ripple rejection and to achieve constant output signals.

GENERAL DESCRIPTION

The TDA9806 is an integrated circuit for multistandard vision IF signal processing and FM sound demodulation in TV and VCR sets.

		PACKAGE			
TYPE NUMBER NAME		DESCRIPTION	VERSION		
TDA9806	SDIP32	plastic shrink dual in-line package; 32 leads (400 mil)	SOT232-1		

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QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VP	supply voltage		4.5	5	5.5	V
I _P	supply current		82	96	110	mA
V _{i VIF(rms)}	vision IF input signal voltage sensitivity (RMS value)	-1 dB video at output	-	60	100	μV
V _{o CVBS (p-p)}	CVBS output signal voltage (peak-to-peak value)		1.7	2.0	2.3	V
B_3	-3 dB video bandwidth on pin CVBS	B/G standard; C _L < 20 pF; R _L > 1 kΩ; AC load	7	8	-	MHz
S/N (W)	weighted signal-to-noise ratio for video		56	60	_	dB
$IM_{\alpha 1.1}$	intermodulation attenuation at 'blue'	f = 1.1 MHz	58	64	-	dB
IM _{α3.3}	intermodulation attenuation at 'blue'	f = 3.3 MHz	58	64	_	dB
α _{H(sup)}	suppression of harmonics in video signal		35	40	-	dB
V _{o(rms)}	audio output signal voltage for FM (RMS value)	B/G standard; 54% modulation	-	0.5	-	V
THD	total harmonic distortion for FM	54% modulation	-	0.15	0.5	%
S/N (W)	weighted signal-to-noise ratio for FM	54% modulation	-	60	_	dB

BLOCK DIAGRAM



PINNING

SYMBOL	PIN	DESCRIPTION
V _{i VIF1}	1	VIF differential input signal voltage 1
V _{i VIF2}	2	VIF differential input signal voltage 2
n.c.	3	not connected
n.c.	4	not connected
n.c.	5	not connected
TADJ	6	tuner AGC takeover adjust (TOP)
T _{PLL}	7	PLL loop filter
n.c.	8	not connected
n.c.	9	not connected
V _{o CVBS}	10	CVBS output signal voltage
n.c.	11	not connected
V _{o AF}	12	audio voltage frequency output
DEEMI	13	de-emphasis input
DEEMO	14	de-emphasis output
C _{DEC}	15	decoupling capacitor
n.c.	16	not connected
V _{i FM}	17	sound intercarrier input voltage
n.c.	18	not connected
TAGC	19	tuner AGC output
V _{o(int)}	20	sound intercarrier output voltage
V _{o(vid)}	21	composite video output voltage
V _{i(vid)}	22	video buffer input voltage
AFC	23	AFC output
VCO1	24	VCO1 reference circuit for 2f _{PC}
VCO2	25	VCO2 reference circuit for 2f _{PC}
C _{ref}	26	$1/_2V_P$ reference capacitor
GND	27	ground
C _{VAGC}	28	VIF AGC capacitor
V _P	29	supply voltage
n.c.	30	not connected
n.c.	31	not connected
n.c.	32	not connected

V_{i VIF1} 1 32 n.c. V_{i VIF2} 2 31 n.c. n.c. 3 30 n.c. 29 V_P n.c. 4 n.c. 5 28 C_{VAGC} TADJ 6 27 GND T_{PLL} 7 26 C_{ref} 25 VCO2 n.c. 8 TDA9806 n.c. 9 24 VCO1 23 AFC Vo CVBS 10 22 V_{i(vid)} n.c. 11 21 Vo(vid) V_{0 AF} 12 DEEM | 13 20 V_{o(int)} DEEMO 14 19 TAGC C_{DEC} 15 18 n.c. 17 ^Vi FM n.c. 16 MHA053 Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Vision IF amplifier

The vision IF amplifier consists of three AC-coupled differential amplifier stages. Each differential stage comprises a feedback network controlled by emitter degeneration.

Tuner and VIF AGC

The AGC capacitor voltage is transferred to an internal IF control signal, and is fed to the tuner AGC to generate the tuner AGC output current (open-collector output). The tuner AGC takeover point can be adjusted. This allows the tuner and the SWIF filter to be matched to achieve the optimum IF input level.

The AGC detector charges/discharges the AGC capacitor to the required voltage for setting of VIF and tuner gain in order to keep the video signal at a constant level. Therefore for negative video modulation the sync level of the video signal is detected.

Frequency Phase Locked Loop detector (FPLL)

The VIF-amplifier output signal is fed into a frequency detector and into a phase detector via a limiting amplifier. During acquisition the frequency detector produces a DC current proportional to the frequency difference between the input and the VCO signal. After frequency lock-in the phase detector produces a DC current proportional to the phase difference between the VCO and the input signal. The DC current of either frequency detector or phase detector is converted into a DC voltage via the loop filter, which controls the VCO frequency.

VCO, travelling wave divider and AFC

The VCO operates with a resonance circuit (with L and C in parallel) at double the PC frequency. The VCO is controlled by two integrated variable capacitors. The control voltage required to tune the VCO from its free-running frequency to actually double the PC frequency is generated by the Frequency-Phase detector and fed via the loop filter to the first variable capacitor (FPLL). This control voltage is amplified and additionally converted into a current which represents the AFC output signal. At centre frequency the AFC output current is equal to zero.

The oscillator signal is divided-by-two with a Travelling Wave Divider (TWD) which generates two differential output signals with a 90 degree phase difference independent of the frequency.

Video demodulator and amplifier

The video demodulator is realized by a multiplier which is designed for low distortion and large bandwidth. The vision IF input signal is multiplied with the 'in-phase' signal of the travelling wave divider output.

The demodulator output signal is fed via an integrated low-pass filter for attenuation of the carrier harmonics to the video amplifier. The video amplifier is realized by an operational amplifier with internal feedback and high bandwidth. A low-pass filter is integrated to achieve an attenuation of the carrier harmonics. The video output signal is 1 V (p-p) for nominal vision IF modulation.

Video buffer

For an easy adaption of the sound traps an operational amplifier with internal feedback is used. This amplifier is featured with a high bandwidth and 7 dB gain. The input impedance is adapted for operating in combination with ceramic sound traps. The output stage delivers a nominal 2 V (p-p) positive video signal. Noise clipping is provided.

Intercarrier mixer

The intercarrier mixer is realized by a multiplier. The VIF amplifier output signal is fed to the intercarrier mixer and converted to intercarrier frequency by the regenerated picture carrier (VCO). The mixer output signal is fed via a high-pass for attenuation of the video signal components.

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Multistandard VIF-PLL and FM-PLL demodulator

FM detector

The FM detector consists of a limiter, an FM-PLL and an AF amplifier. The limiter provides the amplification and limitation of the FM sound intercarrier signal before demodulation. The result is high sensitivity and AM suppression. The amplifier consists of 7 stages which are internally AC-coupled in order to minimize the DC offset and to save pins for DC decoupling.

The FM-PLL consists of an integrated relaxation oscillator, an integrated loop filter and a phase detector. The oscillator is locked to the FM intercarrier signal, output from the limiter. As a result of locking, the oscillator frequency tracks with the modulation of the input signal and the oscillator control voltage is superimposed by the AF voltage. The FM-PLL operates as an FM-demodulator.

The AF amplifier consists of two parts:

- The AF preamplifier for FM sound is an operational amplifier with internal feedback, high gain and high common mode rejection. The AF voltage from the PLL demodulator, by principle a small output signal, is amplified by approximately 33 dB. The low-pass characteristic of the amplifier reduces the harmonics of the intercarrier signal at the sound output terminal, at which the de-emphasis network for FM sound is applied. An additional DC control circuit is implemented to keep the DC level constant, independent of process spread.
- The AF output amplifier (10 dB) provides the required output level by a rail-to-rail output stage. This amplifier makes use of an input selector for switching to FM de-emphasis or mute state, controlled by the mute switching voltage.

Internal voltage stabilizer and $\frac{1}{2}V_{P}$ -reference

The bandgap circuit internally generates a voltage of approximately 1.25 V, independent of supply voltage and temperature. A voltage regulator circuit, connected to this voltage, produces a constant voltage of 3.6 V which is used as an internal reference voltage.

For all audio output signals the constant reference voltage cannot be used because large output signals are required. Therefore these signals refer to half the supply voltage to achieve a symmetrical headroom, especially for the rail-to-rail output stage. For ripple and noise attenuation the $1/_2$ V_P voltage has to be filtered via a low-pass filter by using an external capacitor together with an integrated resistor (f_g = 5 Hz). For a fast setting to $1/_2$ V_P an internal start-up circuit is added.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _P	supply voltage (pin 29)	maximum chip temperature of 120 °C; note 1	0	5.5	V
Vi	voltage at pins 1 to 7, 12 to 19, 22, 23, 28 and 29		0	V _P	V
t _{s(max)}	maximum short-circuit time		-	10	S
V ₁₉	tuner AGC output voltage		0	13.2	V
T _{stg}	storage temperature		-25	+150	°C
T _{amb}	operating ambient temperature		-20	+70	°C
V _{es}	electrostatic handling voltage	note 2	-300	+300	V

Notes

1. $I_P = 110 \text{ mA}$; $T_{amb} = 70 \text{ °C}$; $R_{th j-a} = 60 \text{ K/W}$.

2. Charge device model class B: equivalent to discharging a 200 pF capacitor via a 0 Ω series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
R _{th j-a}	thermal resistance from junction to ambient in free air	60	K/W

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CHARACTERISTICS

 $V_P = 5 V$; $T_{amb} = 25 °C$; see Table 1 for input frequencies and level; input level $V_{i | F|1, 2} = 10 mV RMS$ value (sync-level for B/G); video modulation DSB; residual carrier B/G: 10%; video signal in accordance with *"CCIR, line 17"*; measurements taken in Fig.10; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin 2	29)		- 1	-1		
VP	supply voltage	note 1	4.5	5	5.5	V
l _P	supply current		82	96	110	mA
Vision IF am	plifier (pins 1 and 2)					
V _{i VIF(rms)}	input signal voltage sensitivity (RMS value)	B/G standard; –1 dB video at output	-	60	100	μV
V _{i max(rms)}	maximum input signal voltage (RMS value)	B/G standard; +1 dB video at output	120	200	_	mV
$\Delta V_{o(int)}$	internal IF amplitude difference between picture and sound carrier	within AGC range; B/G standard; ∆f = 5.5 MHz	-	0.7	1	dB
G _{IFcr}	IF gain control range	see Fig.3	65	70	_	dB
R _{i(diff)}	differential input resistance	note 2	1.7	2.2	2.7	kΩ
C _{i(diff)}	differential input capacitance	note 2	1.2	1.7	2.5	pF
V _{1,2}	DC input voltage		-	3.4	-	V
True synchro	onous video demodulator; note	3			•	
f _{VCO(max)}	maximum oscillator frequency for carrier regeneration	$f = 2f_{PC}$	125	130	_	MHz
$\Delta f_{osc} / \Delta T$	oscillator drift as a function of temperature	oscillator is free-running; I _{AFC} = 0; note 4	-	_	±20	ppm/K
V _{0 ref(rms)}	oscillator voltage swing at pins 24 and 25 (RMS value)	B/G standard	70	100	130	mV
f _{pcCR}	picture carrier capture range	B/G standard	±1.5	±2.0	_	MHz
t _{acq}	acquisition time	BL = 60 kHz; note 5	-	_	30	ms
Vi VIF(rms)	VIF input signal voltage sensitivity for PLL to be locked (RMS value; pins 1 and 2)	maximum IF gain; note 6	-	30	70	μV
I _{FPLL(offset)}	FPLL offset current at pin 7	note 7	-	-	±4.5	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Composite vi	deo amplifier (pin 21; sound ca	arrier off)		•		
Vo video(p-p)	output signal voltage (peak-to-peak value)	see Fig.7	0.88	1.0	1.12	V
V _{21(sync)}	sync voltage level	B/G standard	-	1.5	-	V
V _{21(clu)}	upper video clipping voltage level		V _P – 1.1	V _P – 1	-	V
V _{21(cll)}	lower video clipping voltage level		-	0.3	0.4	V
R _{0,21}	output resistance	note 2	-	-	10	Ω
I _{int 21}	internal DC bias current for emitter-follower		1.6	2.0	-	mA
I _{21 max(sink)}	maximum AC and DC output sink current		1.0	-	-	mA
I _{21 max(source)}	maximum AC and DC output source current		2.0	_	_	mA
B ₋₁	-1 dB video bandwidth	B/G standard; C _L < 50 pF; R _L > 1 kΩ; AC load	5	6	-	MHz
B ₋₃	-3 dB video bandwidth	B/G standard; C _L < 50 pF; R _L > 1 kΩ; AC load	7	8	-	MHz
α _H	suppression of video signal harmonics	$C_L < 50 \text{ pF}; R_L > 1 \text{ k}\Omega;$ AC load; note 8a	35	40	-	dB
PSRR	power supply ripple rejection at pin 21	video signal; grey level; B/G standard; see Fig.8	32	35	-	dB
CVBS buffer a	amplifier (only) and noise clipp	er (pins 10 and 22)				
R _{i,22}	input resistance	note 2	2.6	3.3	4.0	kΩ
C _{i,22}	input capacitance	note 2	1.4	2	3.0	pF
V _{I,22}	DC input voltage		1.5	1.8	2.1	V
G _v	voltage gain	B/G standard; note 9	6.5	7	7.5	dB
V _{10(clu)}	upper video clipping voltage level		3.9	4.0	-	V
V _{10(cll)}	lower video clipping voltage level		-	1.0	1.1	V
R _{0,10}	output resistance	note 2	-	-	10	Ω
I _{int 10}	DC internal bias current for emitter-follower		2.0	2.5	-	mA
I _{o,10 max(sink)}	maximum AC and DC output sink current		1.4	-	-	mA
I _{o,10} max(source)	maximum AC and DC output source current		2.4	-	-	mA
B ₋₁	-1 dB video bandwidth	B/G standard; C _L < 20 pF; R _L > 1 kΩ; AC load	8.4	11	-	MHz
B ₋₃	-3 dB video bandwidth	B/G standard; C _L < 20 pF; R _L > 1 kΩ; AC load	11	14	-	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Measuremen	ts from IF input to CVBS output	t (pin 10; 330 Ω between pin	s 21 and 2	22, sound	carrier of	f)
Vo CVBS(p-p)	CVBS output signal voltage on pin 10 (peak-to-peak value)	note 9	1.7	2.0	2.3	V
Vo CVBS(sync)	sync voltage level	B/G standard	-	1.35	-	V
ΔVo	deviation of CVBS output	50 dB gain control	-	-	0.5	dB
	signal voltage at B/G	30 dB gain control	-	-	0.1	dB
$\Delta V_{o(b BG)}$	black level tilt in B/G standard	gain variation; note 10	-	-	1	%
G _{diff}	differential gain	"CCIR, line 330"	-	2	5	%
Φdiff	differential phase	"CCIR, line 330"	-	1	2	deg
B ₋₁	-1 dB video bandwidth	B/G standard; C _L < 20 pF; R _L > 1 kΩ; AC load	5	6	-	MHz
B_3	-3 dB video bandwidth	B/G standard; C _L < 20 pF; R _L > 1 kΩ; AC load	7	8	-	MHz
S/N (W)	weighted signal-to-noise ratio	see Fig.4 and note 11	56	60	-	dB
S/N	unweighted signal-to-noise ratio	see Fig.4 and note 11	49	53	-	dB
ΙΜα _{1.1}	intermodulation attenuation at 'blue'	f = 1.1 MHz; see Fig.5 and note 12	58	64	-	dB
	intermodulation attenuation at 'yellow'	f = 1.1 MHz; see Fig.5 and note 12	60	66	-	dB
IMα _{3.3}	intermodulation attenuation at 'blue'	f = 3.3 MHz; see Fig.5 and note 12	58	64	-	dB
	intermodulation attenuation at 'yellow'	f = 3.3 MHz; see Fig.5 and note 12	59	65	-	dB
$\alpha_{c(rms)}$	residual vision carrier (RMS value)	B/G standard; fundamental wave and harmonics	-	2	5	mV
$\alpha_{H(sup)}$	suppression of video signal harmonics	note 8a	35	40	-	dB
$\alpha_{H(spur)}$	spurious elements	note 8b	40	-	-	dB
PSRR	power supply ripple rejection at pin 10	video signal; grey level; B/G standard; see Fig.8	25	28	-	dB
VIF-AFC dete	ector (pin 28)		,		-	
I ₂₈	charging current	B/G standard; note 10	0.75	1	1.25	mA
	discharging current	B/G standard	15	20	25	μA
t _{resp}	AGC response to an increasing VIF step	B/G standard; note 13	-	0.05	0.1	ms/dB
	AGC response to a decreasing VIF step	B/G standard	-	2.2	3.5	ms/dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Tuner AGC (pin 19)	•	ł	4	ļ	1
V _{i(rms)}	IF input signal voltage for minimum starting point of tuner takeover (RMS value)	input at pins 1 and 2; R _{TOP} = 22 k Ω ; I ₁₉ = 0.4 mA	-	2	5	mV
	IF input signal voltage for maximum starting point of tuner takeover (RMS value)	input at pins 1 and 2; R _{TOP} = 0 Ω ; I ₁₉ = 0.4 mA	50	100	5	mV
V _{0,19}	permissible output voltage	from external source; note 2	_	_	13.2	V
V _{sat,19}	saturation voltage	I ₁₉ = 1.5 mA	_	_	0.2	V
$\Delta V_{TOP,19} / \Delta T$	variation of takeover point by temperature	I ₁₉ = 0.4 mA	_	0.03	0.07	dB/K
I _{19(sink)}	sink current	no tuner gain reduction; see Fig.3				
		V ₁₉ = 12 V	_	_	2.5	μA
		V ₁₉ = 13.2 V	_	-	5	μA
		maximum tuner gain reduction	1.5	2	2.6	mA
ΔG_{IF}	IF slip by automatic gain control	tuner gain current from 20 to 80%	_	6	8	dB
AFC circuit (pin 23); see Fig.6 and note 14					•
S	control steepness $\Delta I_{23}/\Delta f$	note 15	0.5	0.72	1.0	μA/kHz
$\Delta f_{IF} / \Delta T$	frequency variation by temperature	$I_{AFC} = 0$; note 5	_	-	±20	ppm/K
V _{0,23}	output voltage upper limit	see Fig.6	V _P – 0.6	V _P - 0.3	-	V
	output voltage lower limit	see Fig.6	-	0.3	0.6	V
I _{o,23(source)}	output source current		150	200	250	μA
I _{o,23(sink)}	output sink current		150	200	250	μA
ΔI _{23(p-p)}	residual video modulation current (peak-to-peak value)	B/G standard	_	20	30	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Intercarrier n	nixer (B/G standard; pin 20)	1	ł	1	1	1
V _{o(rms)}	IF intercarrier level (RMS value)	SC	_	note 16	-	mV
B_3	-3 dB intercarrier bandwidth	upper limit	7.5	9	-	MHz
$\alpha_{c(rms)}$	residual sound carrier (RMS value)	fundamental wave and harmonics	_	2	-	mV
R _{0,20}	output resistance	note 2	_	-	25	Ω
V _{0,20}	DC output voltage		_	2.0	-	V
I _{int 20}	DC internal bias current for emitter-follower		1.5	1.9	-	mA
I _{20 max(sink)}	maximum AC and DC output sink current		1.1	1.5	-	mA
I _{20 max(source)}	maximum AC and DC output source current		3.0	3.5	-	mA
Limiter ampli	ifier (pin 17); note 17					
V _{i FM(rms)}	input signal voltage for lock-in (RMS value)		-	-	100	μV
V _{i FM(rms)}	input signal voltage (RMS value)	$\left(\frac{S+N}{N}\right) = 40 \text{ dB}$	-	300	400	μV
	allowed input signal voltage (RMS value)		200	-	-	mV
R _{i,17}	input resistance	note 2	480	600	720	Ω
V _{I,17}	DC input voltage		-	2.8	-	V
FM-PLL dete	ctor			·	·	•
f _{i FM(catch)}	catching range of PLL	upper limit	7.0	-	-	MHz
. /		lower limit	_	-	4.0	MHz
f _{i FM(hold)}	holding range of PLL	upper limit	9.0	-	-	MHz
		lower limit	-	-	3.5	MHz
t _{acq}	acquisition time		-	-	4	μs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FM operation	(B/G standard; pin 12); notes 1	7 and 17a	1	-	1	ļ
Vo AF12(rms)	AF output signal voltage (RMS value)	without de-emphasis; short-circuit from pin 13 to pin 14; 27 kHz (54% FM deviation); see Fig.10 and note 18				
		R _x = 470 Ω	200	250	300	mV
		$R_x = 0 \Omega$	400	500	600	mV
Vo AF12(cl)	AF output clipping signal voltage level	THD < 1.5%	1.3	1.4	_	V
Δf_{AF}	frequency deviation	THD < 1.5%; note 18	_	-	53	kHz
$\Delta V_0 / \Delta T$	temperature drift of AF output signal voltage		-	3 × 10 ⁻³	7×10 ⁻³	dB/K
V ₁₅	DC voltage at decoupling capacitor	voltage dependent on VCO frequency; note 19	1.2	-	3.0	V
R ₁₂	output resistance	note 2	_	-	100	Ω
V ₁₂	DC output voltage	tracked with supply voltage	_	$1/_{2}V_{P}$	_	V
I _{12 max(sink)}	maximum AC and DC output sink current		_	_	1.1	mA
I _{12 max(source)}	maximum AC and DC output source current		-	_	1.1	mA
B ₋₃	-3 dB video bandwidth	without de-emphasis; short-circuit from pin 13 to pin 14	100	125	-	kHz
THD	total harmonic distortion		_	0.15	0.5	%
S/N (W)	weighted signal-to-noise ratio	FM-PLL only; with 50 μs de-emphasis; 27 kHz (54% FM deviation); <i>"CCIR 468-4"</i>	55	60	-	dB
$\alpha_{c(rms)}$	residual sound carrier (RMS value)	fundamental wave and harmonics	_	_	75	mV
α_{AM}	AM suppression	50 μ s de-emphasis; AM: f = 1 kHz; m = 0.3 refer to 27 kHz (54% FM deviation)	46	50	-	dB
α ₁₂	mute attenuation of AF signal	B/G standard	70	75	_	dB
ΔV ₁₂	DC jump voltage of AF output terminal for switching AF output to mute state and vice versa	FM-PLL in lock mode	-	±50	±150	mV
PSRR	power supply ripple rejection at pin 12	$R_x = 470 \Omega$; see Fig.8	26	30	_	dB

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT			
AF performance for FM operation (B/G standard); notes 20, 21 and 22; see Table 1									
S/N (W)	weighted signal-to-noise ratio	PC/SC ratio at pins 1 and 2; 27 kHz (54% FM deviation); <i>"CCIR 468-4"</i>	27	-	-	dB			
		black picture	45	51	_	dB			
		white picture	45	51	_	dB			
		6 kHz sine wave (black to white modulation)	40	46	-	dB			
		sound carrier subharmonics; f = 2.75 MHz ±3 kHz	35	40	-	dB			

Notes

- 1. Values of video and sound parameters are decreased at $V_P = 4.5$ V.
- 2. This parameter is not tested during production and is only given as application information for designing the television receiver.
- Loop bandwidth BL = 60 kHz (natural frequency f_n = 15 kHz; damping factor d = 2; calculated with sync level within gain control range). Resonance circuit of VCO: Q₀ > 50; C_{ext} = 8.2 pF ±0.25 pF; C_{int} ≈ 8.5 pF (loop voltage approximately 2.7 V).
- 4. Temperature coefficient of external LC-circuit is equal to zero.
- V_{i IF} = 10 mV (RMS); ∆f = 1 MHz (VCO frequency offset related to picture carrier frequency); white picture video modulation.
- 6. V_{i IF} signal for nominal video signal.
- Offset current measured between pin 7 and half of supply voltage (V_P = 2.5 V) under the following conditions: no input signal at VIF input (pins 1 and 2) and VIF amplifier gain at minimum (V₂₈ = V_P).
- 8. Measurements taken with SAW filter G1962 (sound shelf: 20 dB); loop bandwidth BL = 60 kHz:
 - a) modulation VSB; sound carrier **off**; $f_{video} > 0.5$ MHz.
 - b) sound carrier **on**; $f_{video} = 10 \text{ kHz}$ to 10 MHz.
- The 7 dB buffer gain accounts for 1 dB loss in the sound trap. Buffer output signal is typical 2 V (p-p), in event of CVBS video amplifier output typical 1 V (p-p). If no sound trap is applied a 330 Ω resistor must be connected from output to input (from pin 21 to pin 22).
- 10. The leakage current of the AGC capacitor should not exceed 1 μA at B/G standard. Larger currents will increase the tilt.
- 11. S/N is the ratio of black-to-white amplitude to the black level noise voltage (RMS value, pin 10). B = 5 MHz weighted in accordance with "CCIR 567".
- 12. The intermodulation figures are defined:

$$\alpha_{1.1} = 20 \log \left(\frac{V_0 \text{ at } 4.4 \text{ MHz}}{V_0 \text{ at } 1.1 \text{ MHz}} \right) + 3.6 \text{ dB}; \alpha_{1.1} \text{ value at } 1.1 \text{ MHz} \text{ referenced to black/white signal};$$

$$\alpha_{3.3} = 20 \log \left(\frac{V_0 \text{ at } 4.4 \text{ MHz}}{V_0 \text{ at } 3.3 \text{ MHz}} \right); \alpha_{3.3} \text{ value at } 3.3 \text{ MHz} \text{ referenced to colour carrier.}$$

13. Response speed valid for a VIF input level range of 200 μ V up to 70 mV.

 $V_{o(rms)} =$

Multistandard VIF-PLL and FM-PLL demodulator

TDA9806

- 14. To match the AFC output signal to different tuning systems a current source output is provided. The test circuit is given in Fig.6. The AFC-steepness can be changed by the resistors at pin 23.
- 15. Depending on the ratio $\Delta C/C_0$ of the LC resonant circuit of VCO (Q₀ > 50; see note 3; C₀ = C_{int} + C_{ext}).
- 16. The intercarrier output signal at pin 20 can be calculated by the following formula taking into account the video output signal at pin 21 (V_{o video(p-p)} = 1 V typical) as a reference:

$$= 1 V(p-p) \times \frac{1}{2\sqrt{2}} \times 10^{\frac{V_{iSC}}{V_{iPC}}(dB) + 6 dB \pm 3 d}$$

with $\frac{1}{2\sqrt{2}}$ = correction term for RMS value,

 $\frac{V_{iSC}}{V_{iPC}}$ (dB) = sound-to-picture carrier ratio at VIF input (pins 1 and 2) in dB,

 $6 \, dB = correction term of internal circuitry$

and $\pm 3 \text{ dB}$ = tolerance of video output and intercarrier output amplitude V_{o(rms)}.

Example: SAW filter G1962 (sound shelf: 20 dB) $\Rightarrow \frac{V_{iSC}}{V_{iPC}} = -27 \text{ dB} \Rightarrow V_{o(rms)} = 32 \text{ mV typical.}$

17. Input level for second IF from an external generator with 50 Ω source impedance. AC-coupled with 10 nF capacitor, $f_{mod} = 1$ kHz, 27 kHz (54% FM deviation) of audio references. A VIF input signal is not permitted. Pin 28 has to be connected to positive supply voltage for minimum IF gain. S/N and THD measurements are taken at 50 μ s de-emphasis.

a) Second IF input level 10 mV RMS.

- 18. Measured with an FM deviation of 27 kHz the typical AF output signal is 500 mV (RMS) (R_x = 0 Ω; see Fig.10). By using R_x = 470 Ω the AF output signal is attenuated by 6 dB (250 mV RMS). For handling an FM deviation of more than 53 kHz the AF output signal has to be reduced by using R_x in order to avoid clipping (THD < 1.5%). For an FM deviation up to 100 kHz an attenuation of 6 dB is recommended with R_x = 470 Ω.
- 19. The leakage current of the decoupling capacitor (2.2 μ F) should not exceed 1 μ A.
- 20. For all S/N measurements the used vision IF modulator has to meet the following specifications:
 - a) Incidental phase modulation for black-to-white jump less than 0.5 degrees.
 - b) Picture-to-sound carrier ratio; PC/SC = 13 dB (transmitter).
 - c) Sound shelf of VIF SAW filter: minimum 20 dB.
- 21. Measurements taken with SAW filter K6256 (Siemens) for vision and sound IF (sound shelf: 20 dB). Input level V_{i SIF} = 10 mV (RMS), 27 kHz (54% FM deviation).
- 22. The PC/SC ratio at pins 1 and 2 is calculated as the addition of TV transmitter PC/SC ratio and SAW filter PC/SC ratio. This PC/SC ratio is necessary to achieve the S/N (W) values as noted. A different PC/SC ratio will change these values.

 Table 1
 Input frequencies and carrier ratios

DESCRIPTION	SYMBOL	B/G STANDARD	UNIT
Picture carrier	f _{PC}	38.9	MHz
Sound carrier	f _{SC}	33.4	MHz
Picture-to-sound carrier ratio	SC	13	dB











INTERNAL PIN CONFIGURATION



TDA9806

TEST AND APPLICATION INFORMATION



TDA9806

Multistandard VIF-PLL and FM-PLL demodulator



TDA9806

Multistandard VIF-PLL and FM-PLL demodulator

PACKAGE OUTLINE

SDIP32: plastic shrink dual in-line package; 32 leads (400 mil)



SOT232-1

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status				
Objective specification	This data sheet contains target or goal specifications for product development.			
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.			
Product specification	This data sheet contains final product specifications.			
Limiting values				
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.				
Application information				
Where application information is given, it is advisory and does not form part of the specification.				

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Printed in The Netherlands

533061/1500/01/pp24 Document order number: Date of release: 1995 Sep 05 9397 750 00307



