Modifications List

TDA933xH N1 to N2C version

Sync/Geo:

- Automatic polarity detection on Hd and Vd inputs added, so that the IC can handle sync pulses with positive or negative polarity. Polarities can be read out via status bits **HPOL** and **VPOL**. This read-out gives the possibility to read-out the used VGA mode.
- Free running frequency of horizontal PLL selectable between 31.3 and 33.7 kHz with **HDTV** bit.
- Catching range of horizontal PLL reduced from +/- 6% to +/- 5% around free running frequency. This limits the line flyback voltage at low frequency to an acceptable level.
- Clamp pulse timing selectable for HDTV signals with busbit **HDCL**.
  See also latest spec. 1999 April 12, page 37 fig. 11.
- Start of line blanking (horizontal timing) is adjustable with bus bits **LBL3...LBL0**.
  This gives more flexibility as regards to the flyback pulse width, to prevent fold over, see latest spec. page 36 fig. 10.
- Time-constant of horizontal PLL fixed to Fast mode. Busbit **FAST** is removed from subadress 03. In practice the Fast mode is always the optimal choice.
- Corner correction on East-West is split into independent upper and lower corner correction. This gives more flexibility for optimal alignment of real flat picture tubes.
- Horizontal parallelogram correction changed from 6-bit to 4-bit control.
  The range has not been changed, in practice the 4-bit resolution is sufficient.
- Extra geometry correction horizontal BOW added (4-bits). This allows optimal alignment in combination with real flat picture tubes. See latest spec. page 41 fig. 16.
- Possibility of hangup of vertical divider when switching between TV mode and VGA mode eliminated.
- Picture tube switch-off behaviour:
  - For a better discharge behaviour of the picture tube the slow stop characteristic of the horizontal output is modified, see latest spec. page 40 fig.15.
  - The duration of the discharge current for the picture tube is selectable now with busbit **TFBC**, see also latest spec. page 40 fig.15.

Control:

- Black current control loop can be switched between two point control and one point control (**OPC** bit).
  Two point control has advantages w.r.t. picture tube aging, however one point control is less critical in application in relation to loop stability.

- White point adjust (independent gain adjustment of R, G and B channels) is also possible now when black current loop is not active. This feature has advantages in LCD applications.
- Black level offset control added for R and G channel w.r.t. B channel, so that colour temperature also for low luminance levels can be adjusted, independently from the colour temperature settings at high luminance level (white point adjustment). This black level offset control is always active, so also when the black current loop is not active.
- Bandwidth of RGB channels increased. Luminance bandwidth for low capacitive load is now about 25MHz.
- Soft clipper curve is adapted. There is a sharper bend in the curve, so that the amplitude of short transients cannot exceed the PWL level too much. See also latest spec. page 36 fig. 9.
- New colour matrix added for high definition ATSC standard.
- Cathode drive level range is increased. New range from 41V to 95V (bl-wh), selectable via the **CL3...CL0** bits.
- Saturation control range is increased. Maximum saturation for small signals is increased from about 200% to about 300%. Nominal saturation has changed from 31dec. to about 20dec.
- No collapse of picture tube discharge current when feedback current becomes too small. If feedback current becomes too low the RGB outputs will go to a DC level of 6.0V.
- Peak white limiter is disabled when RGB2 signal is inserted. This prevents that the contrast of the main picture is reduced when the OSD is too bright. The softclipper stays active also for RGB2.
- Steepness of blanking edges on RGB outputs is reduced, to reduce the risk on spook.
- RGB outputs will not be blanked if no Hd pulse is present. This to facilitate OSD without Hd pulse present.

Software information for N2C:

- New **HPOL** status bit is located at subaddress 02, byte D2
  HPOL = 0 Hd input pulse is positive
  HPOL = 1 Hd input pulse is negative
- New **VPOL** status bit is located at subaddress 02, byte D1
  VPOL = 0 Vd input pulse is positive
  VPOL = 1 Vd input pulse is negative
- New **HDTV** input bit is located at subaddress 03, byte D7
  HDTV = 0 horizontal frequency is 15.6kHz (1fH mode) or 31.2kHz (2fH mode)
  HDTV = 1 horizontal frequency is 16.8kHz (1fH mode) or 33.7kHz (2fH mode)
- New **HDCL** input bit is located at subaddress 1D, byte D4
  HDCL = 0 normal timing
  HDCL = 1 HDTV timing
- New **LBL3...LBL0** bits are located at at subaddress 1D, bytes D3...D0

- New **TFBC** input bit is located at subaddress 02, byte D6
  TFBC = 0 18.6ms discharge mode
  TFBC = 1 25ms discharge mode
- **FAST** bit, located at subaddress 03, byte D5 has been removed
- **E-W corner/parabola** control (subaddress 10, bits A5...A0) changed into **E-W upper corner/ parabola** control
- New **E-W lower corner/parabola** control at subaddress 1E, bits A5...A0
- **Horizontal parallelogram** control at subaddress 0D, bits A5...A0 changed into 4 bit control, bits A3...A0
- New **Horizontal bow** control at subaddress 1F, bits A3...A0
- New **OPC** input bit at subaddress 04, bit D7
  OPC = 0 2 point control
  OPC = 1 1 point control
- New **Black level offset R** control at subaddress 1B, bits A3...A0
- New **Black level offset G** control at subaddress 1C, bits A3...A0
- Extra colour matrix mode for high definition ATSC signals:

MAT	**MUS**	matrix position
0	0	PAL
0	1	high definition ATSC
1	0	NTSC Japan
1	1	NTSC USA

Minimal necessary software adaptions when changing from N1 to N2C version:

Existing registers:
- Different value for nominal **Saturation** has to be loaded, was 31dec, now about 20dec.
- Different value of the **Horizontal parallelogram** control has to be loaded, because of change from 6 bit control to 4 bit control.

New registers:
- New subaddresses 1B,1C,1D,1E,1F must be loaded.
- The **Black level offset R** and **G** (subaddress 1B and 1C) can be set at nominal value (register value 7dec.), however for optimal low level colour temperature it is advised to determine the right settings.

- **HDCL** can be set **0**.
- **Horizontal timing** can be set nominal (value = 7dec.); to prevent fold-over it is advised to determine the optimal value in application.
- **E-W lower corner/parabola** can have the same value as upper corner parabola.
- **Horizontal bow** can set nominal for most standard picture tubes (value = 7dec.).

*Notice that it is possible to design the software in such a way that it detects if an N1 or an N2 version is used. Then no software change is needed when changing from N1 to N2 version.
This can be done by reading the bit D7 of status register 01. If this is 1, then it is the N2 version.
In that case the above mentioned minimal software adaptions have to be carried out.

Hardware information for N2C:

The N2 version requires no hardware adaptions.

Additional hardware information for both N1/N2 version:

When using the TDA933xH in combination with the TDA6120A/N2 RGB amplifiers, then emitter followers must be used at the TDA933xH RGB outputs. In connection with the DC input voltage range of the TDA6120A/N2 this **must** be PNP emitter followers. See also application report AN98073 page 78.

Status of the TDA933xH N2C samples:

- All changes from N1 to N2C are working.
- Bandwidth Improvement: via Yin/RGB1 about 25MHz, via RGB2 about 33MHz (Cload10pF).
- The problem at **RBL = 1,** found in the N2B samples has been solved in the N2C version.
- Special attention has to be paid to the application when the the low power start-up function is used (risetime of Vstart and Vcc). Details are not completed yet.