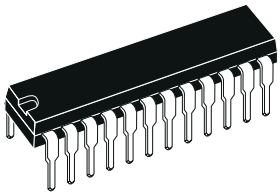
TDA9207

150MPIX VIDEO CONTROLLER WITH I²C BUS FOR CRT & LCD MONITORS

PRODUCT PREVIEW

- 150MHz PIXEL RATE
- 2.9ns RISE AND FALL TIME @ 120MHz/2V_{PP}/5pF LOAD
- I^2C BUS CONTROL
- GREY SCALE TRACKING VERSUS BRIGHTNESS
- OSD MIXING
- NEGATIVE FEED-BACK FOR DC-COUPLED CATHODES
- INTERNAL POSITIVE FEED-BACK FOR LCD APPLICATION
- 0.5 ~ 4.5V DACS FOR BLACK LEVEL RESTORATION (AC-COUPLED CATHODES) OR CUT-OFF CONTROLS WITH TDA9533 (ST VIDEO OUTPUT BUFFER FOR DC COUPLED CATHODES)
- BEAM CURRENT LIMITING
- PEDESTRAL CLAMPING ON OUTPUT STAGE
- SYNC CLIPPING
- POSSIBILITY OF LIGHT OR DARK GREY OSD BACKGROUND
- OSD INDEPENDENT CONTRAST CONTROL
- ADJUSTABLE BANDWIDTH
- INPUT BLACK LEVEL CLAMPING WITH BUILT IN CLAMPING PULSE
- STAND-BY MODE
- 5V TO 8V POWER SUPPLY



SHRINK DIP24
(Shrink Plastic Package)

ORDER CODE : TDA9207

DESCRIPTION

The TDA9207 is a monolithic integrated RGB preamplifier for color Monitors with I^2C Bus Control and On-Screen Display.

The classical Contrast, Brightness, Drive and Cut-Off Controls are provided.

On Top of that, additional functions have been integrated as follows :
- OSD contrast,
- Bandwidth adjustment,
- Grey background,
- Internal back porch clamping pulse generator.

The RGB incoming signals are amplified and shaped, to drive all commonly used Video buffer without intermediate follower stage.

Eventhrough encapsulated in 24 pins package only, the IC allows any kind of CRT Cathode coupling :
- AC coupled with DC restore,
- DC coupled with Feed-Back from Cathodes,
- DC coupling with Cut-Off controls on Video Output buffer (with TDA9533).

The IC, as any ST Video preamplifier, is designed in such a way to be able to drive real load without external interface.

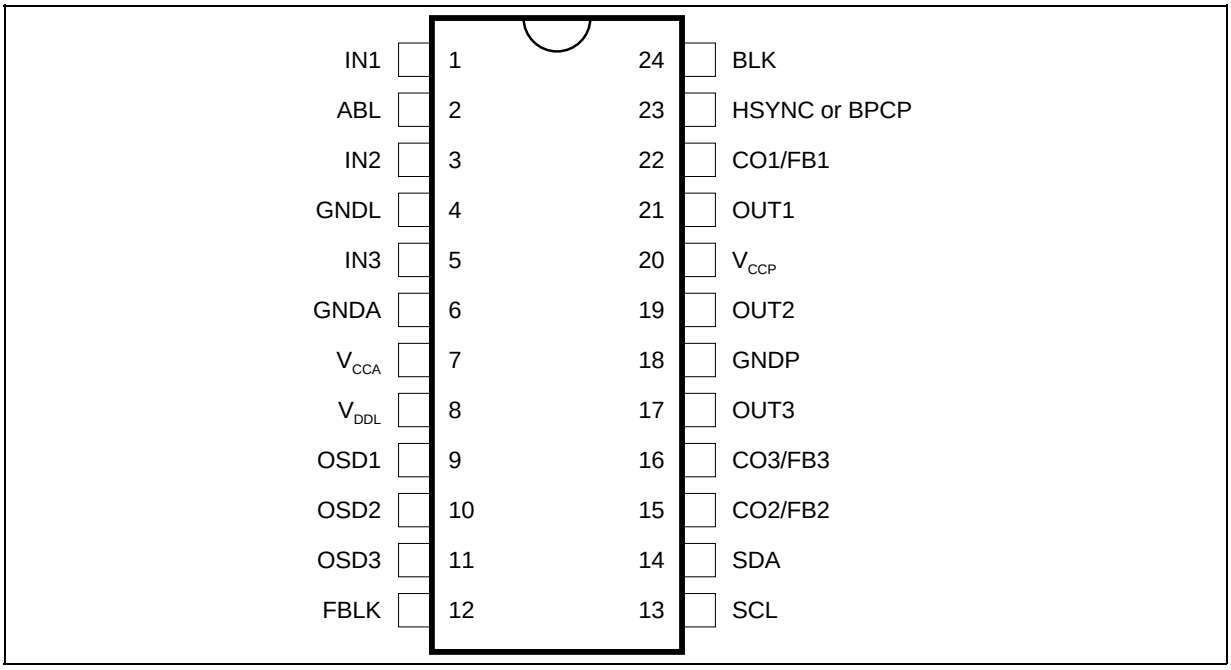
A very typical advantage of ST devices is their ability to sink and source currents, while most of competitive devices have problem to sink large current.

Thanks to the original internal output stage structure, those driving capabilities are combined with low Power Dissipation as there is not static current consumption in the output pins.

All together, the large integration combined with high performance and advanced features make the TDA9207 one of the best choice for any CRT Monitor ranging from 14" to 17".

Combined with TDA910x (H/V processor) ; TDA9533 (Video amplifier) ; STV942x (OSD) and ST72xx (MCU), the TDA9207 allows to realize high performance and cost optimized application.

PIN CONNECTIONS



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PIN DESCRIPTION

Pin Number	Symbol	Function
1	IN1	Red Video Input
2	ABL	ABL Input
3	IN2	Green Video Input
4	GNDL	Logic Ground
5	IN3	Blue Video Input
6	GNDA	Analog Ground
7	V_{CCA}	Analog V_{CC}
8	V_{DDL}	Logic V_{DD}
9	OSD1	Red OSD Input
10	OSD2	Green OSD Input
11	OSD3	Blue OSD Input
12	FBLK	Fast Blanking
13	SCL	SCL
14	SDA	SDA
15	CO2/FB2	Green Cut-off Output/Feedback Input
16	CO3/FB3	Blue Cut-off Output/Feedback Input
17	OUT3	Blue Video Output
18	GNDP	Power Ground
19	OUT2	Green Video Output
20	V_{CCP}	Power V_{CC}
21	OUT1	Red Video Output
22	CO1/FB1	Red Cut-off Output/Feedback Input
23	HSYNC BPCP	HSYNC BPCP
24	BLK	Blanking Input

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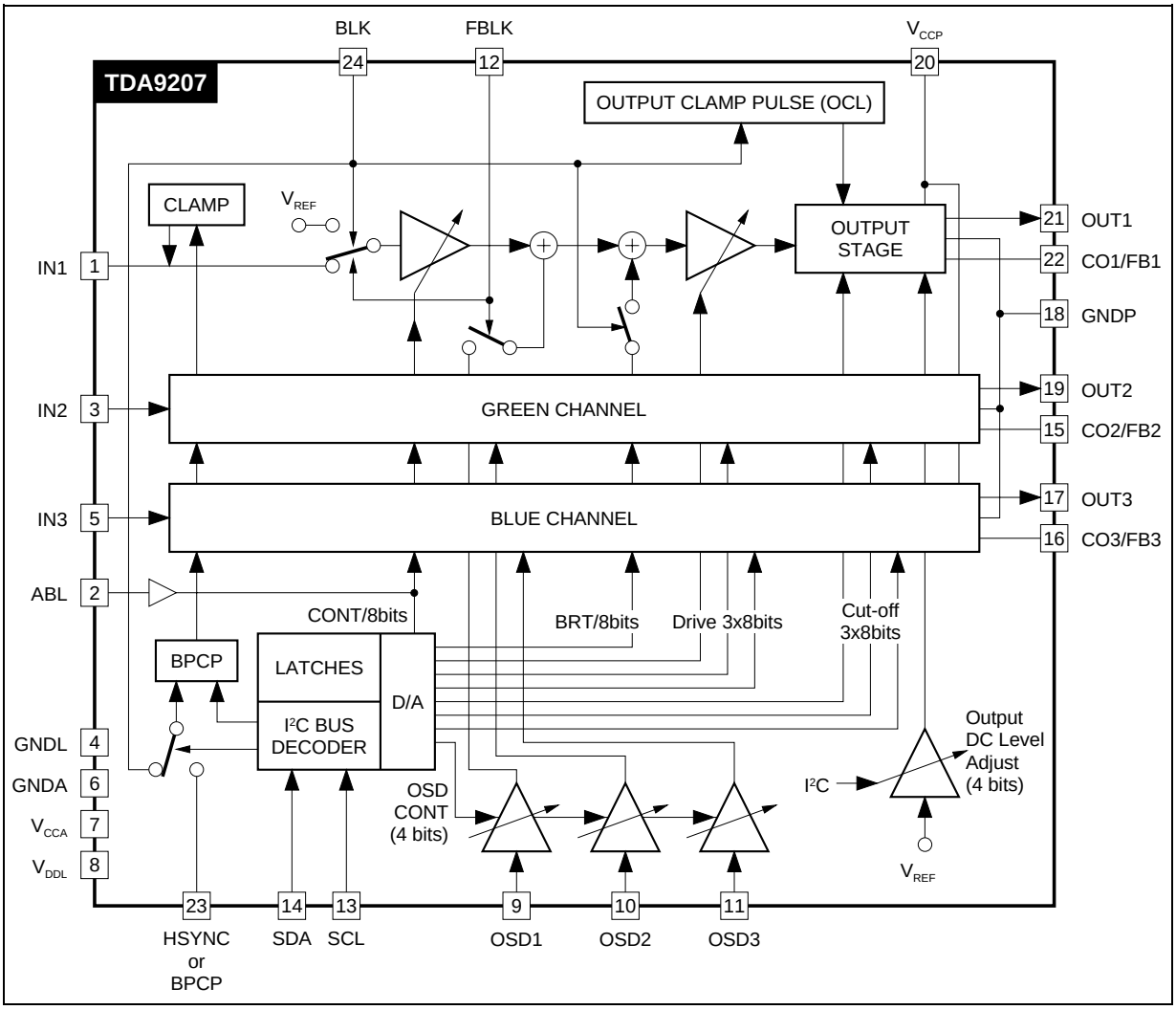
BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

1 - Input Stage

The R, G and B signals must be fed to the 3 inputs through coupling capacitors (100nF).

The maximum input peak-to-peak Video amplitude is 1V.

The input stage includes a clamping function. This clamp uses the input serial capacitor as a "memory capacitor".

In order to avoid a discharge of the serial capacitor during the line (due to leakage current), the input voltage is referenced to the ground.

The clamp is gated by an internally generated "Back Porch Clamping Pulse" (BPCP). Register 8 allows choice of the way to generate BPCP (see Figure 1) :

- When bit 0 is set to 0, BPCP is synchronized on the trailing or leading edge of HSYNC (Pin 23) (bit 1 = 0 : trailing edge, bit 1 = 1 : leading edge). Thanks to an automatic function, the IC is able to work with positive or negative HSYNC pulse..
- When bit 0 is set to 1, BPCP is synchronized on the leading edge of the blanking pulse BLK (Pin 24). One can use positive or negative blanking pulse by programming bit 0 in Register 9.
- BPCP width can be adjusted with bit 2 and 3 (see Register 8 table).
- In case of application provides already the Back Porch Clamping Pulse, bit 4 must be set to 1 (direct connection between Pin 23 and internal BPCP is provided).

A sync clipping function is provided on channel 2. In the case of input signal voltage is lower than reference voltage (SOG standard for example), output voltage is set to the brigthness voltage (V_{BRT}).

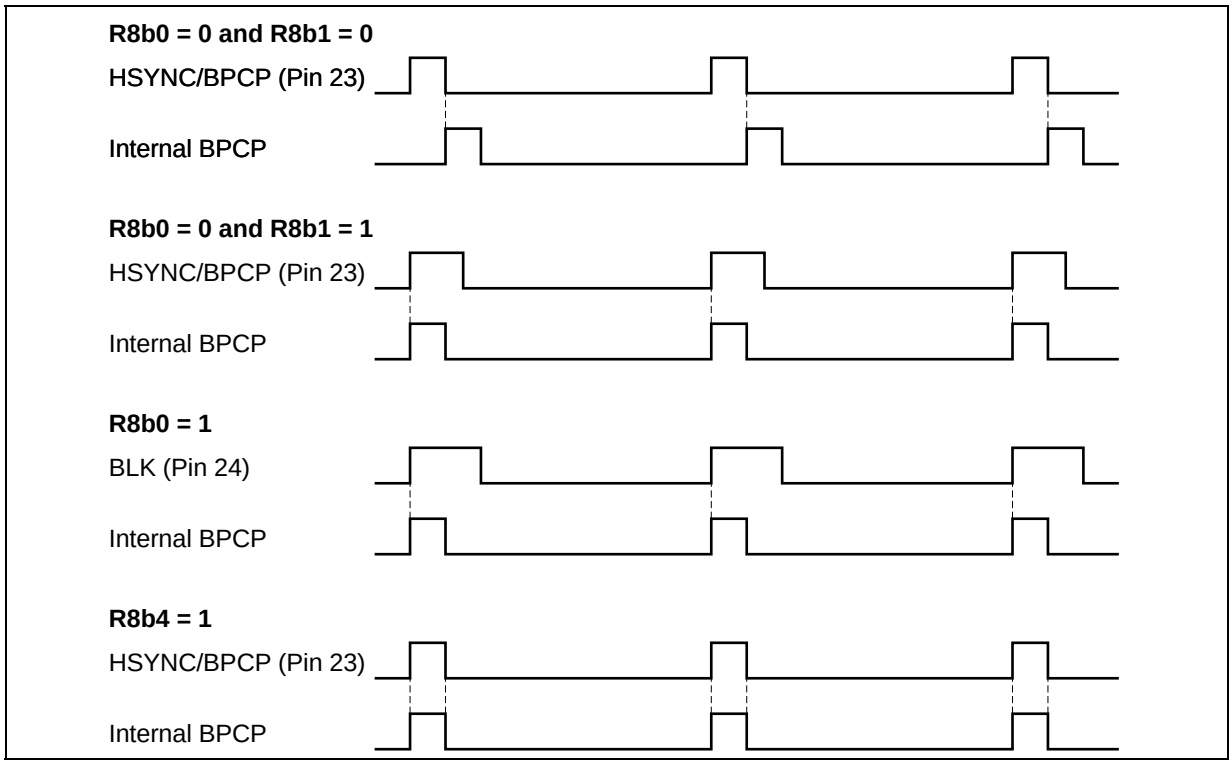
As a matter of fact, no voltage below the brigthness voltage can be obtained on output signals and unbalance colors can't occur whatever the standard is.

To validate this function, bit 7 in Register 9 must be set to 1.

2 - Contrast Adjustment (8 bits)

The contrast adjustment is made by controlling simultaneously the gain of the 3 internal amplifiers through I^2C bus interface. Register 1 allows adjustment in a range of 48dB.

Figure 1



FUNCTIONAL DESCRIPTION (continued)

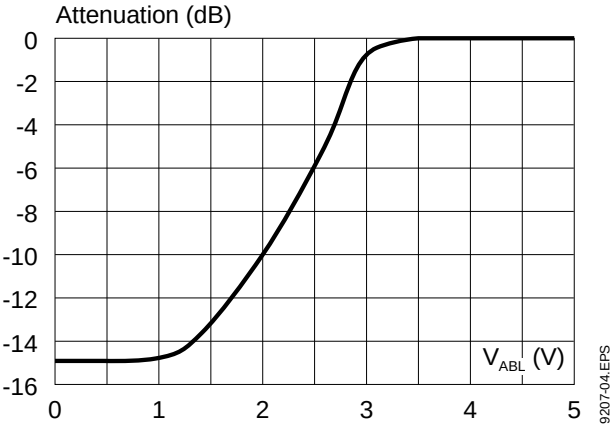
3 - ABL Control

The TDA9207 includes an ABL input (automatic beam limitation) in order to attenuate R, G, B Video signals according to beam intensity.

The operating range is to 2V typically (from 3V to 1V). A typical 15dB maximum attenuation is applied to the signal wathever the contrast adjustment is. Refer to Figure 2 for ABL attenuation range.

In case of ABL feature is not used, ABL input (Pin 2) must be connected to 5V supply voltage.

Figure 2



4 - Brightness Adjustment (8 bits)

Brightness adjustment is controlled by I^2C bus thanks to Register 2. It consists to add the same DC voltage to the 3 R, G, B signals after contrast adjustment. This voltage is present only outside the blanking pulse (see Figure 3). It can be adjusted in the range of 0V to 2V with 8mV step.

The DC output level during the blanking pulse is forced to "INFRA BLACK" level (V_{DC}).

5 - Drive Adjustment (3 x 8 bits)

In order to adjust the white balance, the TDA9207 offers the possibility to adjust separately the overall gain of each channel thanks to I^2C bus (Registers 3, 4 and 5).

The very large drive adjustment range (48dB) allows different standard or custom color temperature.

It can also be used to adjust the output voltages at the optimum amplitude to drive the CRT drivers, keeping the whole contrast control for end-user only.

The drive adjustment is located after the Contrast, Brightness and OSD switch blocks, so that the white balance will remains correct when BRT is adjusted, and will also be correct on OSD portion of the signal.

6 - OSD Inputs

The TDA9207 includes the circuitry to mix OSD signals into the RGB main picture. Four pins are dedicated to this function as follow :

- 3 TTL RGB inputs (Pins 9, 10, 11) which are connected to the 3 outputs of the corresponding OSD processor,
- one TTL fast blanking input (Pin 12) also connected to the FBLK output of the OSD processor.

When a high level is present on FBLK, the IC will acts as follow :

- The 3 main picture RGB input signals are internally switched to the internal input clamp reference voltage.
- The 3 output signals are set to the voltage corresponding to the 3 OSD input logic states (0 or 1) (see Figure 3).

If OSD input is low level, output equals brightness voltage (V_{BRT}).

If OSD input is high level, output equals V_{OSD} where $V_{OSD} = V_{BRT}$ + OSD and OSD is an I^2C bus controlled voltage.

OSD varies between 0V to 4.5V by step of 300mV thanks to Register 7 (4 bits). The same variation is applied simultaneously on the 3 channels providing an OSD contrast.

Grey color can be obtained on output signals if :

- OSD1 = 1 and OSD2 = 0 and OSD3 = 1
- and if a special bit (bit 5 or 6) in Register 9 is set to 1.

If R9b5 is set to 1, light grey is obtained on output.
If R9b6 is set to 1, dark grey is obtained on output.

In the case of R9b5 and R9b6 are set to 0, normal operation is provided on output signals.

7 - Output Stage

The 3 output stages are large bandwidth output amplifiers able to deliver up to $4.6V_{PP}$ for $0.7V_{PP}$ on input.

When high level is applied on BLK input (Pin 24), the 3 outputs are forced to "INFRA BLACK" level (V_{DC}) thanks to a sample and hold system (see here after).

The black level (which is the output voltage outside the blanking pulse with minimum brightness and no Video input signals) is 400mV higher than V_{DC}.

The brightness level (V_{BRT}) is then obtained by programming the corresponding register.

The sample and hold system allows control of the "INFRA BLACK" level in the range of 0.5V to 2.5V thanks to Register 6 (in case of AC coupling) or Registers 10, 11, 12 (in case of DC coupling).

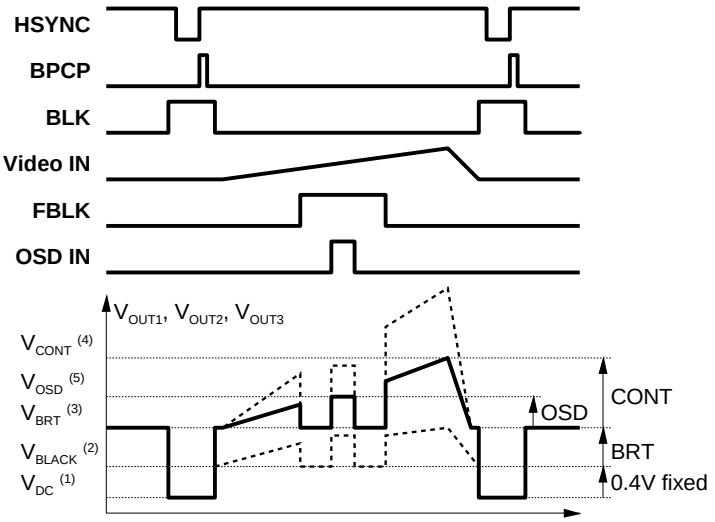
Refer to "CRT cathode coupling" part for further details.

FUNCTIONAL DESCRIPTION (continued)

The overall waveforms of the output signal are shown in Figures 3 and 4.
In the case of blanking pulse is not applied on TDA9207, an additional feature allows the connection of internal BPCP to the sample and hold system so that the output DC level is still I^2C controlled.

For that purpose, bit 7 in Register 8 must be set to 1.
Then more, in order to simplify the application, it is possible to supply the power V_{CC} with 5V (instead of 8V nominal) at the expense of output swing voltage.

Figure 3 : Waveforms VOUT, BRT, CONT, OSD



Notes : 1. V_{DC} = 0.5 to 2.5V
2. $V_{BLACK} = V_{DC} + 0.4V$
3. $V_{BRT} = V_{BLACK}$ + BRT (with BRT = 0 to 2V)
4. $V_{CONT} = V_{BRT}$ + CONT with CONT = k x Video IN (CONT = $4.6V_{PP}$ max. for $V_{IN} = 0.7V_{PP}$)
5. $V_{OSD} = V_{BRT}$ + OSD (OSD max. = $4.5V_{PP}$, OSD min. = $0.3V_{PP}$)

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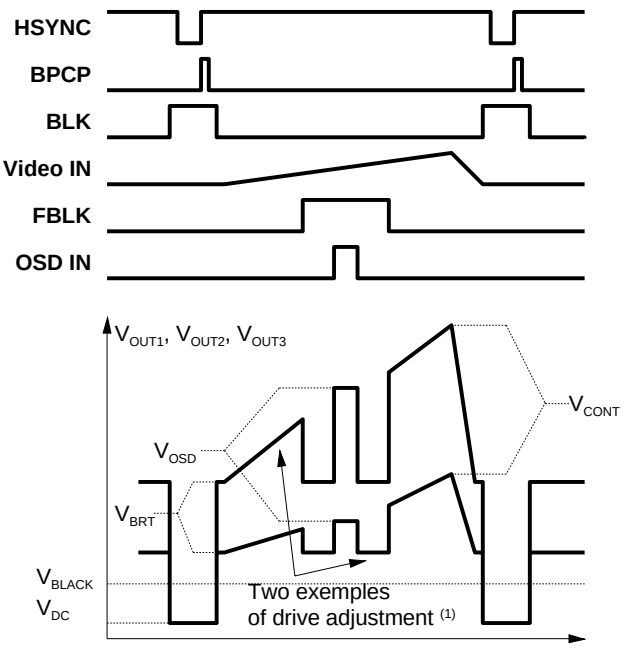
Figure 4 : Waveforms (DRIVE adjustment)



Note : 1. Drive adjustment modifies the following voltages : V_{CONT}, V_{BRT} and V_{OSD}.
Drive adjustment do not modify the following voltages : V_{DC} and V_{BLACK}.

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FUNCTIONAL DESCRIPTION (continued)

8 - Bandwidth Adjustment

A new feature, bandwidth adjustment, has been implemented on TDA9207.

This function has several advantages :

- Depending an external capacitive load and on pic to pic output voltage, bandwidth can be adjusted in order to avoid any slew-rate phenomenon (see Table 1 here after and refer to Register 13 description).
- Since it is possible to slew down signal rise/fall time at the CRT driver input without affecting too much rise/fall time at the CRT driver output, preamp bandwidth can be adjusted in order to reduce electromagnetic radiation.
- As the preamp bandwidth adjustment permits also to adjust the rise/fall time on the cathode (through the CRT driver), it is possible to optimize the frequency response / CRT driver power consumption ratio for any kind of chassis.
- In picture mode, when high Video voltage swing is of great interest at the expense of rise/fall time, bandwidth adjustment may be the right way to avoid any slew rate phenomenon at the CRT driver output and to fit with electromagnetic radiation requirements.

Table 1 : Recommendation for bandwidth adjustment

Video Output Voltage	C_{LOAD}		
	1.5pF	**5pF**	**10pF**
$2V_{PP}$	TBD	120MHz	TBD
$3V_{PP}$	TBD	100MHz	TBD
$4V_{PP}$	TBD	TBD	TBD

9 - CRT Cathode Coupling

Thanks to the multiplex of cut-off output and feedback input, the IC provides several kind of CRT cathode coupling.

9.1 - AC coupling with DC restore (see Figure 5)

In this mode, output DC level (V_{DC}) is adjusted simultaneously for the 3 channels from 0.5V to 2.5V thanks to Register 6 (4 bits). The cut-off voltage is programmed independently for each channel from 0.5V to 4.5V with the help of registers 10, 11, 12 (3 x 8 bits).

9.2 - DC Coupling with cut-off controls on Video Amplifier (with TDA9533)

The functionning of the TDA9207 and the way to program it are the same as in the previous mode. But now, the cut-off control is made at the Video amplifier input (see Figure 6).
In AC coupling and in DC coupling with cut-off control, bits 2, 3 and 4 in Register 9 must be set to 1.

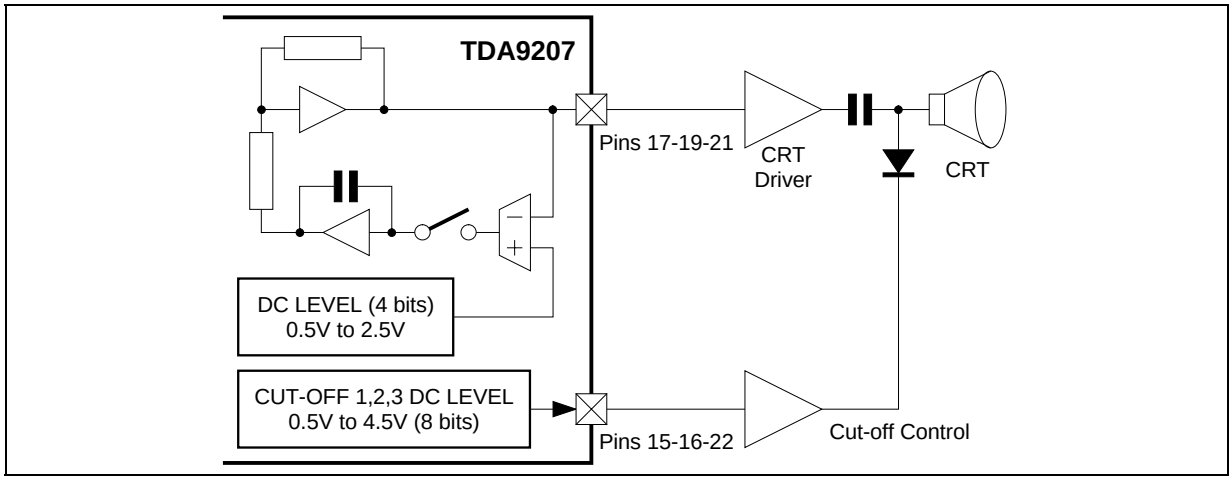
9.3 - DC Coupling Mode

In this mode, the cut-off level is controlled at the output of the preamp. So, output DC level (V_{DC}) is adjusted independently for each channel from 0.5V to 2.5V via registers 10, 11 and 12 (see Figure 7).
In DC coupling mode, bit 2 must be set to 1 and b3 to 0 in Register 9.

9.4 - DC Coupling with feedback mode

The feedback voltage coming from the cathode is sent to the TDA9207. The sample and hold system compares this voltage with a reference coming from the cut-off DC level DAC and controls the DC voltage on the feedback input in the range of 0.5V to 2.5V.
Each channel is controlled independently thanks to Registers 10, 11 and 12 (see Figure 8).
In DC coupling with feedback mode, bit 2 and bit 4 must be set to 0 in Register 9.

Figure 5



FUNCTIONAL DESCRIPTION (continued)

Figure 6

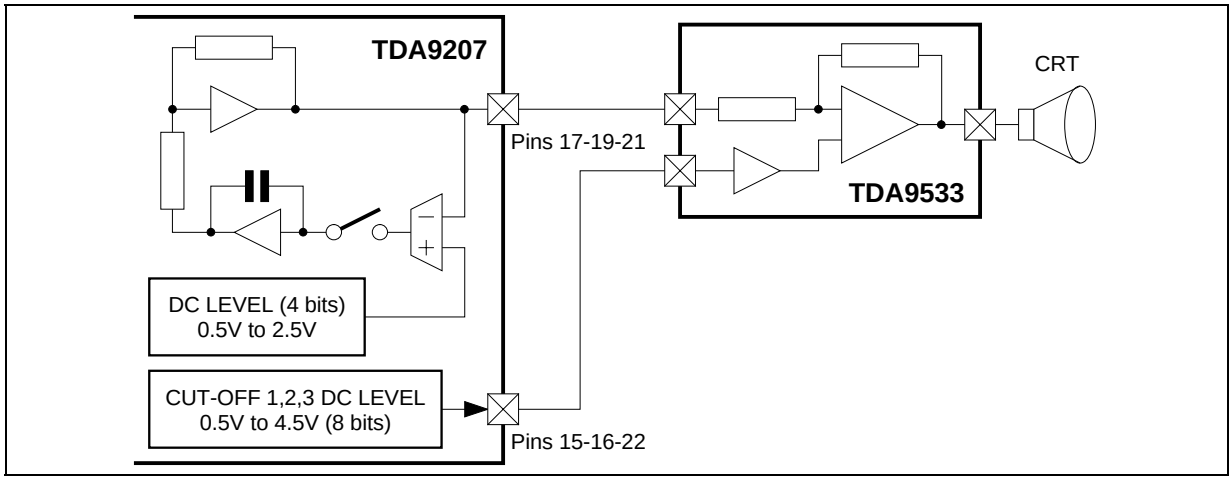


Figure 7

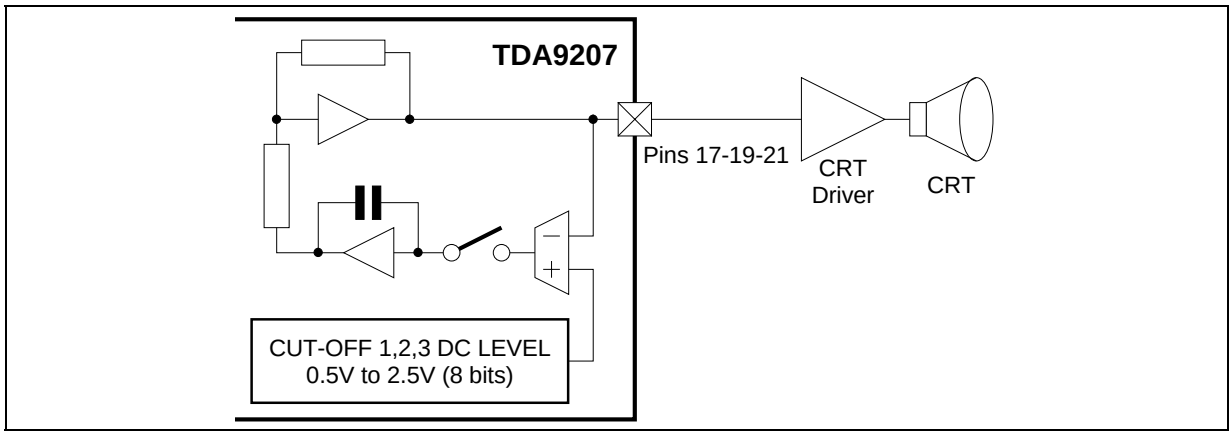
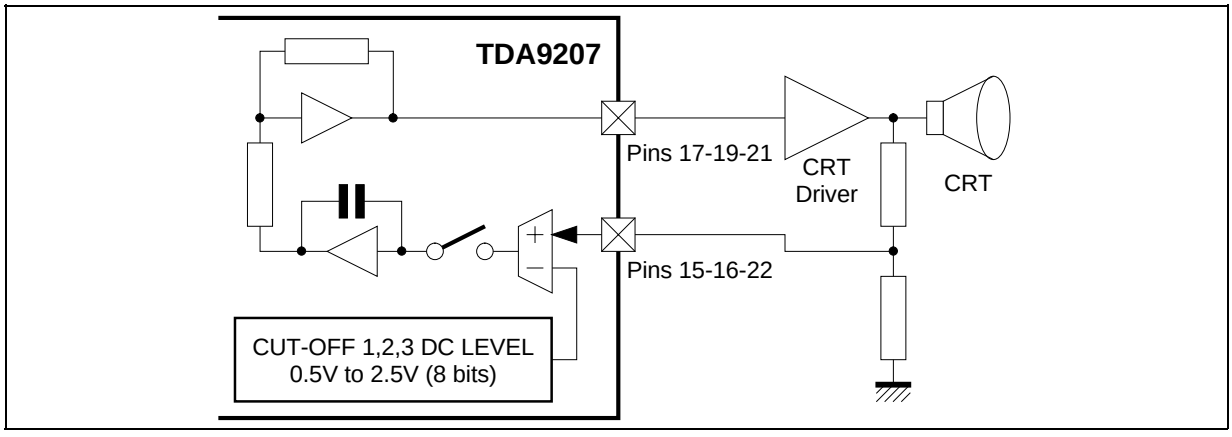


Figure 8



FUNCTIONAL DESCRIPTION (continued)

10 - Stand-by Mode

A stand-by mode is implemented on the IC. As soon as the power V_{CC} (Pin 20) falls down below 3V typically, the device enters in stand-by mode wathever the voltage on analog V_{CC} (Pin 7) and on logic V_{DD} (Pin 8) is. In this case, all the analog part biases are internally switched-off while the logic parts (I^2C bus, power-on reset) are still supplied.

As a matter of fact, the corresponding power consumption is lower than 50mW in stand-by mode.

11 - Serial Interface

The 2 wires serial interface is an I^2C interface. The slave address of TDA9207 is DC hex.

A6	A5	A4	A3	A2	A1	A0	W
1	1	0	1	1	1	0	0

The host MCU can write into the TDA9207 registers. Read mode is not available.

To write data into the TDA9207, after a start, the MCU must send (see Figure 9). :

- the I^2C address slave byte with a low level for the R/W bit,
- the byte to the internal register address where the MCU wants to write data,
- the data.

All bytes are sent MSB bit first and the write data transfer is closed by a stop.

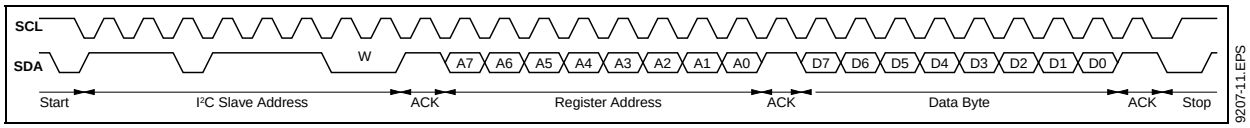
When transmitting several datas, it is possible to send before the stop as many as needed register address plus data without sending start and slave address.

12 - Power-on Reset

A power-on reset function is implemented on the TDA9207 so that the I^2C registers are in a well known status after power-on. Typical threshold for a rising supply on logic V_{DD} (Pin 8) is 3.8V.

It has some hysteresis and I^2C registers are reseted as soon as V_{DD} falls below 3.2V.

Figure 9 : I^2C Write Operation



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Pin	Value	Unit
V_S V_S V_{SPW}	Supply Voltage on Analog V_{CC} Supply Voltage on Logic V_{DD} Supply Voltage on Power V_{CC}	7 8 20	5.5 5.5 8.8	V V V
V_{IN}	Voltage at any Input Pins (except Video inputs) and Input/Output Pins		5.5	V
$V_{INVIDEO}$	Voltage at Video Inputs	1, 3, 5	1.4	V

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THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance	Max.	69	$^oC/W$

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DC ELECTRICAL CHARACTERISTICS

T_{amb} = 25^{o}C, V_{CCA} = 5V, V_{DD} = 5V, V_{CCP} = 8V unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S VS VSPW	Supply Voltage	Analog V_{CC} (Pin 7) Logic V_{DD} (Pin 8) Power V_{CC} (Pin 20)	4.5 4.5 4.5	5 5 8	5.5 5.5 5.8	V V V
I_{CC}	Supply Current	Analog V_{CC} and V_{DD}		75		mA
I_{CCP}	Supply Current	Power V_{CC}		52		mA
V_I	Video Input Voltage Amplitude			0.7	1	V_{PP}
V_{OR}	Typical Output Voltage Range		0.5		7	V_{DC}
V_{IL} V_{IH}	Low Level Input Voltage High Level Input Voltage	OSD, FBLK, BLK, HSYNC	 2.4		0.8	V V
I_{IN}	Input Current	OSD, FBLK, BLK, HSYNC	-1		1	µA

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AC ELECTRICAL CHARACTERISTICS

T_{amb} = 25°C, V_{CCA} = 5V, V_{DD} = 5V, V_{CCP} = 8V, V_I = 0.7V_{PP}, C_{LOAD} = 5pF, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VIDEO INPUTS (Pins 1,3,5)						
V_I	Video input Voltage Amplitude	Contrast and Drive at maxi		0.7	1	V_{PP}
VIDEO OUTPUTS (Pins 17,19,21)						
VIDEO SIGNAL						
GAM	Maximum Gain	Contrast and Drive at maxi (CRT = DRV = 254dec)		16.4		dB
VOM	Maximum Video Output Voltage (peak-to-peak)	Contrast and Drive at maxi (CRT = DRV = 254dec)		4.6		V_{PP}
VON	Nominal Video Output Voltage (peak-to-peak)	Contrast and Drive at POR (CRT = DRV = 180dec)		2.3		V_{PP}
CAR	Contrast Attenuation Range	Contrast maxi (CRT = 254dec) to Contrast mini (CRT = 1dec)		48		dB
DAR	Drive Attenuation Range	Drive maxi (DRV = 254dec) to Drive mini (DRV = 1dec)		48		dB
GM	Gain Matching	Contrast and Drive at POR		± 0.1		dB
t_R t_F	Rise time Fall time	V_{OUT} = 2V_{PP} (BW = 15dec) V_{OUT} = 3V_{PP} (BW = 7dec)		2.9 3.6		ns ns
BW	Large Signal Bandwidth	V_{OUT} = 2V_{PP} (BW = 15dec) V_{OUT} = 3V_{PP} (BW = 7dec)		120 100		MHz MHz
	Bandwidth Adjustement Range	Minimum bandwidth (BW = 0dec) Maximum bandwidth (BW = 15dec)		80 120		MHz MHz
CT	Crosstalk between Video Outputs	V_{OUT} = 2.3V_{PP} @ f = 10MHz @ f = 50MHz		70 35		dB dB
VIDEO SIGNAL - BRIGTHNESS						
BRTmax	Maximum Brightness Level	Brightness at maxi (BRT = 255dec) Drive at maxi (DRV = 254dec)		2		V_{PP}
BRTmin	Minimum Brightness Level	Brightness at mini (BRT = 0dec) Drive at maxi (DRV = 254dec)		0		V_{PP}
VIP	Insertion Pulse			0.4		V
BRTM	Brightness Matching	Brightness and Drive at POR		± 20		mV
VIDEO SIGNAL - OSD						
OSDmax OSDmin	Maximum OSD Output Level Minimum OSD Output Level	Drive at maxi (DRV = 254dec) OSD at maxi (OSD = 15dec) OSD at mini (OSD = 0dec)		4.5 0		V_{PP} V_{PP}
VIDEO SIGNAL - DC LEVEL (AC COUPLING MODE)						
DCLmax DCLmin	Maximum Output DC Level Minimum Output DC Level	DCL at maxi (DCL = 15 dec) DCL at mini (DCL = 3 dec)		2.5 0.5		V V
VIDEO SIGNAL - DC LEVEL (DC COUPLING MODE)						
DCLmax DCLmin	Maximum Output DC Level Minimum Output DC Level	Cut-off at maxi (Cut-off = 255dec) Cut-off at mini (Cut-off = TBD)		2.5 0.5		V V
CUT-OFF OUTPUTS /FEEDBACK INPUTS (Pins 15,16,22)						
CUT-OFF OUTPUTS (AC COUPLING MODE)						
COmax	Maximum Cut-off Output Voltage	Cut-off at maxi (Cut-off = 255dec) (Sourced current = 200µA)		4.5		V
COmin	Minimum Cut-off Output Voltage	Cut-off at mini (Cut-off = 0dec) (Sinked Current = 2mA)		0.5		V
COTD	Cut-off Output Voltage Drift	T_j Variation = 100°C		TBD		mV
FEEDBACK INPUTS (DC WITH FEEDBACK MODE)						
VFBmax VFBmin	Controlled Feedback Input Level Maximum Minimum	Cut-off at maxi (Cut-off = 255dec) Cut-off at mini (Cut-off = TBD)		2.5 0.5		V V
IFB	Input Current on Feedback Inputs	V ≤ 2.5V		-1		µA

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AC ELECTRICAL CHARACTERISTICS (continued)

T_{amb} = 25°C, V_{CCA} = 5V, V_{DD} = 5V, V_{CCP} = 8V, V_I = 0.7V_{PP}, C_{LOAD} = 5pF, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ABL (PIN 2)						
GABLmin GABLmax	ABL Mini Attenuation ABL Maxi Attenuation	$V_{ABL} \geq 3V$ V_{ABL} = 1V		0 15		dB dB
V_{ABL}	ABL Threshold Voltage	For output attenuation		3		V
IABLhigh IABLlow	ABL Input Current	V_{ABL} = 3V V_{ABL} = 1V		0 -2		µA µA

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I^2C ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_{CC} = 12V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low Level Input Voltage	On Pins SDA, SCL			1.5	V
V_{IH}	High Level Input Voltage		3			V
I_{IN}	Input Current (Pins SDA, SCL)	0.4V < V_{IN} < 4.5V	-10		+10	µA
$f_{SCL(Max.)}$	SCL Maximum Clock Frequency		200			kHz
V_{OL}	Low Level Output Voltage	SDA Pin when ACK Sink Current = 6mA			0.6	V

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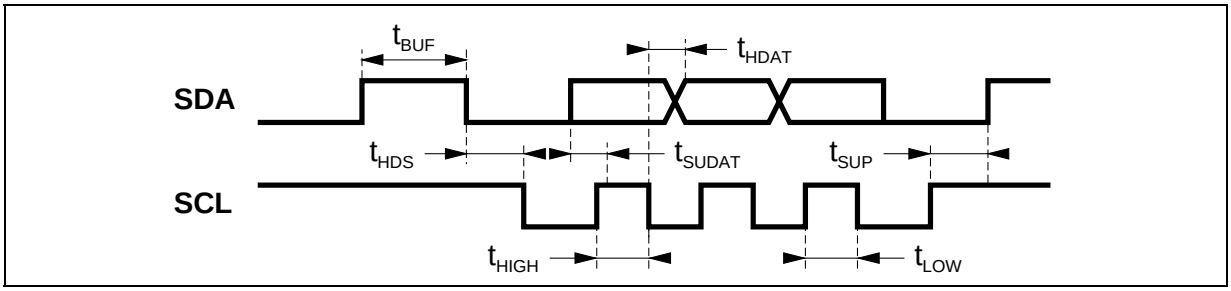
I^2C INTERFACE TIMINGS REQUIREMENTS (see Figure 12)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{BUF}	Time the bus must be free between 2 access	1300			ns
t_{HDS}	Hold Time for Start Condition	600			ns
t_{SUP}	Set-up Time for Stop Condition	600			ns
t_{LOW}	The Low Period of Clock	1300			ns
t_{HIGH}	The High Period of Clock	600			ns
t_{HDAT}	Hold Time Data	300			ns
t_{SUDAT}	Set-up Time Data	250			ns
t_R, t_F	Rise and Fall Time of both SDA and SCL	20		300	ns

9207-08.TBL

Figure 10



9207-12.EPS

I²C REGISTER DESCRIPTION

Registers Sub-address

Sub-address		Register Names		POR Value		Max. Value
Hex	Dec			Hex	Dec	
01	01	Contrast (CRT)	8-bit DAC	B4	180	254
02	02	Brightness (BRT)	8-bit DAC	B4	180	255
03	03	Drive 1 (DRV)	8-bit DAC	B4	180	254
04	04	Drive 2 (DRV)	8-bit DAC	B4	180	254
05	05	Drive 3 (DRV)	8-bit DAC	B4	180	254
06	06	Output DC Level (DCL)	4-bit DAC	09	09	15
07	07	OSD Contrast (OSD)	4-bit DAC	09	09	15
08	08	BPCP & OCL	See Table	04	04	
09	09	Miscellaneous	See Table	1C	28	
0A	10	Cut Off Out 1 DC Level (Cut-off)	8-bit DAC	B4	180	255
0B	11	Cut Off Out 2 DC Level (Cut-off)	8-bit DAC	B4	180	255
0C	12	Cut Off Out 3 DC Level (Cut-off)	8-bit DAC	B4	180	255
0D	13	Bandwidth Adjustment (BW)	4-bit DAC	07	07	15

Note : For Contrast & Drive adjustement, code 01 (dec) and 255(dec) are not allowed.
For Output DC Level, code 00(dec), 01(dec), 02(dec) are not allowed.
For Cut Off Output DC Level, output voltage is linear between code TBD and code TBD.

BPCP & OCL Register (R8)

b7	b6	b5	b4	b3	b2	b1	b0	Function	POR Value
							0	BPCP Source = HSYNC	x
							1	BPCP Source = BLK	
						0		HSYNC edge = trailing	x
						1		HSYNC edge = leading	
				0	0			BPCP Width = 0.33µs	
				0	1			BPCP Width = 0.66µs	x
				1	0			BPCP Width = 1µs	
				1	1			BPCP Width = 1.33µs	
			0					BPCP Source = HSYNC	x
			1					BPCP Source = BPCP input	
		0						Normal Operation	x
		1						Force BPCP to 1 (for test)	
	0							Normal Operation	x
	1							Force OCL to 1 (for test)	
0								OCL Source = BLK input	x
1								OCL Source = BPCP	

I²C REGISTER DESCRIPTION (continued)

Miscellaneous Register (R9)

b7	b6	b5	b4	b3	b2	b1	b0	Function	POR Value
							0	Positive Blanking Polarity	x
							1	Negative Blanking Polarity	
						0		Soft Blanking = OFF	x
						1		Soft Blanking = ON	
			1	1	1			AC Coupling Mode	x
			x	0	1			DC Coupling Mode	
			0	x	0			DC Coupling with Feedback Mode	
	0	0						Light Grey on OSD Ouputs = OFF	x
	0	1						Light Grey on OSD Ouputs = ON	
	0	0						Dark Grey on OSD Ouputs = OFF	x
	1	0						Dark Grey on OSD Ouputs = ON	
0								SOG Clipping = OFF	x
1								SOG Clipping = ON	

Bandwidth Adjustment (R13)

b7	b6	b5	b4	b3	b2	b1	b0	Function	POR Value
				1	1	1	1	120MHz	
				0	1	1	1	100MHz	x
				0	0	0	0	80MHz	
		0	0					Normal Operation	x
		0	1					BW DAC output connected to BLK input (for test)	
		1	0					BW DAC complementary output connected to BLK input (for test)	

INTERNAL SCHEMATICS

Figure 11

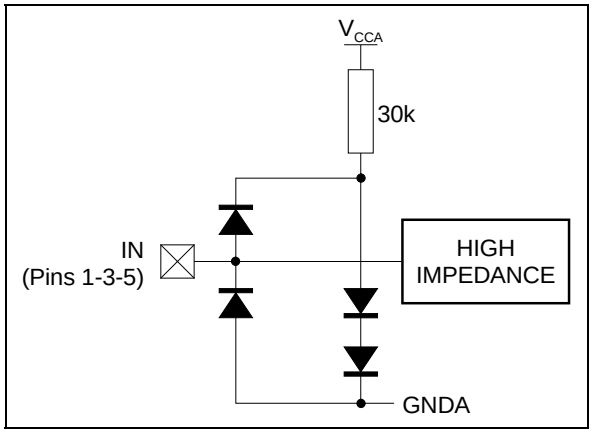


Figure 12

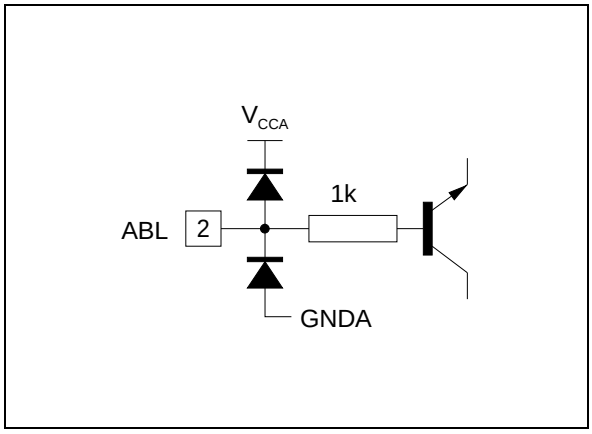


Figure 13

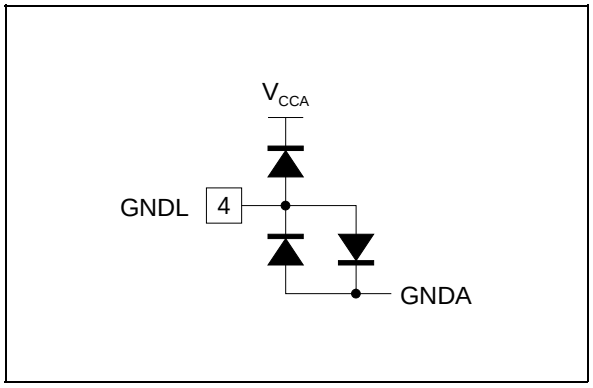


Figure 14

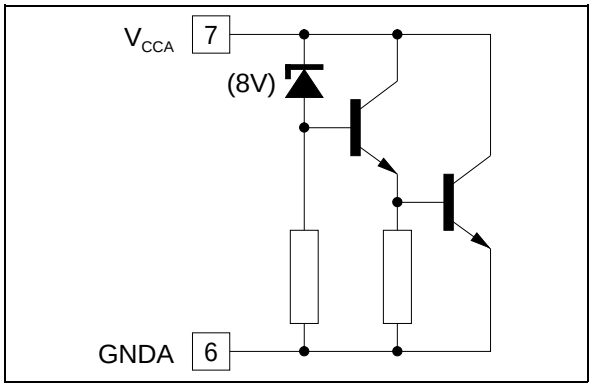


Figure 15

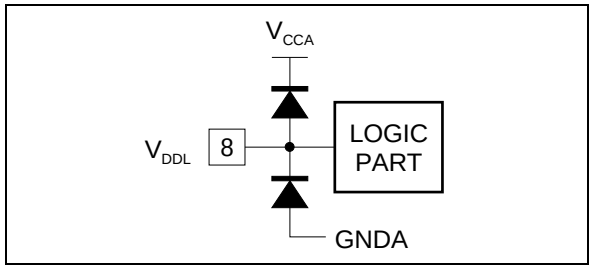


Figure 16

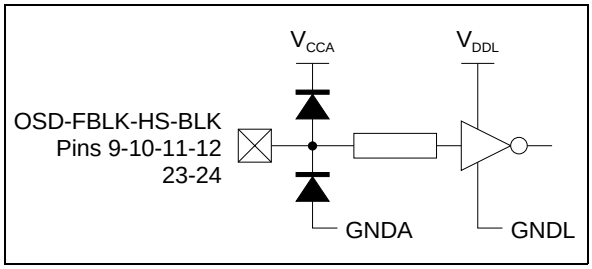


Figure 17

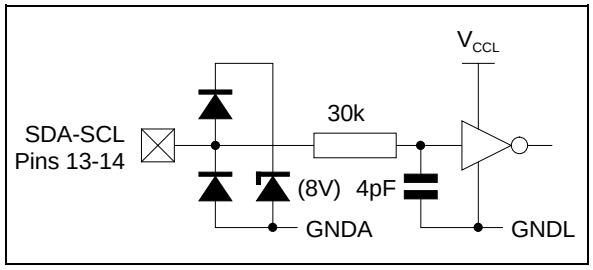
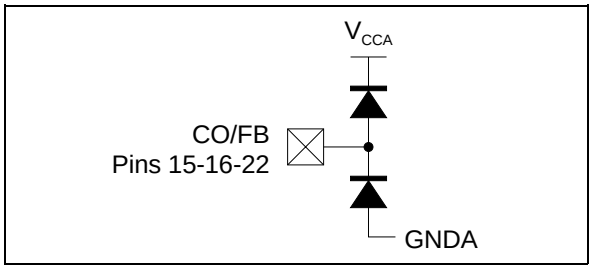


Figure 18



INTERNAL SCHEMATICS (continued)

Figure 19

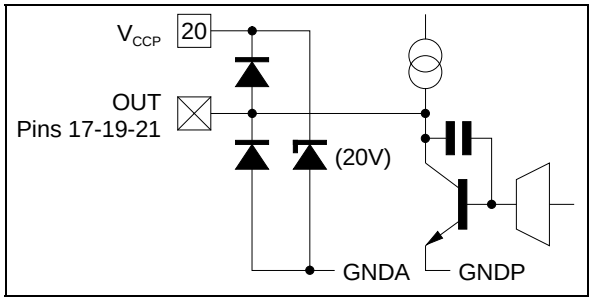
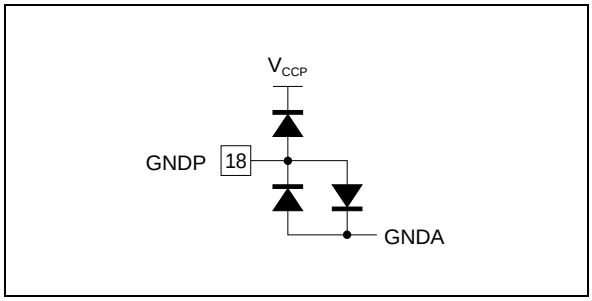
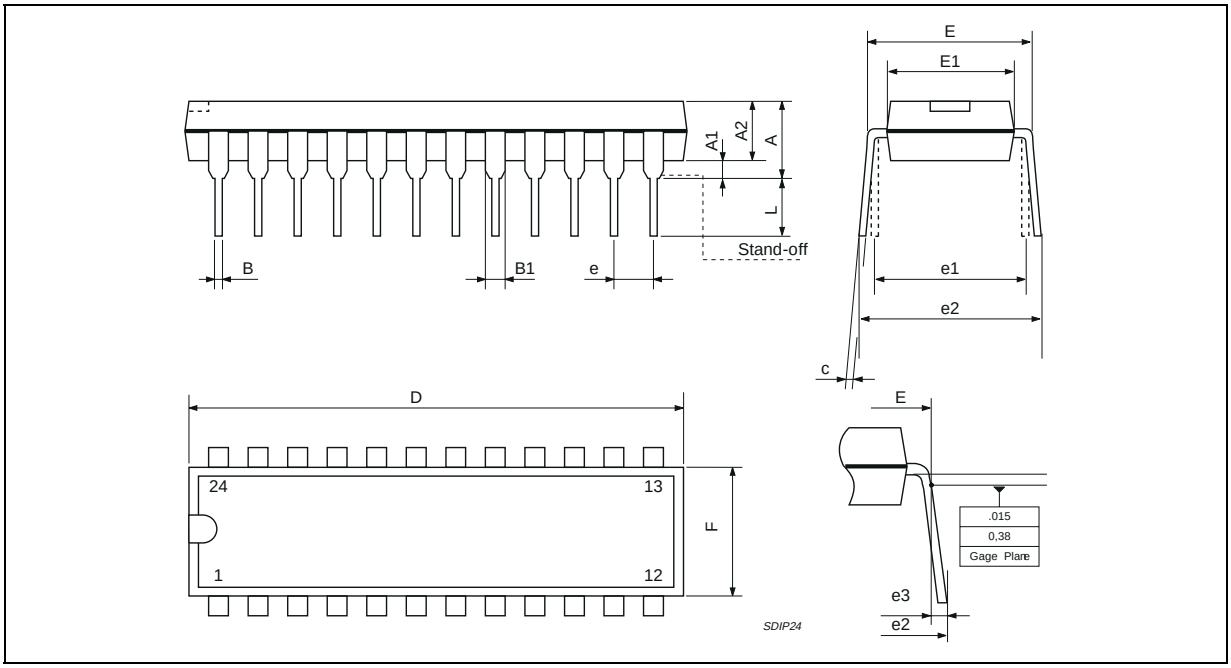


Figure 20



PACKAGE MECHANICAL DATA

24 PINS - PLASTIC DIP (SHRINK)



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.08			0.20
A1	0.51			0.020		
A2	3.05	3.30	4.57	0.120	0.130	0.180
B	0.36	0.46	0.56	0.0142	0.0181	0.0220
B1	0.76	1.02	1.14	0.030	0.040	0.045
C	0.23	0.25	0.38	0.0090	0.0098	0.0150
D	22.61	22.86	23.11	0.890	0.90	0.910
E	7.62		8.64	0.30		0.340
E1	6.10	6.40	6.86	0.240	0.252	0270
e		1.778			0.070	
e1		7.62			0.30	
e2			10.92			0.430
e3			1.52			0.060

SDIP24.TBL