

# DATA SHEET

## **TDA9177** YUV transient improvement processor

Product specification  
Supersedes data of 1996 Jun 28  
File under Integrated Circuits, IC02

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## YUV transient improvement processor

## TDA9177

### FEATURES

- Can be used in  $1f_H$  and  $2f_H$  applications
- Luminance step improvement
- Line width control
- Smart peaking for detail enhancement
- Embedded feature reduction facility for smart noise control
- Compensating chrominance delay
- YUV interface
- Two additional pins for access to 6-bit ADC and I<sup>2</sup>C-bus
- Versatile I<sup>2</sup>C-bus and pin control for user adjustments.



In combination with the TDA9170, it builds a high performance and intelligent picture improvement solution.

The sharpness processor provides 1D luminance step improvement and detail enhancement by smart peaking, suitable for both  $1f_H$  and  $2f_H$  applications. The TDA9177 can be used as a cost effective alternative to (but also in combination with) Scan Velocity Modulation (SVM).

### GENERAL DESCRIPTION

The TDA9177 is an I<sup>2</sup>C-bus controlled sharpness improvement IC with additional inputs for 6-bit analog-to-digital conversion to facilitate additional parameter measurement (e.g. ambient light control). It should preferably be used in front of an RGB video signal processor with YUV interface.

An on-board 6-bit Analog-to-Digital Converter (ADC) can be used for interfacing two analog, low frequency voltage signals to the I<sup>2</sup>C-bus.

The supply voltage is 8 V. The TDA9177 is mounted in a 24-pin SDIP envelope.

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{CC}$	supply voltage		7.2	8.0	8.8	V
$V_{i(Y)}$	luminance input voltage	AMS = LOW	–	0.315	0.42	V
		AMS = HIGH	–	1.0	1.33	V
$V_{i(UV)}$	UV input voltage		–	–	1.9	V
$V_{FS(ADC)}$	full scale ADC input voltage		–	$0.5V_{ref}$	–	V
$V_{ref}$	reference voltage		3.90	4.05	4.20	V

### ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9177	SDIP24	plastic shrink dual in-line package; 24 leads (400 mil)	SOT234-1

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BLOCK DIAGRAM

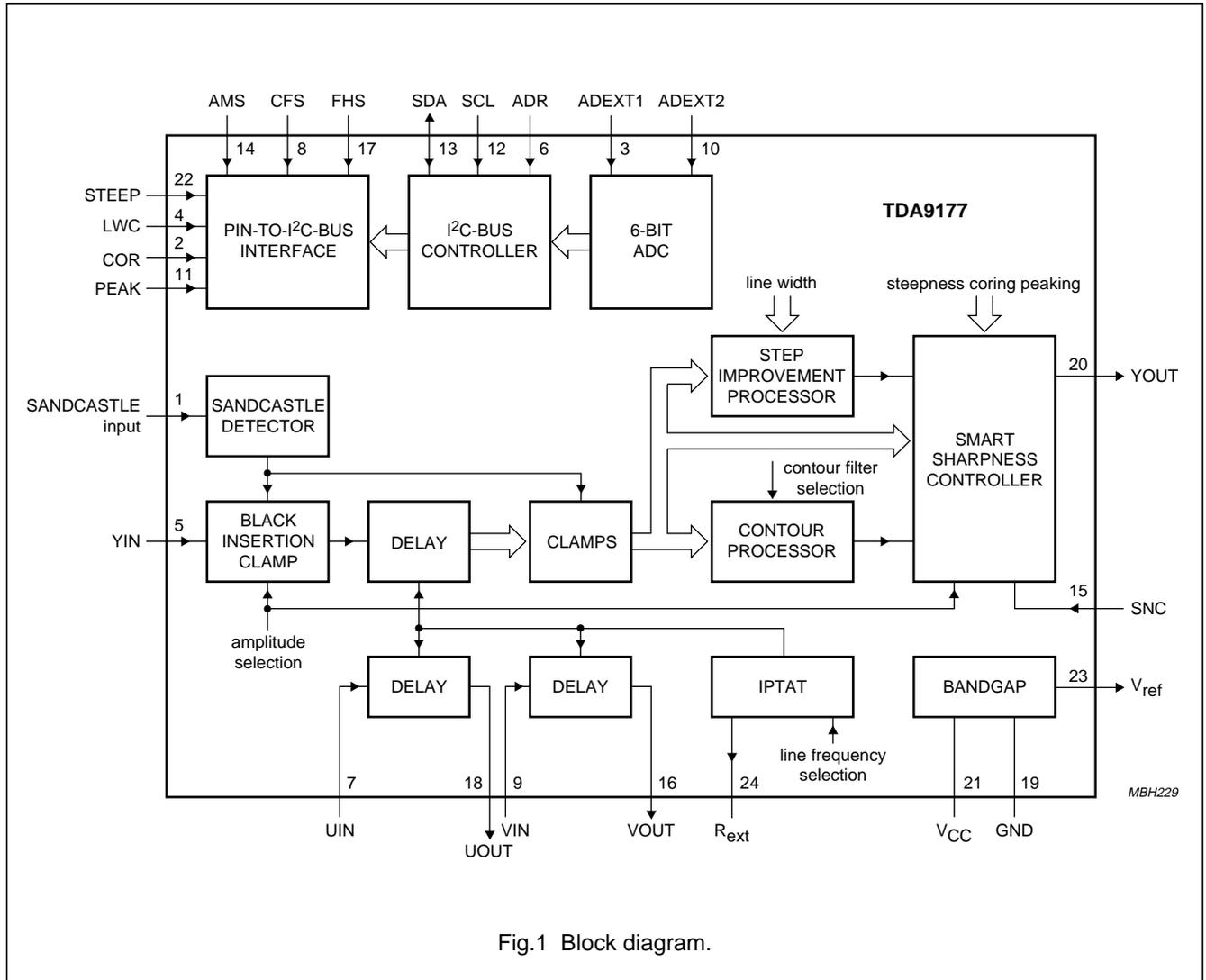


Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
SANDCASTLE	1	sandcastle input
COR	2	coring level input
ADEXT1	3	ADC input 1
LWC	4	line width control input
YIN	5	luminance input
ADR	6	I <sup>2</sup> C-bus address input
UIN	7	colour U input
CFS	8	contour filter select input
VIN	9	colour V input
ADEXT2	10	ADC input 2
PEAK	11	peaking amplitude input
SCL	12	serial clock input (I <sup>2</sup> C-bus)
SDA	13	serial data input/output (I <sup>2</sup> C-bus)
AMS	14	amplitude select input
SNC	15	smart noise control input
VOUT	16	colour V output
FHS	17	line frequency select input
UOUT	18	colour U output
GND	19	system ground
YOUT	20	luminance output
V <sub>CC</sub>	21	supply voltage
STEEP	22	steepness control input
V <sub>ref</sub>	23	reference voltage output
R <sub>ext</sub>	24	resistor reference

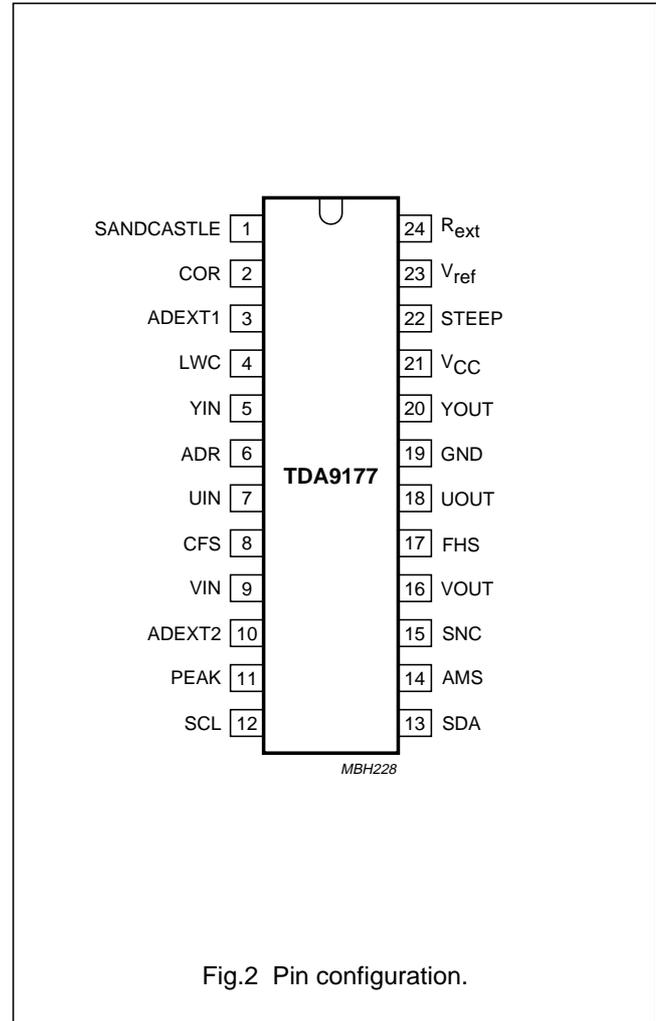


Fig.2 Pin configuration.

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### FUNCTIONAL DESCRIPTION

#### Y-input selection and amplification

The dynamic range of the luminance input amplifier and output amplifier can be switched between 0.315 V and 1.0 V typically (excluding sync), either externally (pin AMS) or by I<sup>2</sup>C-bus (bit AMS of the control register). Amplitudes outside the corresponding maximum specified range will be clipped smoothly. The sync part is processed transparently to the output, independently of the feature settings. The input is clamped during the HIGH period of the CLP, defined by the sandcastle reference, and should be DC-decoupled with an external capacitor. During the clamp pulse, an artificial black level is inserted in the input signal to correctly preset the internal circuitry.

The input amplifier drives a delay line of four delay sections, which form the core of the sharpness improvement processor.

#### Sharpness improvement processor

The sharpness improvement processor increases the slope of large luminance transients of vertical objects and enhances transients of details in natural scenes by contour correction. It comprises three main processing units, these being the step improvement processor, the contour processor and the smart sharpness controller.

#### STEP IMPROVEMENT PROCESSOR

The step improvement processor (see Fig.9) comprises two main functions:

1. the MINMAX generator
2. the MINMAX fader.

The MINMAX generator utilizes 5 taps of an embedded luminance delay line to calculate the minimum and maximum envelope of all signals momentarily stored in the delay line. The MINMAX fader chooses between the minimum and maximum envelopes, depending on the polarity of a decision signal derived from the contour processor. Figures 4, 5 and 6 show some waveforms of the step improvement processor and illustrate that fast transients result with this algorithm. The MINMAX generator also outputs a signal that represents the momentary envelope of the luminance input signal. This envelope information is used by the smart sharpness controller.

Limited line width control (also called aperture control) can be performed externally (pin 4, LWC) or by I<sup>2</sup>C-bus (LW-DAC). Line width control can be used to compensate

for horizontal geometry because of the gamma or blooming of the spot of the CRT.

#### THE CONTOUR PROCESSOR

The contour processor comprises two contour generators with different frequency characteristics. The contour generator generates a second-order derivative of the incoming luminance signal and is used both as a decision signal for the step improvement processor and as a luminance correction signal for the smart sharpness controller. In the smart sharpness controller, this correction signal is added to the proper delayed original luminance input signal, making up the peaking signal for detail enhancement. The peaking path is allowed to select either the narrow- or wide-peaked contour generators either externally (pin 8, CFS) or by I<sup>2</sup>C-bus (bit CFS in the control register). The step improvement circuitry always selects the wide-peaked contour filter.

The contour generators utilize 3 taps (narrow band) or 5 taps (broad band) of the embedded luminance delay lines. Figures 11 and 12 illustrate the normalized frequency transfer of both the narrow and wide contour filters.

#### SMART SHARPNESS CONTROLLER

The smart sharpness controller (see Fig.10) is a fader circuit that fades between peaked luminance and step-improved luminance, defined by the output of a step discriminating device known as the step detector. It also contains a variable coring level stage.

The step detector behaves like a band-pass filter, so both amplitude of the step and its slope add to the detection criterion. The smart sharpness controller has four user controls:

1. Steepness control
2. Peaking control
3. Coring level control
4. Smart Noise control.

Control settings can be performed either by the I<sup>2</sup>C-bus or externally by pin, depending on the status of the I<sup>2</sup>C-bus bit STB.

The steepness setting controls the amount of steepness in the edge-correction processing path. The peaking setting controls the amount of contour correction for proper detail enhancement.

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The envelope signal generated by the step improvement processor modulates the peaking setting in order to reduce the amount of peaking for large sine excursions see Figs 7 and 8.

The coring setting controls the coring level in the peaking path for rejection of high-frequency noise. All three settings facilitate reduction of the impact of the sharpness features, e.g. for noisy luminance signals.

An external noise detector and a user-preferred noise algorithm are needed to make a fully automatic I<sup>2</sup>C-bus controlled smart sharpness control.

An on-board, hard-wired smart sharpness algorithm can be executed by driving pin SNC with the output of an external noise detector. This pin, however, is active both in I<sup>2</sup>C-bus and pin mode. Figures 13 and 14 illustrate the impact of the noise control voltage at pin SNC on the user settings.

Figure 15 shows the relationship between the feature settings STEEP, COR, PEAK, LWC and their corresponding pin voltages.

### Chrominance compensation

The chrominance delay lines compensate for the delay of the luminance signal in the step improvement processor, to ensure a correct colour fit. No delay compensation will be performed in the chrominance path for line-width corrections in the luminance path.

### Successive approximation ADC

Pins ADEXT1 and ADEXT2 are connected to a 6-bit successive approximation ADC, via a multiplexer. The multiplexer toggles between the inputs with each field.

For each field flyback, a conversion is started for either of the two inputs and the result is stored in the corresponding bus register, ADEXT1 or ADEXT2.

In this way, any analog, slowly varying signal can be given access to the I<sup>2</sup>C-bus. If a register access conflict occurs, the data of that register is made invalid by setting the flag bit DV (Data Valid) to zero.

### I<sup>2</sup>C-bus

At power up, the bit STB (standby) in the control register is reset, to leave control to the pins. However, the I<sup>2</sup>C-bus is at standby and responds if properly addressed. By setting STB to logic 1, the control of all features is instead left to the I<sup>2</sup>C-bus registers. The PDD bit (Power Down Detected) in the status register is set each time an interruption of the supply power occurs and is reset only by reading the status register. A 3-bit identification code can also be read from the status register, which can be used to automatically configure the application by software.

The input control registers can be written sequentially by the I<sup>2</sup>C-bus by the embedded automatic subaddress increment feature or by addressing it directly. The output control functions cannot be addressed separately. Reading out the output control functions always starts at subaddress 00 and all subsequent words are read out by the automatic subaddress increment procedure. The I<sup>2</sup>C address is 40H if pin 6 (ADR) is connected to ground and E0H if pin 6 (ADR) is connected to pin 23 (V<sub>ref</sub>).

### I<sup>2</sup>C-bus specification

#### Slave address

A6	A5	A4	A3	A2	A1	A0	R/W
ADR	1	ADR	0	0	0	0	X

Auto-increment mode available for subaddresses.

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## Control functions

FUNCTIONS	TYPE	SUBADDRESS	DATA BYTE								
			D7	D6	D5	D4	D3	D2	D1	D0	
<b>Inputs</b>											
Control	REG	00	X	X	X	X	CFS	FHS	AMS	STB	
Peaking	DAC	01	X	X	PK5	PK4	PK3	PK2	PK1	PK0	
Steepness	DAC	02	X	X	SP5	SP4	SP3	SP2	SP1	SP0	
Coring	DAC	03	X	X	CR5	CR4	CR3	CR2	CR1	CR0	
Line width	DAC	04	X	X	LW5	LW4	LW3	LW2	LW1	LW0	
<b>Outputs</b>											
Status	REG	00	0	0	0	0	ID2	ID1	ID0	PDD	
ADEXT1 (output)	REG	01	0	DV	AD5	AD4	AD3	AD2	AD1	AD0	
ADEXT2 (output)	REG	02	0	DV	AD5	AD4	AD3	AD2	AD1	AD0	

### INPUT SIGNALS

**Table 1** Address selection

ADR	FUNCTION
0	I <sup>2</sup> C address is 40H
1	I <sup>2</sup> C address is E0H

**Table 2** Standby

STB	FUNCTION
0	pin mode
1	I <sup>2</sup> C-bus mode

**Table 3** Amplitude selection

AMS	FUNCTION
0	0.315 V luminance
1	1.0 V luminance

**Table 4** Line frequency selection

FHS	FUNCTION
0	1f <sub>H</sub>
1	2f <sub>H</sub>

**Table 5** Contour filter selection

CFS	FUNCTION
0	narrow contour filter
1	wide contour filter

**Table 6** Peaking amplitude

PK5 to PK0	FUNCTION
000000	0%
111111	100%

**Table 7** Steepness correction

SP5 to SP0	FUNCTION
000000	0%
111111	100%

**Table 8** Coring level

CR5 to CR0	FUNCTION
000000	0%
111111	100%

**Table 9** Line width correction

LW5 to LW0	FUNCTION
000000	0%
111111	100%

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## OUTPUT SIGNALS

**Table 10** Power Down Detection (PDD)

PDD	FUNCTION
0	no power down detected since last read action
1	power down detected

**Table 11** Identification  
(version number or derivative type)

ID2 to ID0	FUNCTION
000	TDA9177/N1

**Table 12** Data valid of ADC registers

DV	FUNCTION
0	data not valid because of possible register access collision
1	data valid

**Table 13** Bits AD5 to AD0

AD5 to AD0	FUNCTION
000000B	0 V
111111B	$0.5V_{ref}$

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	supply voltage		-0.5	+8.8	V
$V_i$	input voltage on any input		-0.5	$V_{CC} + 0.5$	V
$V_o$	output voltage of any output		-0.5	$V_{CC} + 0.5$	V
$T_{stg}$	storage temperature		-55	+150	°C
$T_{amb}$	operating ambient temperature		-10	+70	°C

## QUALITY SPECIFICATION

Quality level in accordance with "SNW-FQ-611 part E".

All pins are protected against ESD by means of internal clamping diodes. The protection circuit meets the specification:

Human body model (100 pF, 1500  $\Omega$ ): All pins >3000 V.Machine model (200 pF, 0  $\Omega$ ): All pins >300 V.

Latch-up:

At an ambient temperature of 70 °C, all pins meet the specification:

 $I_{trigger} > 100 \text{ mA}$  or  $V_{pin} > 1.5V_{CC(max)}$  $I_{trigger} < -100 \text{ mA}$  or  $V_{pin} < -0.5V_{CC(max)}$ 

## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	<59	K/W

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**CHARACTERISTICS** $V_{CC} = 8\text{ V}$ ;  $R_{ref} = 10\text{ k}\Omega \pm 2\%$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ ; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supplies</b>						
MAIN SUPPLY $V_{CC}$ (PIN 21)						
$V_{CC}$	supply voltage		7.2	8.0	8.8	V
$I_{CC}$	supply current	1f <sub>H</sub> mode	–	40	–	mA
		2f <sub>H</sub> mode	–	45	–	mA
REFERENCE SUPPLY $V_{ref}$ (PIN 23)						
$V_{ref}$	reference supply voltage		3.90	4.05	4.20	V
$I_{L(max)}$	maximum load current		1.0	–	–	mA
RESISTOR REFERENCE $R_{ext}$ (PIN 24)						
$V_{Rref}$	resistor supply voltage		–	2	–	V
$R_{ref}$	resistor value		–	10	–	k $\Omega$
<b>Luminance input/output selection</b>						
LUMINANCE INPUT YIN (PIN 5)						
$V_{i(Y)}$	luminance input voltage	AMS = LOW	–	0.315	0.42	V
		AMS = HIGH	–	1.0	1.33	V
$V_{i(Yclamp)}$	luminance input voltage level during clamping		–	4.0	–	V
$I_{ib(Y)}$	luminance input bias current	no clamp	–	–	0.1	$\mu\text{A}$
LUMINANCE INPUT VOLTAGE RANGE SELECTION AMS (PIN 14); note 1						
$V_{AMSL}$	input voltage for low luminance range		–	–	0.5	V
$V_{AMSH}$	input voltage for high luminance range		3.5	–	5.5	V

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>LUMINANCE OUTPUT YOUT (PIN 20)</b>						
$V_{o(Y)}$ (p-p)	luminance output voltage, peak-to-peak	AMS = LOW	–	0.315	–	V
		AMS = HIGH	–	1.0	–	V
$V_{o(Yclamp)}$	luminance output voltage during clamping	AMS = LOW	–	2.35	–	V
		AMS = HIGH	–	2	–	V
S/N(Y)	luminance output signal-to-noise ratio		52	–	–	dB
$B_Y$	luminance bandwidth	1f <sub>H</sub> mode (–1 dB); transparent; note 2	5	–	–	MHz
		2f <sub>H</sub> mode (–1 dB); transparent; note 2	10	–	–	MHz
$E_{bl}$	black level error	transparent; note 3	–	0	1.0	%
$E_{G(n)}$	nominal gain error	transparent	–	0	5	%
$R_{out}$	output resistance		–	–	150	Ω
$I_{ob}$	output bias current		1.3	–	–	mA
<b>Step improvement</b>						
<b>GENERAL</b>						
$t_{r(min)}$	minimum rise time 10% to 90%	1f <sub>H</sub> mode; note 4	–	20	–	ns
		2f <sub>H</sub> mode; note 4	–	20	–	ns
<b>LINE WIDTH CONTROL</b>						
$\delta_{(min)}$	minimum duty factor	2 MHz	–	33	–	%
$\delta_{(max)}$	maximum duty factor	2 MHz	–	67	–	%
$t_{sd(max)}$	maximum step displacement	1f <sub>H</sub> mode	–	140	–	ns
		2f <sub>H</sub> mode	–	70	–	ns
<b>LINE-WIDTH CONTROL LWC (PIN 4); note 1</b>						
$V_{i(min)}$	input voltage for minimum line width		–	–	37.5	%V <sub>ref</sub>
$V_{i(max)}$	input voltage for maximum line width		87.5	–	137.5	%V <sub>ref</sub>
$I_{bias}$	input bias current		–	0.5	–	μA
<b>Contour processing</b>						
<b>CONTOUR FILTER NARROW-PEAKED</b>						
$f_{pc}$	peaking centre frequency	1f <sub>H</sub>	–	3.57	–	MHz
		2f <sub>H</sub>	–	7.14	–	MHz
<b>CONTOUR FILTER WIDE-PEAKED</b>						
$f_{pc1}$	peaking centre frequency	1f <sub>H</sub>	–	4.14	–	MHz
		2f <sub>H</sub>	–	8.28	–	MHz
$Q_{max}$	maximum contour amplitude at centre frequency	note 5	–	12	–	dB

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CONTOUR FILTER SELECTION CFS (PIN 8); note 1						
$V_{i(ncf)}$	input voltage for narrow contour filter		–	–	0.5	V
$V_{i(wcf)}$	input voltage for wide contour filter		3.5	–	5.5	V
<b>Smart sharpness controller</b>						
STEP DETECTOR						
$f_{dc}$	detection centre frequency	$1f_H$	–	2.13	–	MHz
		$2f_H$	–	4.26	–	MHz
CORING						
$Q_{smcL}$	minimum coring level	note 6	–	0	–	%
$Q_{smcH}$	maximum coring level	note 6	–	22	–	%
CORING LEVEL CONTROL COR (PIN 2); note 1						
$V_{i(min)}$	input voltage for minimum coring		–	–	37.5	% $V_{ref}$
$V_{i(max)}$	input voltage for maximum coring		87.5	–	137.5	% $V_{ref}$
$I_{bias}$	input bias current		–	–	0.5	$\mu A$
PEAKING LEVEL CONTROL PEAK (PIN 11); note 1						
$V_{i(min)}$	input voltage for minimum peaking		–	–	37.5	% $V_{ref}$
$V_{i(max)}$	input voltage for maximum peaking		87.5	–	137.5	% $V_{ref}$
$I_{bias}$	input bias current		–	–	0.5	$\mu A$
STEEPNESS LEVEL CONTROL STEEP (PIN 22); note 1						
$V_{i(min)}$	input voltage for minimum steepness		–	–	37.5	% $V_{ref}$
$V_{i(max)}$	input voltage for maximum steepness		87.5	–	137.5	% $V_{ref}$
$I_{bias}$	input bias current		–	–	0.5	$\mu A$
SMART NOISE CONTROL SNC (PIN 15)						
$V_{nfr}$	level for no feature reduction		–	0.0	–	V
$V_{cfr}$	level for complete feature reduction		–	$V_{ref}$	–	V
$I_{bias}$	input bias current		–	–	1.0	$\mu A$
<b>Overall group delay performance for luminance</b>						
$t_d$	delay time from input to output	$1f_H$ mode	–	175	–	ns
		$2f_H$ mode	–	108	–	ns
$t_{de}$	delay error contour correction	$1f_H$ mode; note 7	–	0	10	ns
		$2f_H$ mode; note 7	–	0	5	ns
$t_{de1}$	delay error step correction	$1f_H$ mode; note 7	–	0	10	ns
$t_{de2}$	delay error step correction	$2f_H$ mode	–	0	5	ns

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DELAY TIME SELECTION FHS (PIN 17); note 1						
$V_{i1fH}$	input voltage for $1f_H$		–	–	0.5	V
$V_{i2fH}$	input voltage for $2f_H$		3.5	–	5.5	V
<b>Colour difference processing</b>						
COLOUR DIFFERENCE INPUTS UIN AND VIN (PINS 7 AND 9)						
$V_{iUIN(p-p)}$	input voltage range UIN, peak-to-peak		1.9	–	–	V
$V_{iVIN(p-p)}$	input voltage range VIN, peak-to-peak		1.9	–	–	V
$I_{bias}$	input bias current UIN, VIN	no clamp	–	–	0.1	$\mu A$
$V_{cl}$	voltage level during clamping		–	4.0	–	V
COLOUR DIFFERENCE OUTPUTS UOUT AND, VOUT (PINS 18 AND 16)						
$V_{o(cl)}$	output voltage level during clamping		–	3.2	–	V
G	gain		–	1.0	–	
$E_{off}$	offset error	transparent	–	0	1	%
$E_G$	gain error	transparent	–	0	5	%
$E_{G(UV)}$	UV gain tracking error	transparent	–	0	1	%
B	bandwidth	$1f_H$	7	–	–	MHz
		$2f_H$	7	–	–	MHz
$t_d$	delay time	$1f_H$	–	175	–	ns
		$2f_H$	–	108	–	ns
$R_{out}$	output resistance		–	–	150	$\Omega$
$I_{ob}$	output bias current		0.5	–	–	mA
<b>Successive Approximation ADC</b>						
ADEXT1 AND ADEXT2 (PINS 3 AND 10)						
$V_{FS}$	full scale input voltage range	with respect to GND	–	2.0	–	V
$I_{ib}$	input bias current		–	–	1	$\mu A$
	data path		–	6	–	bit
DLE	differential linearity error		–	–	1	LSB
ILE	integral linearity error		–	–	1	LSB
$f_{con}$	conversion frequency	each channel	–	$0.5f_V$	–	Hz
$Q_{adt}$	conversion time (video lines)	each channel	–	8	–	lines

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Timing</b>						
SANDCASTLE INPUT SANDCASTLE (PIN 1)						
$V_{scbn}$	detection level for blank	no clamping	1.25	1.5	1.75	V
$V_{scbc}$	detection level for blank	with clamping and w.r.t. top level sandcastle pulse	–	–0.6	–	V
$t_{scnV}$	input blanking width for no V-sync		–	–	15	$\mu$ s
$t_{scV}$	input blanking width for V-sync		35	–	–	$\mu$ s
$V_{bkvar}$	ripple on sandcastle burst key level		–	–	0.4	V
<b>Overall output group delay performance</b>						
$t_{dm(YUV)}$	delay of matching YUV	$1f_H$	–	0	10	ns
		$2f_H$	–	0	5	ns

**Notes**

1. This selection is only valid when the standby bit STB is **not** set.
2. In transparent mode i.e. no step improvement and no peaking, the bandwidth of the luminance path for which the group delay is constant is 7 MHz in  $1f_H$  mode and 14 MHz in  $2f_H$  mode. However, as the circuit uses all-pass filters, ringing on the output signal may occur if the bandwidth of the input signal is larger than 7 MHz in  $1f_H$  mode or 14 MHz in  $2f_H$  mode. As the step improvement circuit adds harmonics to the luminance signal, the bandwidth of the output signal is much larger than 14 MHz.
3. The black level error that may occur will mainly be caused by inaccuracies in the internal clamping circuit. This internal clamping circuit is activated during 70% of the duration of the burst key pulse on the sandcastle signal. Integration of the 'ramp shaped' black level error during the full duration of the burst key pulse will reduce the black level error to less than 1%.
4. Peaking set to minimum. Input signal is a sine wave with the nominal peak-to-peak amplitude corresponding to the selected input range.
5. The contour signal cannot be measured separately from the luminance input signal. The contour signal is also processed by the smart noise controller. The frequency transfer in the peaking mode of the luminance signal can be derived from the frequency transfer of the selected contour signal, taking into account the summation of the contour signal and the luminance input signal. The frequency transfer is most easily measured by sine excitation with a relatively small signal amplitude of 10% of the selected dynamic range of the luminance input, to avoid interaction with the step detector.
6. The coring level refers to the internally selected contour signal. It is dependent on the contour filter selected and is specified for the corresponding peaking centre frequency. The coring level can not be measured explicitly at the luminance output from a big step or sine excitation, because of its interaction with the step detector.
7. Contour correction and step improvement delays are internal delays and cannot be measured in a straightforward way. Contour correction delay mismatch results in asymmetrical 'ears' with respect to the centre of the transient. Step improvement correction delay mismatch affects the symmetry of the line width control.

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Figures 3 to 8 show the excitation and response of the TDA9177 sharpness improvement processor.

The excitation shown in Fig.3 is a 2T-pulse, followed by a step function. Because the TDA9177 can handle both  $1f_H$  and  $2f_H$  signals, figures illustrating both situations could have been provided. However, as the difference between these two modes (with respect to the TDA9177) is that the time scale of a  $2f_H$  response diagram is half that of a  $1f_H$  response diagram under equal conditions, only the  $1f_H$  figures are shown.

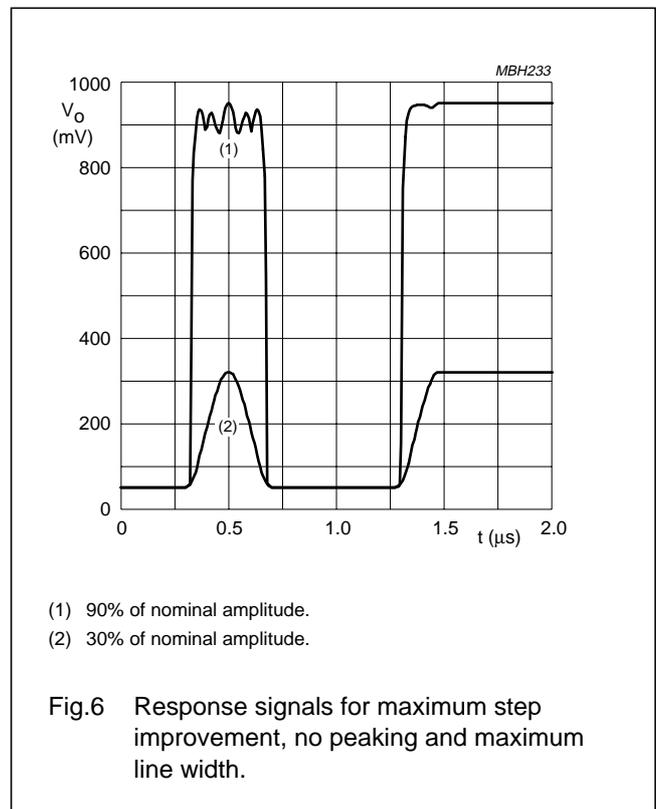
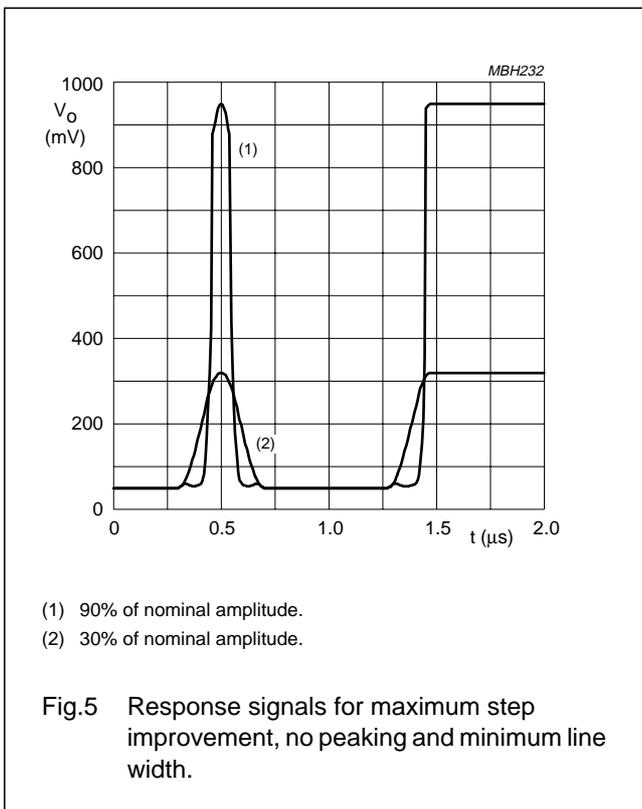
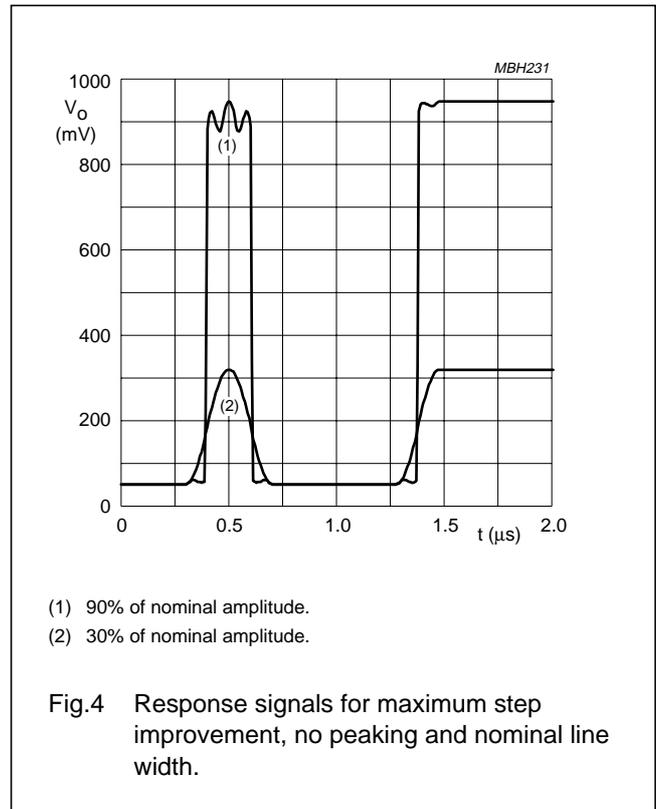
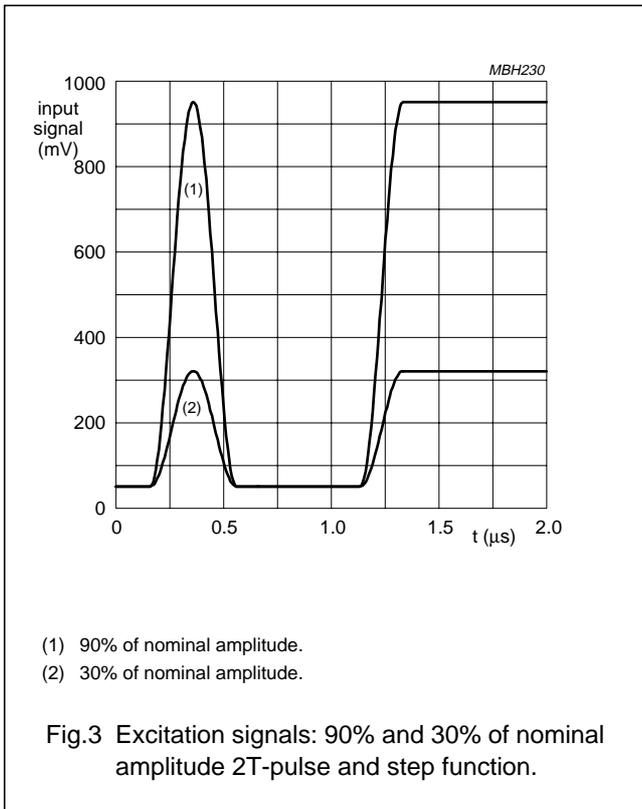
Figure 4 shows that the step improvement processor does not affect small amplitudes. Large transients, however, acquire steeper edges.

Figures 5 and 6 show that the width of the signal processed by the step improvement processor can be modified by the Line Width Control pin LWC (or DACLW). Figure 7 shows that the contour processor does not affect large transients, but works exclusively on small signals, e.g. details in a video signal.

Figure 8 shows the combination of smart peaking and the step improvement processor; small signals will be affected by the contour processor, while large transients will be modified by the step improvement processor.

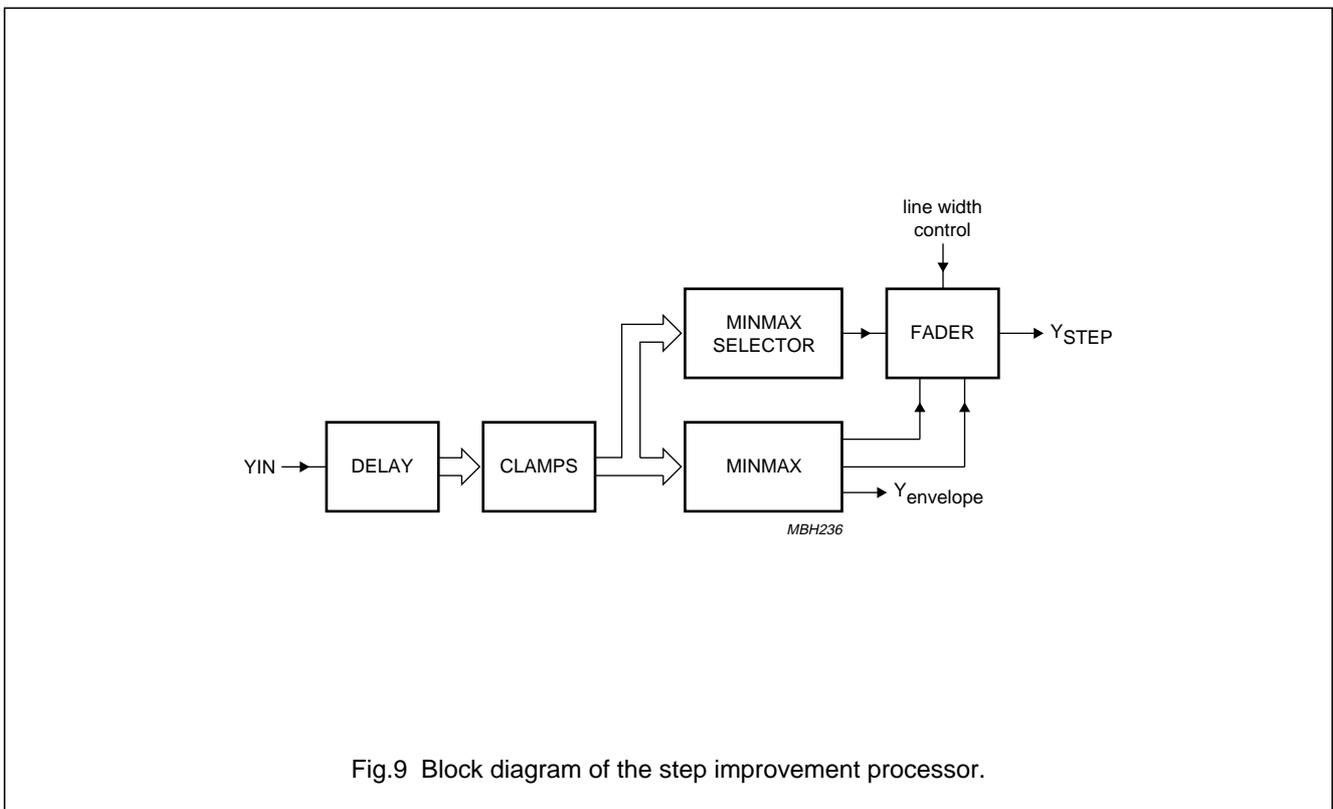
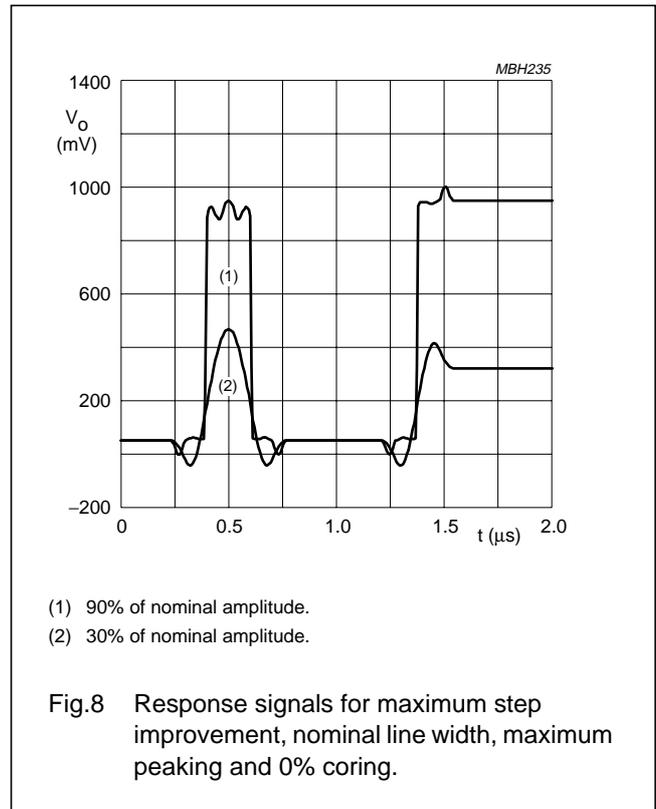
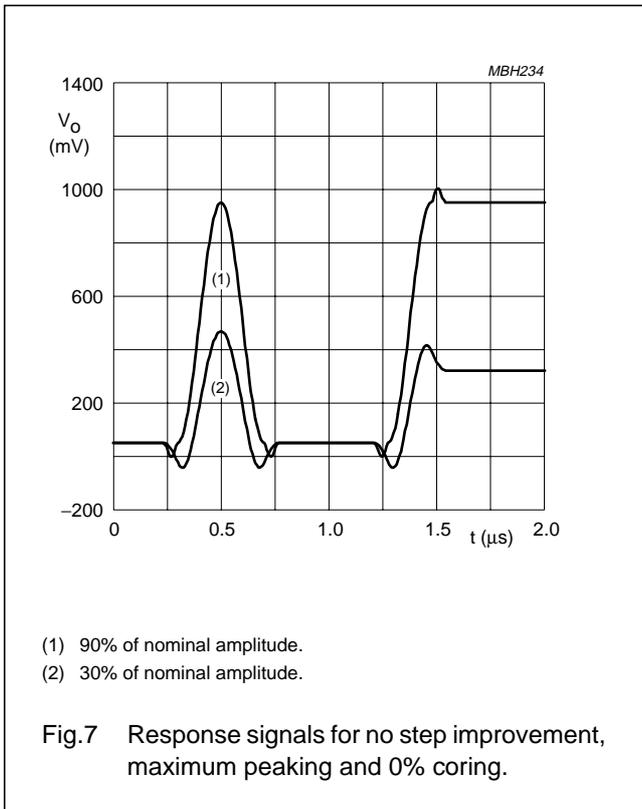
YUV transient improvement processor

TDA9177



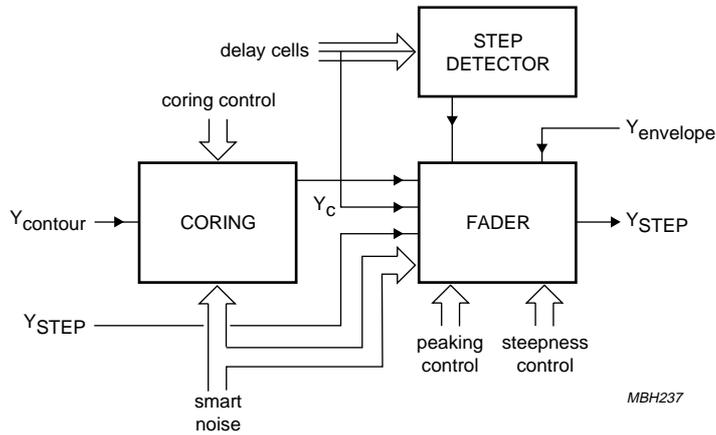
YUV transient improvement processor

TDA9177



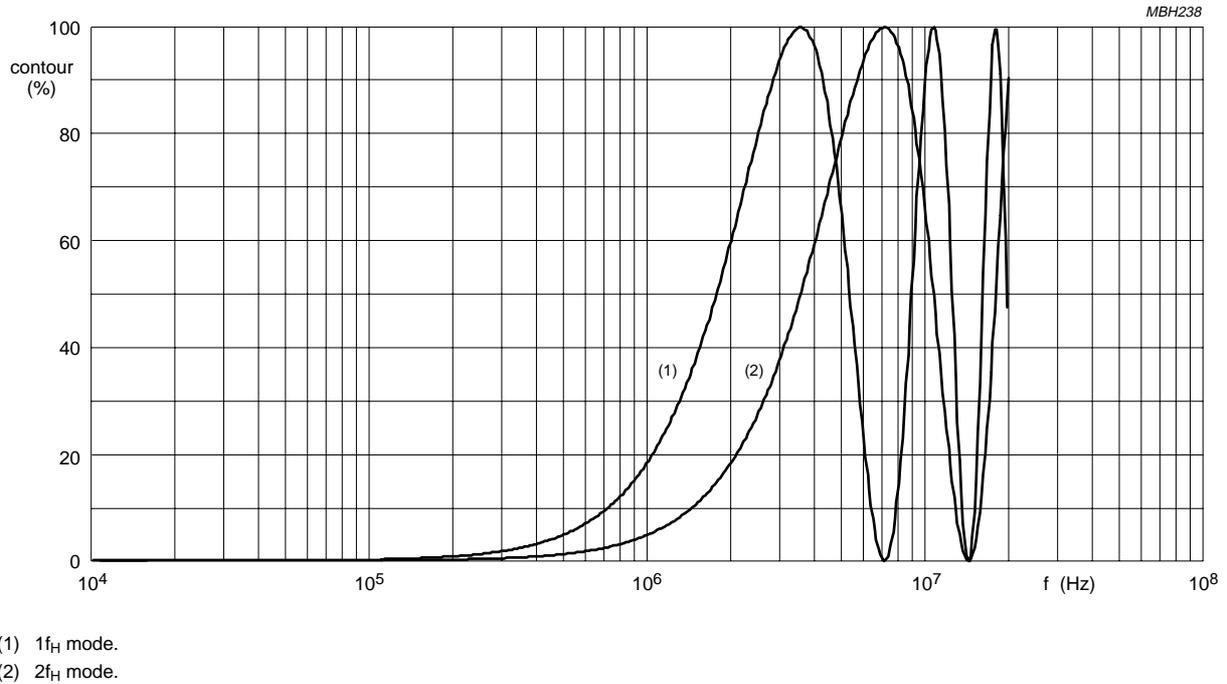
YUV transient improvement processor

TDA9177



MBH237

Fig.10 Block diagram of the smart sharpness controller.



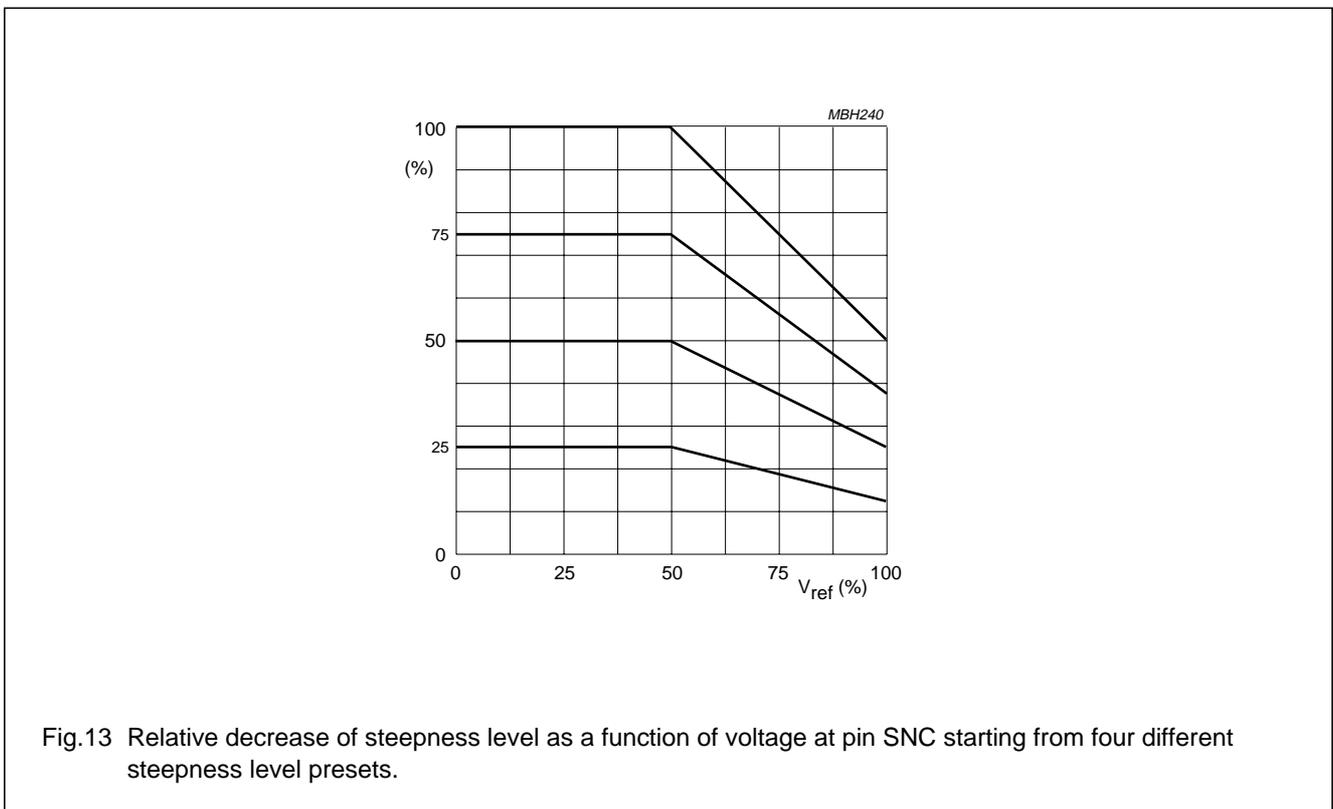
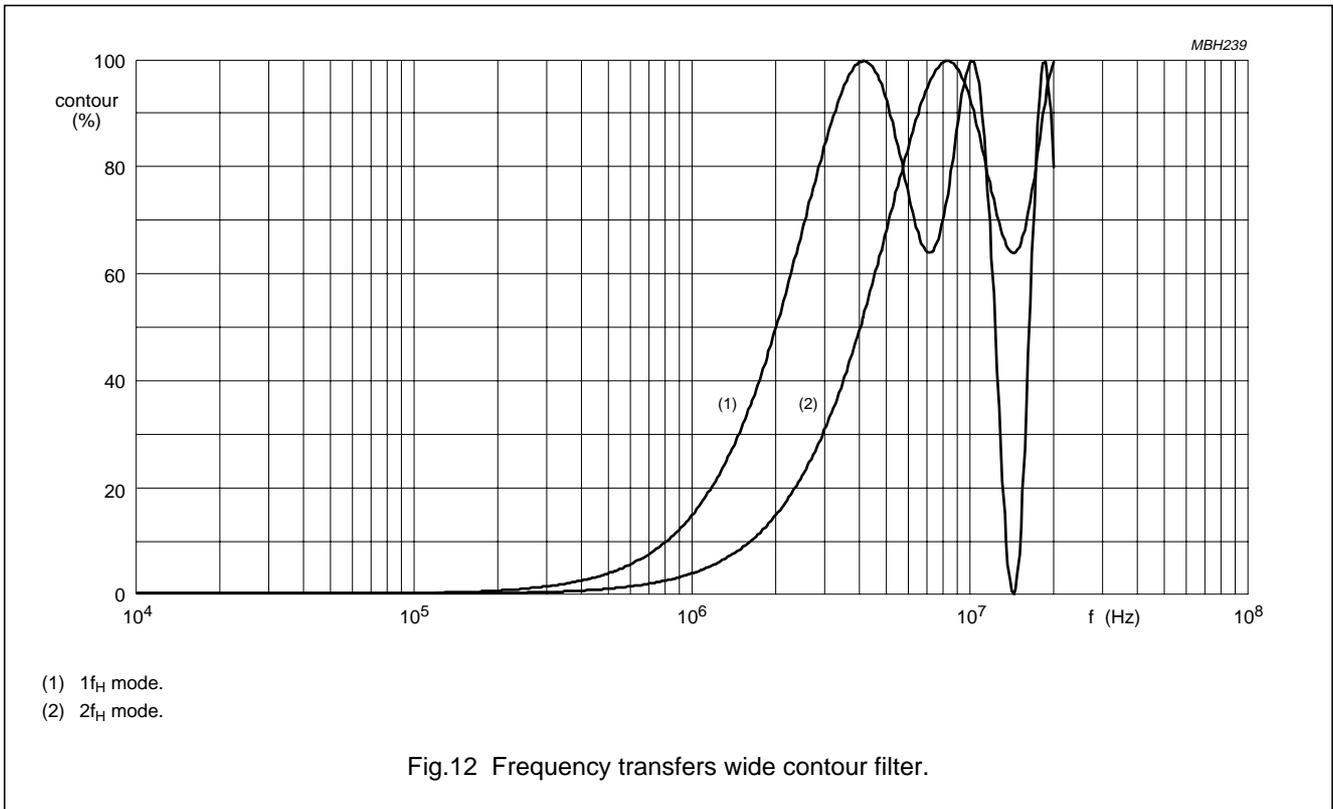
MBH238

- (1)  $1f_H$  mode.
- (2)  $2f_H$  mode.

Fig.11 Frequency transfers narrow contour filter.

YUV transient improvement processor

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YUV transient improvement processor

TDA9177

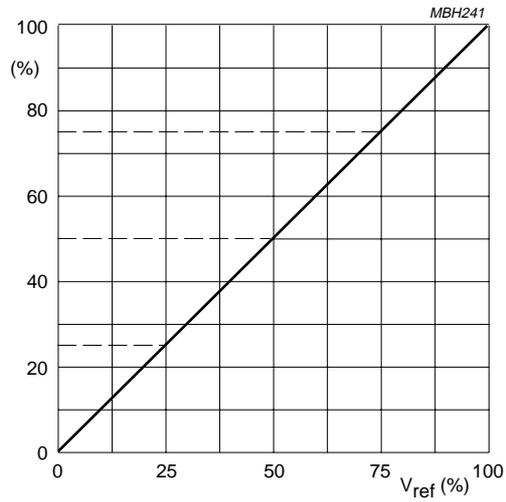


Fig.14 Relative increase of coring level as a function of voltage at pin SNC starting from four different coring level presets.

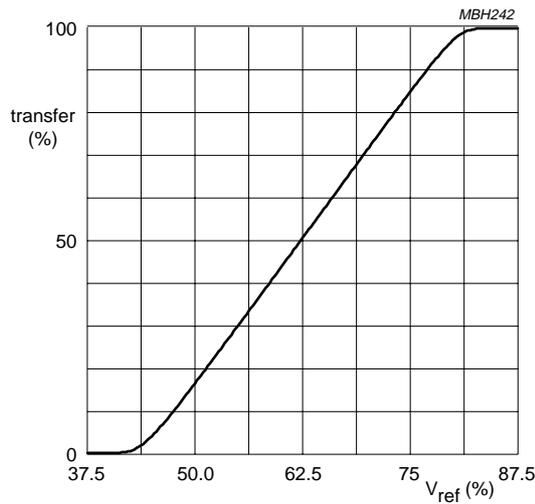
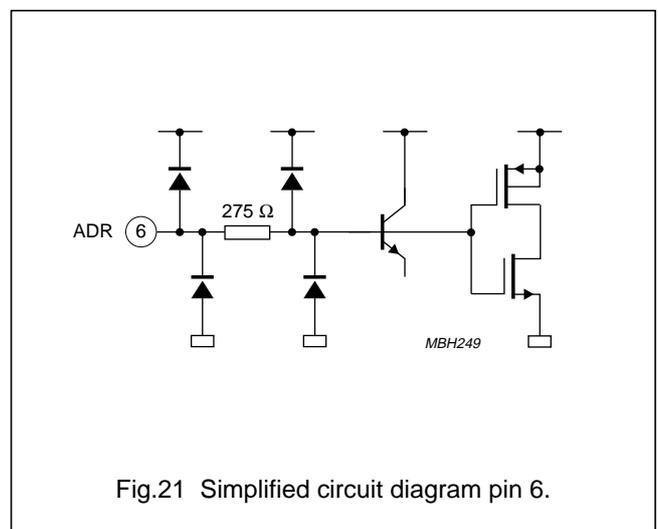
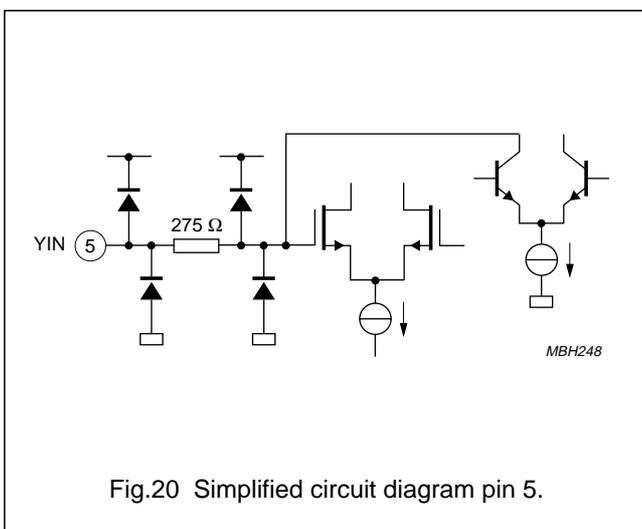
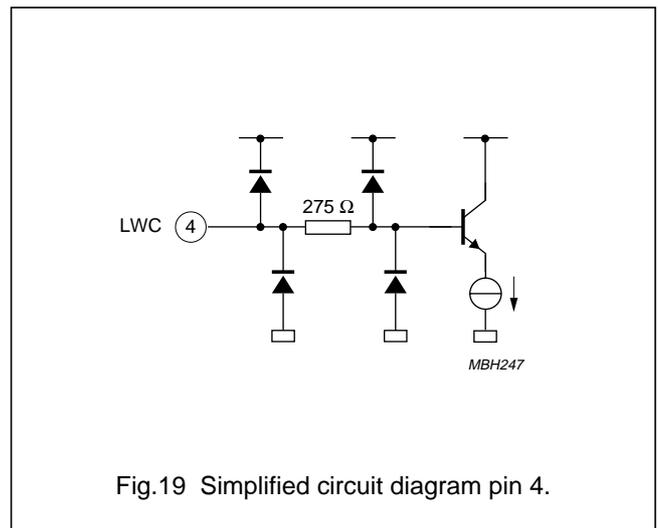
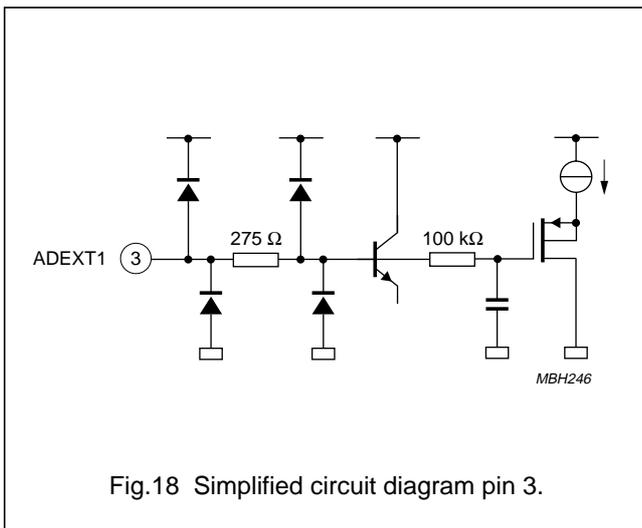
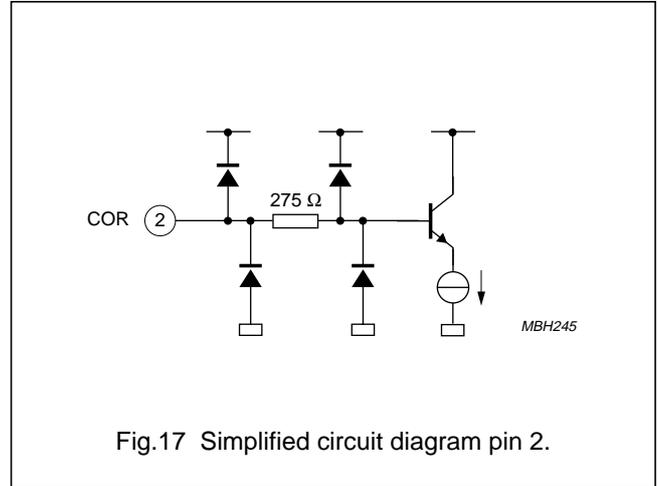
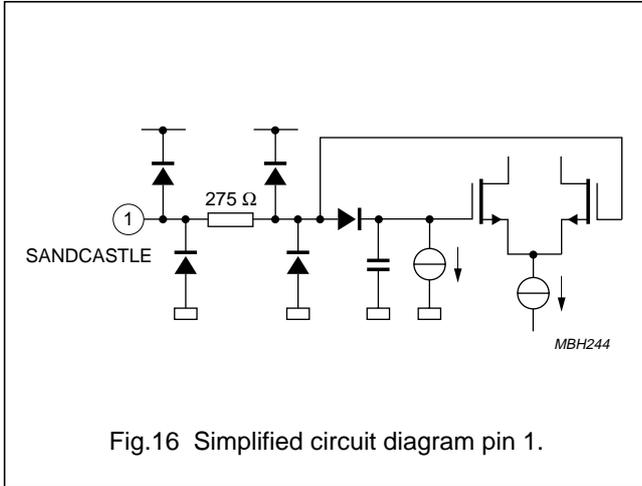


Fig.15 Feature setting control as a function of the pin voltage for peaking, coring, steepness and line width.

YUV transient improvement processor

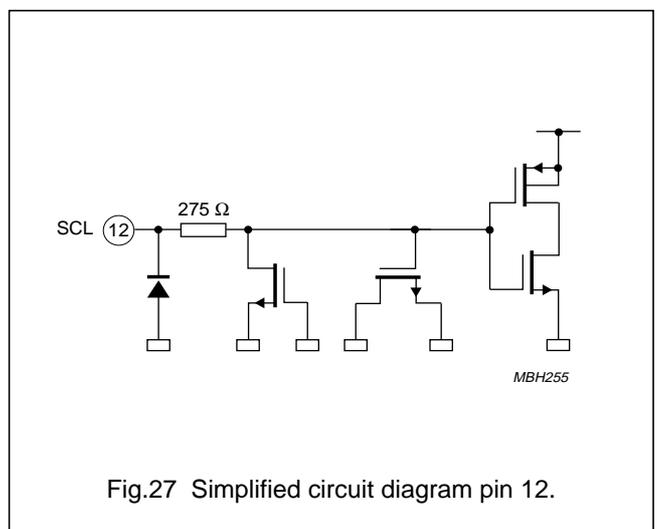
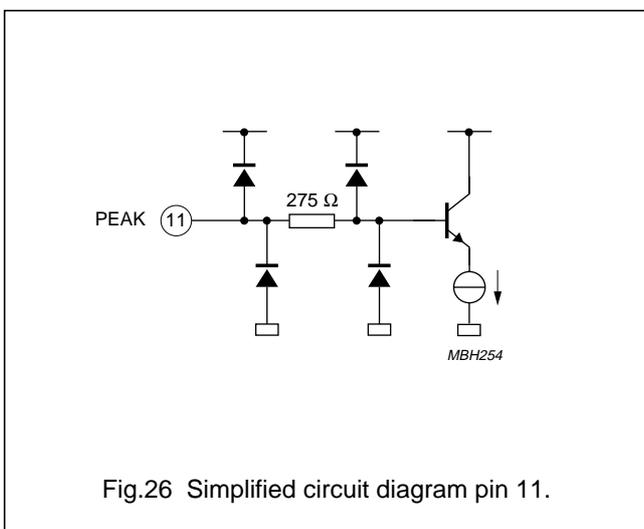
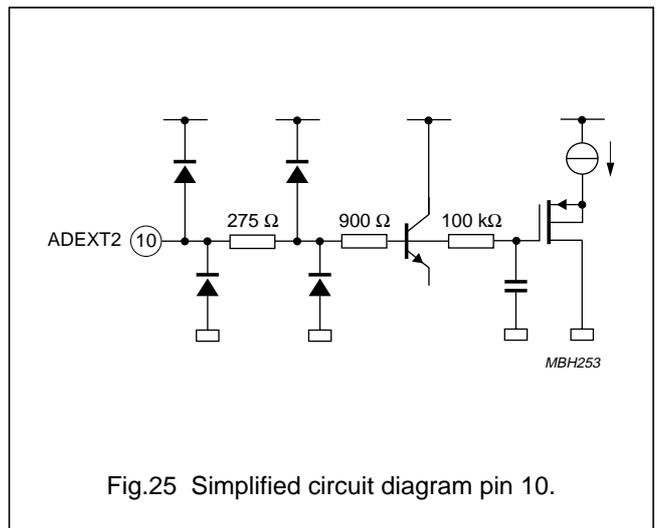
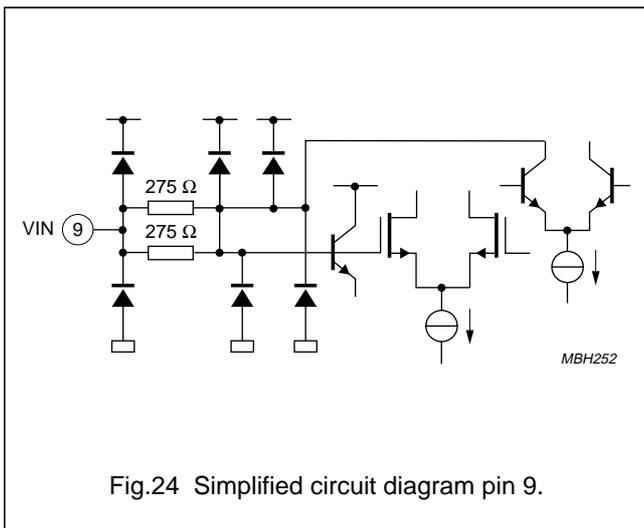
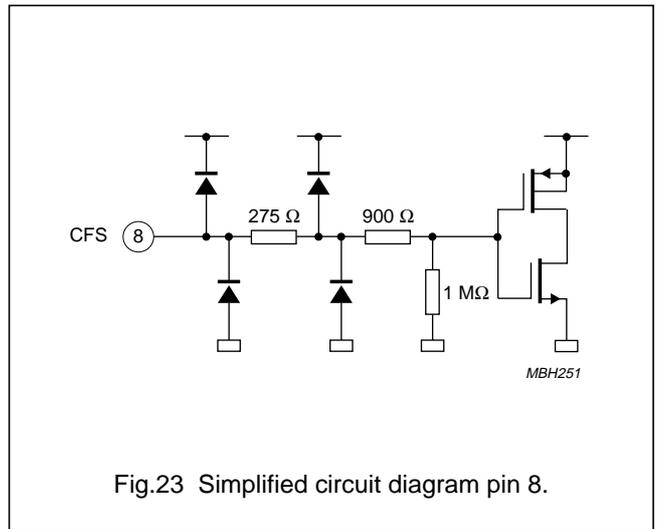
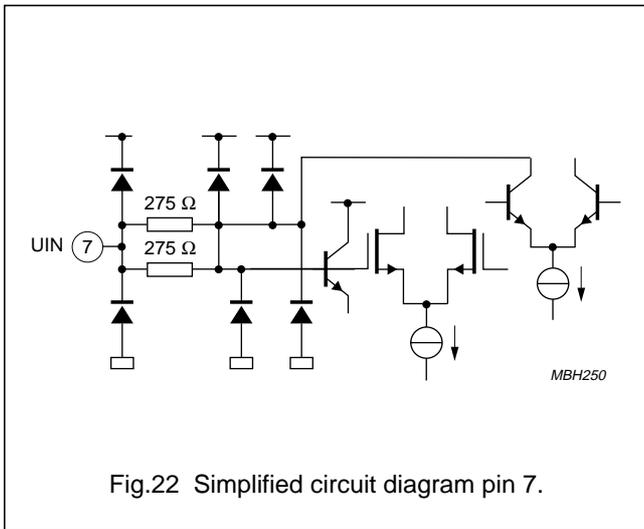
TDA9177

INTERNAL CIRCUITRY



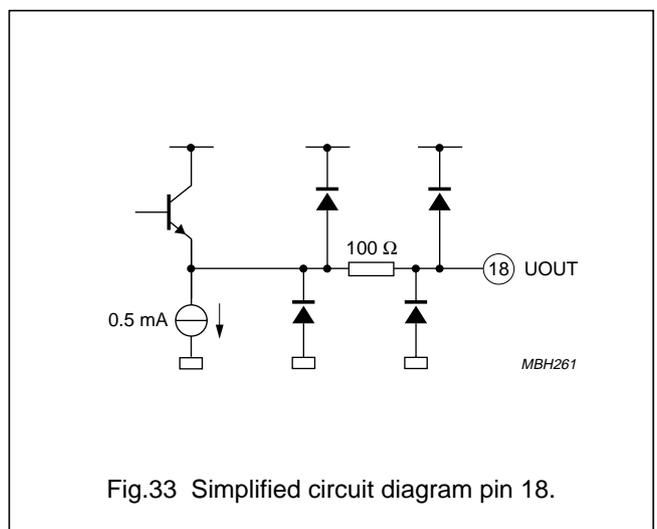
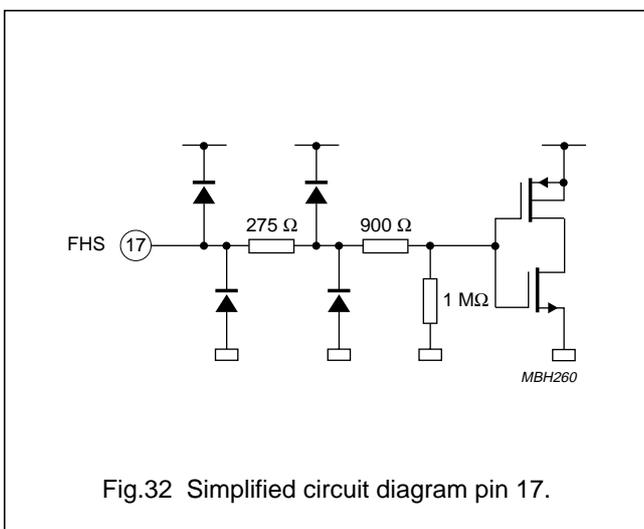
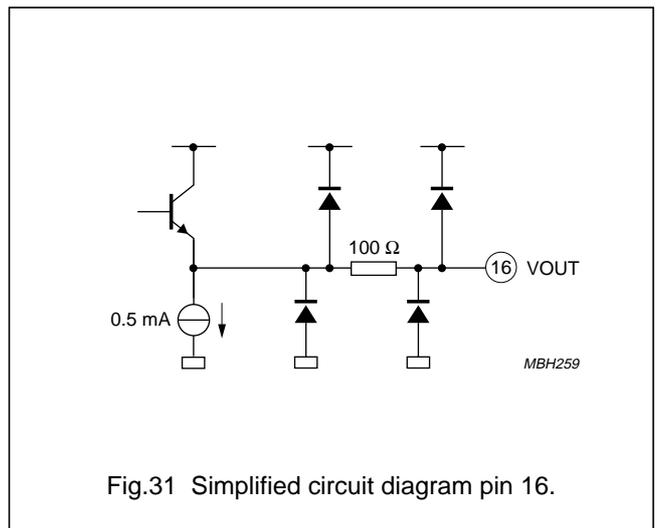
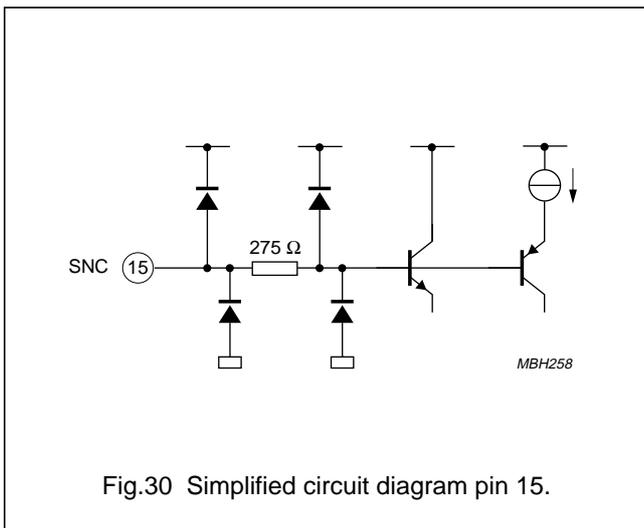
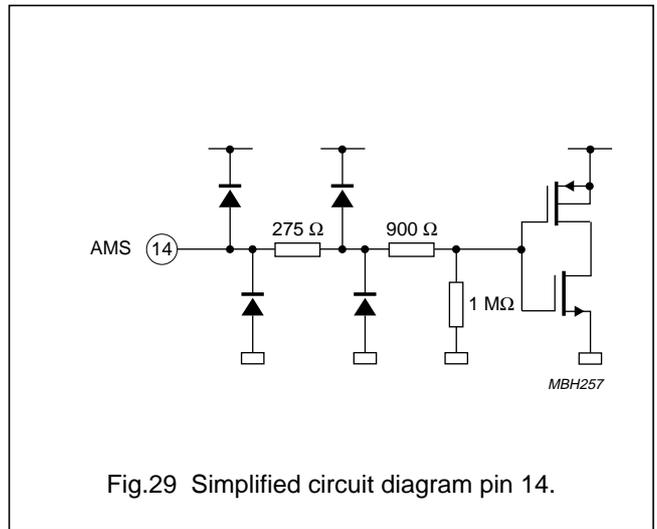
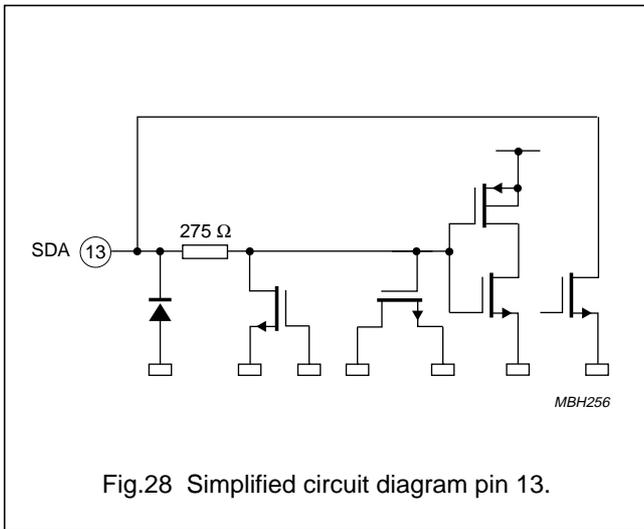
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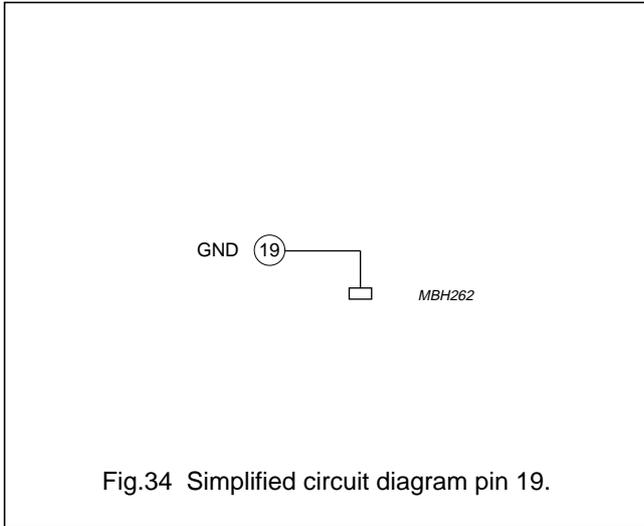


Fig.34 Simplified circuit diagram pin 19.

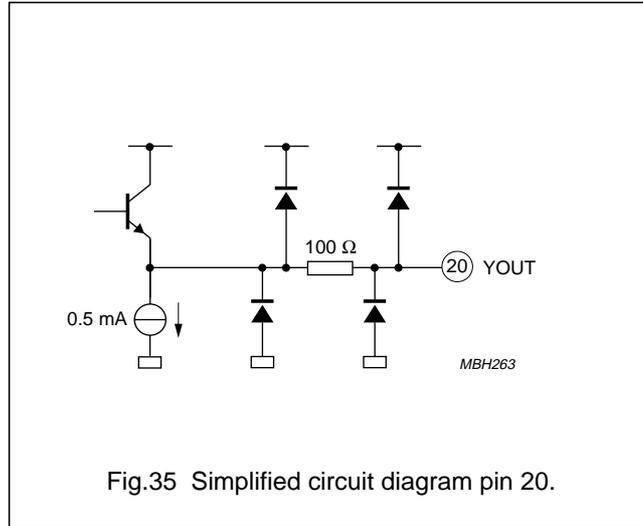


Fig.35 Simplified circuit diagram pin 20.

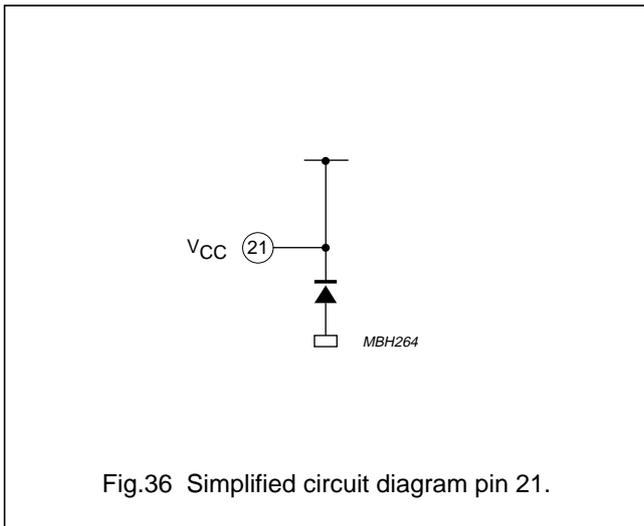


Fig.36 Simplified circuit diagram pin 21.

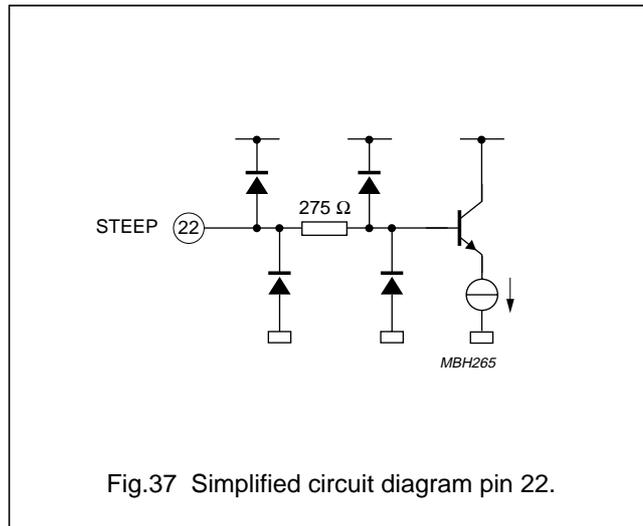


Fig.37 Simplified circuit diagram pin 22.

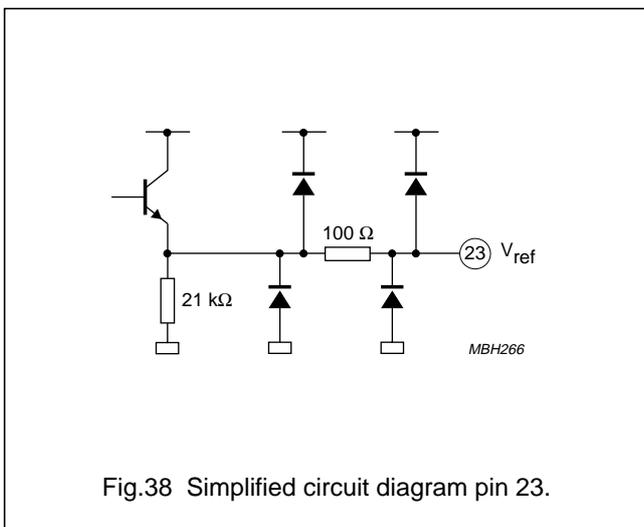


Fig.38 Simplified circuit diagram pin 23.

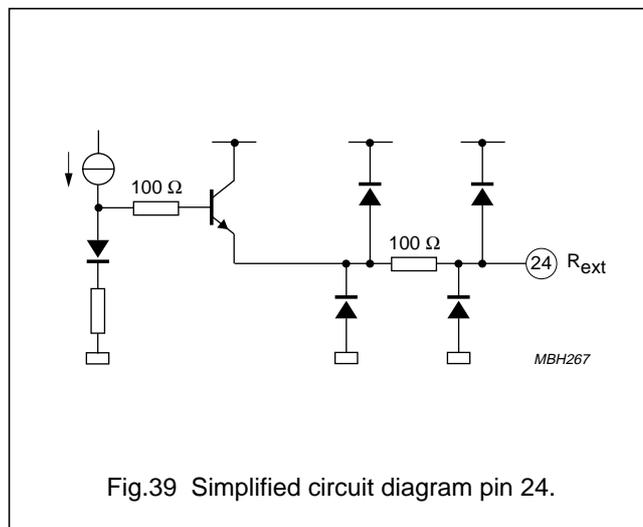


Fig.39 Simplified circuit diagram pin 24.

# YUV transient improvement processor

# TDA9177

### APPLICATION INFORMATION

To benefit optimally from its picture-sharpening capabilities, the TDA9177 should be positioned as the last part of the YUV-chain.

Feature reduction as a function of the noise contents of the picture can easily be realized in hardware by using a Noise Detector. Smart Noise Control (SNC) can be tailor-made for each application, by means of controlling the peaking and the steepness values by software (I<sup>2</sup>C-bus control).

Whenever I<sup>2</sup>C-bus control is not feasible, the embedded smart sharpness algorithm can be executed by driving pin SNC with the output of a noise detector. In this concept, additional post-processing of the noise detector output can easily be realized with external components.

Figure 40 shows an application example in which the TDA9177 is bus controlled, with the I<sup>2</sup>C-bus address at 40H. Furthermore, the Smart Noise Control pin (SNC; pin 15) is not used in the example shown.

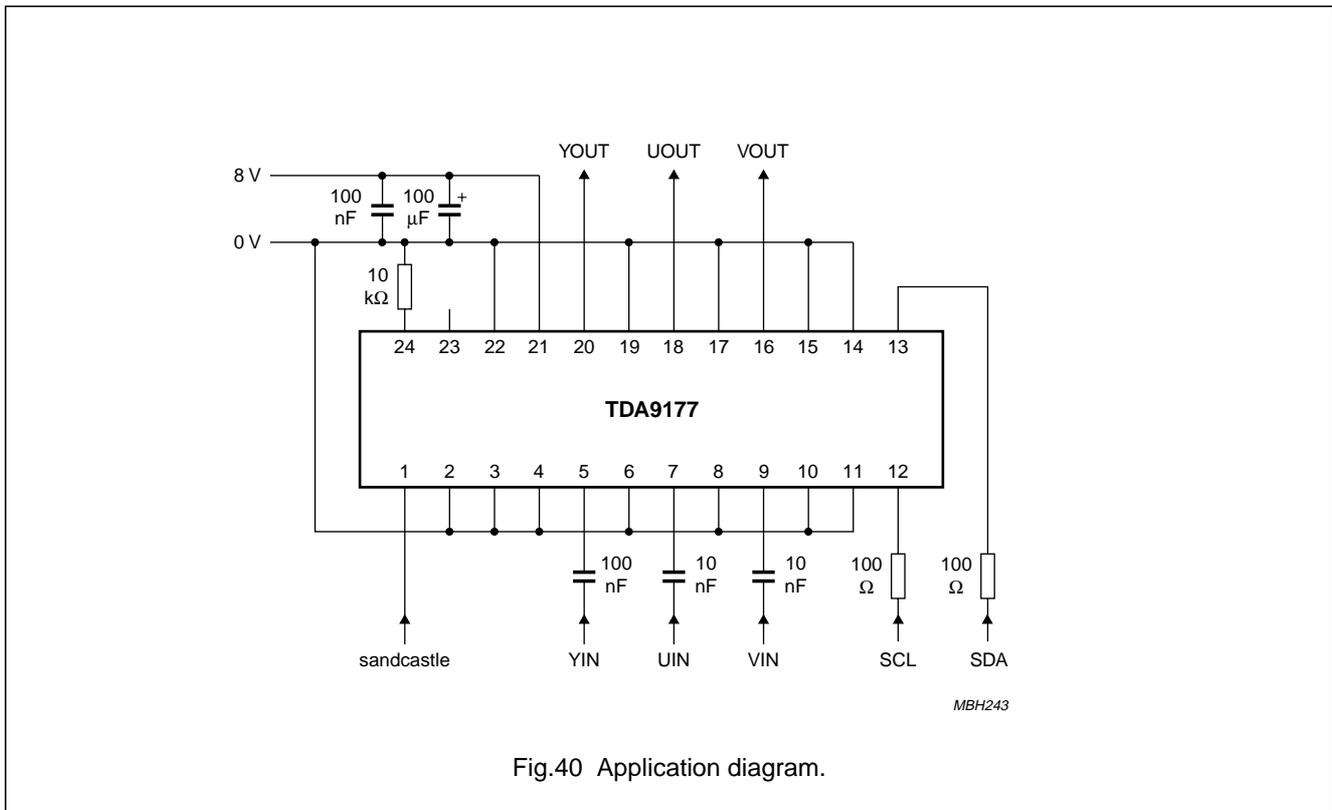


Fig.40 Application diagram.

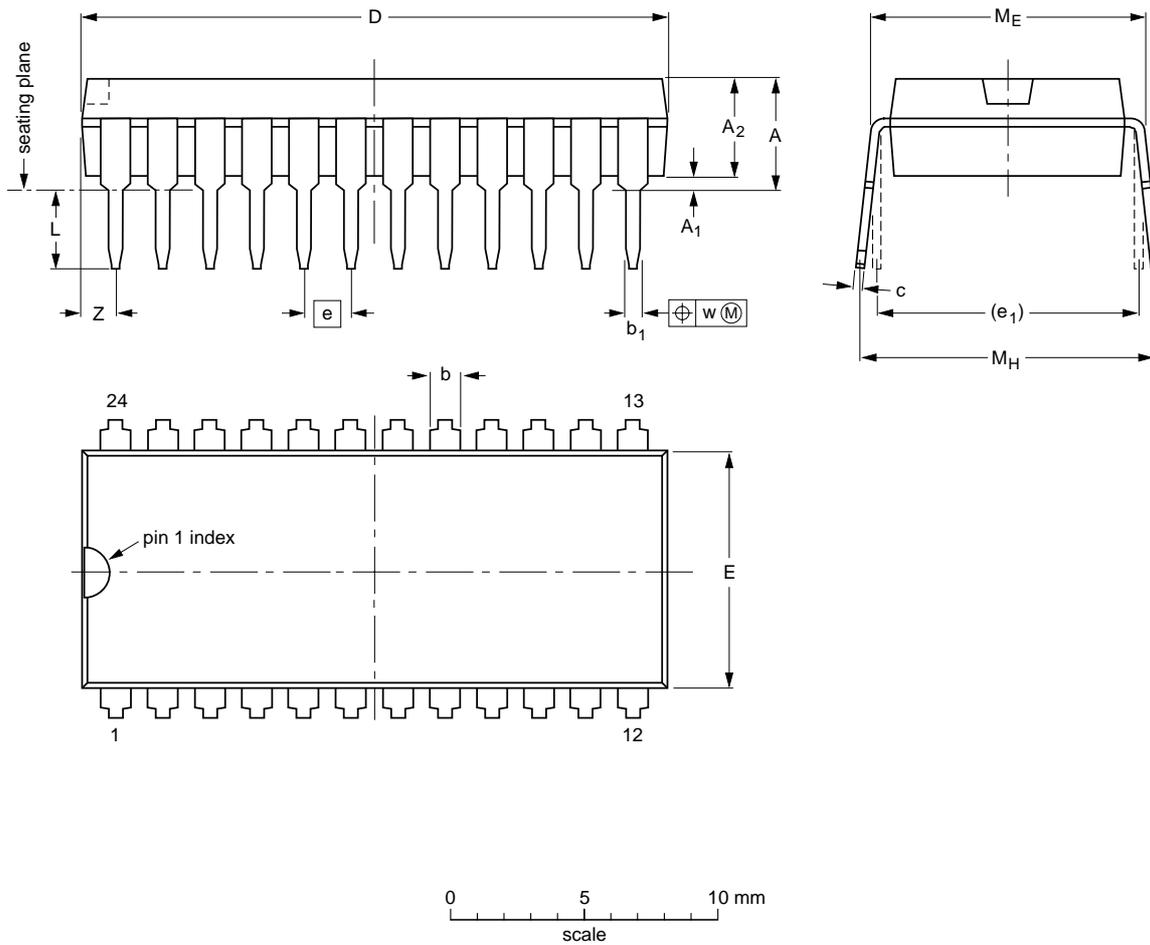
YUV transient improvement processor

TDA9177

PACKAGE OUTLINE

SDIP24: plastic shrink dual in-line package; 24 leads (400 mil)

SOT234-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.7	0.51	3.8	1.3 0.8	0.53 0.40	0.32 0.23	22.3 21.4	9.1 8.7	1.778	10.16	3.2 2.8	10.7 10.2	12.2 10.5	0.18	1.6

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT234-1						92-11-17 95-02-04

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## YUV transient improvement processor

## TDA9177

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### SOLDERING

#### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "*IC Package Databook*" (order code 9398 652 90011).

#### Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg\ max}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

#### Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

## YUV transient improvement processor

TDA9177

**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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