SGS-THOMSON MICROELECTRONICS

TDA9105

DEFLECTION PROCESSOR FOR MULTISYNC MONITORS

PRELIMINARY DATA

HORIZONTAL

- DUAL PLL CONCEPT
- 150kHz MAXIMUM FREQUENCY
- SELF-ADAPTATIVE
- X-RAY PROTECTION INPUT
- DC ADJUSTABLE DUTY-CYCLE
- 1st PLL LOCK /UNLOCK INFORMATION
- WIDE RANGE DC CONTROLLED H-POSITION
- ON/OFF SWITCH (FOR PWR MANAGEMENT)
- TWO H-DRIVE POLARITIES
- MOIRE OUTPUT

VERTICAL

- VERTICAL RAMP GENERATOR
- 50 TO 165Hz AGC LOOP
- DC CONTROLLED V-AMP, V-POS, S-AMP & C-COR
- ON/OFF SWITCH

EWPCC

- VERTICAL PARABOLA GENERATOR WITH DC CONTROLLED KEYSTONE & AMPLITUDE
- AUTO TRACKING WITH V-POS & V-AMP

GEOMETRY

- WAVE FORM GENERATOR FOR PARALELLOGRAM & SIDE PIN BALANCE CONTROL
- AUTO TRACKING WITH V-POS & V-AMP

DYNAMIC FOCUS

- VERTICAL PARABOLA OUTPUT FOR VERTICAL DYNAMIC FOCUS
- AUTO TRACKING WITH V-POS & V-AMP

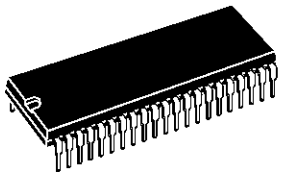
GENERAL

- ACCEPT POSITIVE OR NEGATIVE HORIZONTAL & VERTICAL SYNC POLARITIES
- SEPARATE H & V TTL INPUT
- COMPOSITE BLANKING OUTPUT

DESCRIPTION

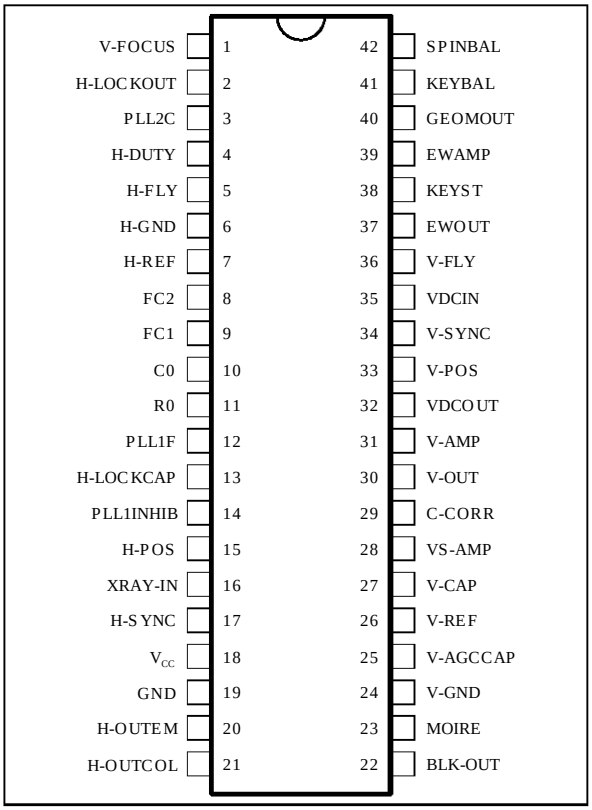
The TDA9105 is a monolithic integrated circuit assembled in a 42 pins shrink dual in line plastic package.

This IC controls all the functions related to the horizontal and vertical deflection in multimodes or multisync monitors.
This IC, combined with TDA9205 (RGB preamp), STV942x (OSD processor), ST727x (micro controller) and TDA817x (vertical booster), allows to realize very simple and high quality multimodes or multisync monitors.



SHRINK42
(Plastic Package)
ORDER CODE : TDA9105

PIN CONNECTIONS



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PIN DESCRIPTION

Pin	Name	Function
1	V-FOCUS	Vertical Dynamic Focus Output
2	H-LOCKOUT	First PLL Lock/Unlock Output
3	PLL2C	Second PLL Loop Filter
4	H-DUTY	DC Control of Horizontal Drive Output Pulse Duty-cycle. If this Pin is grounded, the Horizontal and Vertical Outputs are inhibited. By connecting a Capacitor on this Pin a Soft-start function may be realized on H-drive Output.
5	H-FLY	Horizontal Flyback Input (positive polarity)
6	H-GND	Horizontal Section Ground
7	H-REF	Horizontal Section Reference Voltage, must be filtered
8	FC2	VCO Low Threshold Filtering Capacitor
9	FC1	VCO High Threshold Filtering Capacitor
10	C0	Horizontal Oscillator Capacitor
11	R0	Horizontal Oscillator Resistor
12	PLL1F	First PLL Loop Filter
13	H-LOCKCAP	First PLL Lock/Unlock Time Constant Capacitor. When Frequency is changing, a Blanking Pulse is generated on Pin 23, the duration of this Pulse is proportionnel to the Capacitor on Pin 13.
14	PLL1INHIB	TTL-Compatible Input for PLL1 Output Current Inhibition
15	H-POS	DC Control for Horizontal Centering
16	XRAY-IN	X-RAY protection Input (with internal latch function)
17	H-SYNC	TTL compatible Horizontal Sync Input
18	V_{CC}	Supply Voltage (12V Typ.)
19	GND	Ground
20	H-OUTEM	Horizontal Drive Output (emiter of internal transistor)
21	H-OUTCOL	Horizontal Drive Output (open collector of internal transistor)
22	BLK OUT	Blanking Output, activated during frequency changes, when X-RAY Input is triggered, when VS is too low, or when Device is in stand-by mode (through H-DUTY Pin 2) and during H-FLY, V-FLY, V-SYNC, VSawth retrace.
23	MOIRE	Moire Output
24	V-GND	Vertical Section Signal Ground
25	V-AGCCAP	Memory Capacitor for Automatic Gain Control Loop in Vertical Ramp Generator
26	V-REF	Vertical Section Reference Voltage
27	V-CAP	Vertical Sawtooth Generator Capacitor
28	VS-AMP	DC Control of Vertical S-Shape Amplitude
29	C-CORR	DC Control of Vertical C-Correction
30	V-OUT	Vertical Ramp Output (with frequency independant amplitude and S-Correction)
31	V-AMP	DC Control of Vertical Amplitude Adjustment
32	VDCOUT	Vertical Position Reference Voltage Output
33	V-POS	DC Control of Vertical Position Adjustment
34	V-SYNC	TTL-Compatible Vertical Sync Input
35	VDCIN	Geometric Correction Reference Voltage Input
36	V-FLY	Vertical Flyback Input (positive polarity)
37	EWOUT	East /West Pincushion Correction Parabola Output
38	KEYST	DC Control of Keystone Correction
39	EWAMP	DC Control East/West Pincushion Correction Amplitude
40	GEOMOUT	Side Pin Balance & Parallelogram Correction Parabola Output
41	KEYBAL	DC Control of Parallelogram Correction
42	SPINBAL	DC Control of Side Pin Correction Amplitude

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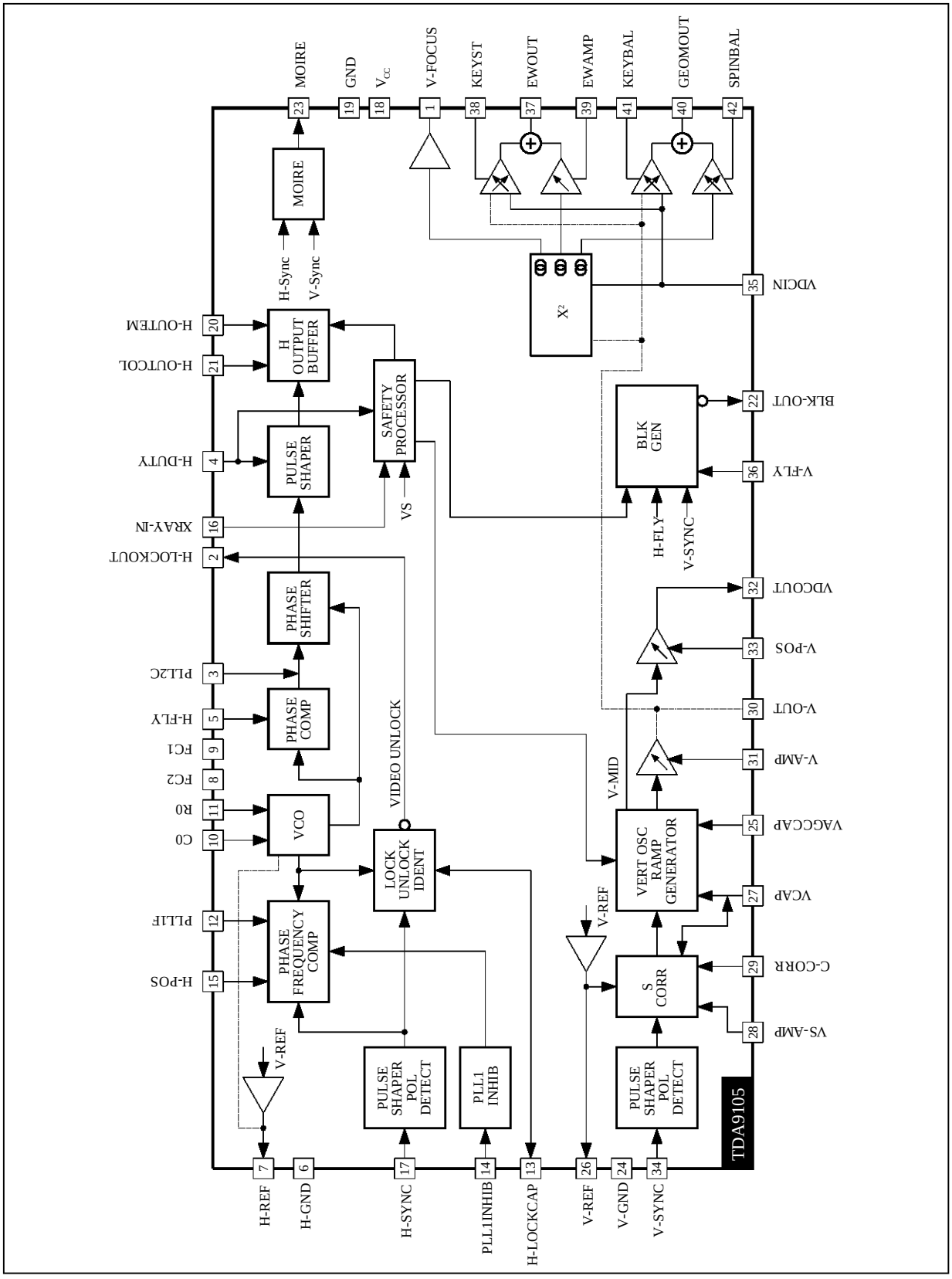
BLOCK DIAGRAM



QUICK REFERENCE DATA

Parameter	Value	Unit
Horizontal Frequency	15 to 150	kHz
Autosynch Frequency (for Given R0, C0)	1 to 3.7	FH
± Hor Sync Polarity Input	YES	
Compatibility with Composite Sync on H-SYNC Input	YES (see note 1)	
Lock/Unlock Identification on 1st PLL	YES	
DC Control for H-Position	YES	
X-RAY Protection	YES	
Hor DUTY Adjust	YES	
Stand-by Function	YES	
Two Polarities H-Drive Outputs	YES	
Supply Voltage Monitoring	YES	
PLL1 Inhibition Input	YES	
Composite Blanking Output	YES	
Horizontal Moire Output	YES	
Vertical Frequency	35 to 200	Hz
Vertical Autosync (for 150nF)	50 to 165	Hz
Vertical S-Correction	YES	
Vertical C-Correction	YES	
Vertical Amplitude Adjustment	YES	
Vertical Position Adjustment	YES	
East/West Parabola Output	YES	
PCC (Pin Cushion Correction) Amplitude Adjustment	YES	
Keystone Adjustment	YES	
Dynamic Horizontal Phase Control Output	YES	
Side Pin Balance Amplitude Adjustment	YES	
Parallelogram Adjustment	YES	
Tracking of Geometric Corrections with V-AMP and V-POS	YES	
Reference Voltage	YES (see note 2)	
Mode Detection	NO	
Vertical Dynamic Focus	YES	

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Notes : 1. Provided PLL inhibition input is used, see application diagram on page 27.
2. One for Horizontal section and one for Vertical section.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (Pin 18)	13.5	V
V_{IN}	Max Voltage on Pins 4, 15, 28, 29, 31, 33, 38, 39, 41, 42 Pin 5 Pins 17, 34 Pin 16	8 1.8 6 12	V
VESD	ESD Succeptibility Human Body Model, 100pF Discharge through 1.5kΩ EIAJ Norm, 200pF Discharge through 0Ω	 2 300	 kV V
T_{stg}	Storage Temperature	-40, +150	°C
T_j	Max Operating Junction Temperature	150	°C
T_{oper}	Operating Temperature	0, +70	°C

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THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ (j-a)}$	Junction-Ambient Thermal Resistance Max.	65	°C/W

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HORIZONTAL SECTION

Operating Conditions

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VCO						
R0min	Oscillator Resistor Min Value (Pin 11)		6			kΩ
C0min	Oscillator Capacitor Min Value (Pin 10)		390			pF
Fmax	Maximum Oscillator Frequency				150	kHz
HsVR	Horizontal Sync Input Voltage (Pin 17)		0		5.5	V
INPUT SECTION						
MinD	Minimum Input Pulses Duration (Pin 17)		0.7			µS
Mduty	Maximum Input Signal Duty Cycle (Pin 17)				25	%
OUTPUT SECTION						
I5m	Maximum Input Peak Current (Pin 5)				5	mA
 HOI1 HOI2	Horizontal Drive Output Max Current Pin 20 Pin 21	 Sourced current Sink current			 20 20	 mA mA
DC CONTROL VOLTAGES						
DCadj	DC Voltage on DC Controls (Pins 4-15)	V_{REF-H} = 8V	2		6	V

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HORIZONTAL SECTION (continued)

Electrical Characteristics (V_{CC} = 12V, T_{amb} = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY AND REFERENCE VOLTAGES						
V_{CC}	Supply Voltage (Pin 18)		10.8	12	13.2	V
I_{CC}	Supply Current (Pin 18)	See Figure 1		40	60	mA
V_{REF-H}	Reference Voltage for Horizontal Section (Pin 7)	I = 2mA	7.4	8	8.6	V
I_{REF-H}	Max Sourced Current on V_{REF-H} (Pin 7)				5	mA
V_{REF-V}	Reference Voltage for Vertical Section (Pin 26)	I = 2mA	7.4	8	8.6	V
I_{REF-V}	Max Sourced Current on V_{REF-V} (Pin 26)				5	mA
INPUT SECTION/PLL1						
V_{INTH}	Horizontal Input Threshold Voltage (Pin 17)	Low level voltage High level voltage	 2		0.8	V
V_{VCO}	VCO Control Voltage (Pin 12)	V_{REF-H} = 8V		1.6 to 6.2		V
V_{COG}	VCO Gain, dF/dV (Pin 12)	R0 = 6.49kΩ, C0 = 680pF		17		kHz/V
Hph	Horizontal Phase Adjust (Pin 15)	% of Horizontal period		±12.5		%
f0	Free Running Frequency (adjustable by changing R0)	R0 = 6.49kΩ, C0 = 680pF	25	27	29	kHz
CR	PLL1 Capture Range Fh Min Fh Max	R0 = 6.49kΩ, C0 = 680pF See conditions on Fig. 1		 f0 3.7 x f0		 kHz kHz
PLLinh	PLL 1 Inhibition (Pin 14) PLL ON (Typ. Threshold = 1.6V) PLL OFF	V_{14} V_{14}	 2		0.8	V V
I_{HLock0}	Max Output Current on HLock Output	I_2			10	mA
V_{HLock0}	Low Level Voltage on HLock Output	V_2 with I_2 = 10mA		0.25	0.5	V
SECOND PLL AND HORIZONTAL OUTPUT SECTION						
FBth	Flyback Input Threshold Voltage (Pin 5)	See Figure 14	0.65	0.75		V
Hjit	Horizontal Jitter	See Application Diagram (Pins 8-9)		80		ppm
 HDmin HDmax	Horizontal Drive Output Duty-cycle (Pin 20 or 21) (see Note) Minimum Maximum	 V_4 = 2V V_4 = 6V V_4 = V_{REF} - 100mV	 32 53.5 57.5	 34 56 60	 36 58.5 62.5	 % % %
HDvd	Horizontal Drive Low Level Output Voltage	Pin 20 to GND, V_{21}-V_{20}, I_{OUT} = 20mA		1.1	1.7	V
HDem	Horizontal Drive High Level Output Voltage (output on Pin 20)	Pin 21 to V_{CC}, I_{OUT} = 20mA	9.5	10		V
XRAYth	X-RAY Protection Input Threshold Voltage (Pin 16)		TBD	8	TBD	V
ISblkO	Maximum Output Current on Composite Blanking Output	I_{22}			10	mA
VSblkO	Low-Level Voltage on Composite Blanking Output (Blanking ON)	V_{22} with I_{22} = 10mA		0.25	0.5	V
ISmoiO	Maximum Output Current on Moire Output	I_{23}			10	mA
VSmoiO	Low-Level Voltage on Moire Output	V_{23} with I_{23} = 10mA		0.25	0.5	V
Vphi2	Internal Clamping Voltage on 2nd PLL Loop Filter Output (Pin 3)	Vmin Vmax		1.6 3.2		V V
V_{OFF}	Threshold Voltage to Stop H-out, V-out and to Activate BLKout (OFF Mode when $V_4 < V_{OFF}$) (Pin 4)	V_4			1	V
VSCinh	Supply Voltage to Stop H-out, V-out when V_{CC} < VSCinh (Pin 18)		TBD	7.5		V

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Note : If H-drive is taken on Pin 20 (Pin 21 connected to supply), H-D is the ratio of low level duration to horizontal period.
If H-drive is taken on Pin 21 (Pin 20 grounded), H-D is the ratio of high level duration to horizontal period.
In both cases, H-D period driving horizontal scanning transistor off.

VERTICAL SECTION
Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VSVR	Vertical Sync Input Voltage (Pin 34)	0		5.5	V
VEWM	Maximum EW Output Voltage (Pin 37)			6.5	V
VDHPCM	Maximum Dynamic Horizontal Phase Control Output Voltage (Pin 40)			6.5	V
VDHPCm	Minimum Dynamic Horizontal Phase Control Output Voltage (Pin 40)	0.9			V
VDFm	Minimum Vertical Dynamic Focus Output Voltage (Pin 1)	0.9			V
Rload	Minimum Load for less than 1% Vertical Amplitude Drift (Pin 25)	65			MΩ

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Electrical Characteristics (V_{CC} = 12V, T_{amb} = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{BIASP}	Bias Current (current sourced by PNP Base) (Pins 28-29)	For V_{28-29} = 2V		2		µA
I_{BIASN}	Bias Current (Pin 31) (sinked by NPN base)	For V_{31} = 6V		0.5		µA
VSth	Vertical Sync Input Threshold Voltage (Pin 34)	High-level Low-level	2		 0.8	V V
VSBI	Vertical Sync Input Bias Current (Current Sourced by PNP Base)	V_{34} = 0.8V		1		µA
V_{RB}	Voltage at Ramp Bottom Point (Pin 27)			2/8		V_{REF-V}
V_{RT}	Voltage at Ramp Top Point (with Sync) (Pin 27)			5/8		V_{REF-V}
V_{RTF}	Voltage at Ramp Top Point (without Sync) (Pin 27)			V_{RT}-0.1		V
VSW	Minimum Vertical Sync Pulse Width (Pin 34)		5			µS
VSmDut	Vertical Sync Input Maximum Duty-cycle (Pin 34)				15	%
VSTD	Vertical Sawtooth Discharge Time Duration (Pin 27)	With 150nF cap		70		µS
VFRF	Vertical Free Running Frequency	V_{28} = 2V, V_{29} grounded, Measured on Pin 27 Cosc (Pin27) = 150nF		100		Hz
ASFR	AUTO-SYNC Frequency (see Note 1)	With C_{27} = 150nF	50		165	Hz
RAFD	Ramp Amplitude Drift Versus Frequency	V_{31} = 6V, C_{27} = 150nF 50Hz < f < 165Hz		100		ppm/Hz
Rlin	Ramp Linearity on Pin 30	V_{28}, V_{29} grounded		0.5		%
Vpos	Vertical Position Adjustment Voltage (Pin 32)	V_{33} = 2V V_{33} = 4V V_{33} = 6V	 3.65	3.2 3.5 3.8	3.3	V V V
I_{VPOS}	Max Current on Vertical Position Control Output (Pin 32)			±2		mA
V_{OR}	Vertical Output Voltage (Pin 30) (peak-to-peak voltage on Pin 30)	V_{31} = 2V V_{31} = 4V V_{31} = 6V	 3.75	2 3 4	2.2	V V V
V_{OUTDC}	DC Voltage on Vertical Output (Pin30)	See Note 2		7/16		V_{REF-V}
V0I	Vertical Output Maximum Current (Pin 30)			±5		mA
dVS	Max Vertical S-Correction Amplitude V_{28} = 2V inhibits S-CORR V_{28} = 6V gives maximum S-CORR	 $\Delta V/V_{30pp}$ at T/4 $\Delta V/V_{30pp}$ at 3T/4	 TBD	 -4 +4	 TBD	 % %
Ccorr	Max Vertical C-Correction Amplitude	V_{29} = 2V V_{29} = 4V V_{29} = 6V	 TBD	-5 0 +5	TBD	% % %
VFly Th	Vertical Flyback Threshold (Pin 36)			1	TBD	V
VFly Inh	Inhibition of Vertical Flyback Input (Pin 36)	See Note 1		V_{REF}- 0.5		V
$I_{BIAS\ DCIN}$	Bias Current (Pin 35) (sourced by PNP base)	For V_{35} = V_{32}		2		µA

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Notes : 1. It is the frequency range for which the VERTICAL OSCILLATOR will automatically synchronize, using a single capacitor value on Pin 27 and with a constant ramp amplitude.
2. Typically 3.5V for Vertical reference voltage typical value (8V).

VERTICAL SECTION (continued)

East/West Function

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
EW_{DC}	DC Output Voltage (see Figure 2)	V_{33} = 4V , $V_{35} = V_{32}$, V_{38} = 4V		2.5		V
$TDEW_{DC}$	DC Output Voltage Thermal Drift	See Note 2		100		ppm/°C
EW_{para}	Parabola Amplitude	V_{28} = 2V, V_{29} grounded, V_{31} = 6V, V_{33} = 4V, $V_{35} = V_{32}$, V_{38} = 4V, V_{39} = 6V V_{39} = 2V	 TBD	 2.9 0	 	 V V
EW_{track}	Parabola Amplitude versus V-AMP Control (tracking between V-AMP and E/W)	V_{28} = 2V, V_{29} grounded V_{33} = 4V, $V_{35} = V_{32}$, V_{38} = 4V, V_{39} = 4V V_{31} = 2V V_{31} = 4V V_{31} = 6V	 	 0.36 0.82 1.45	 	 V V V
KeyAdj	Keystone Adjustment Capability : A/B Ratio (see Figure 2) B/A Ratio	V_{28} = 2V, V_{29} grounded, V_{31} = 6V, V_{33} = 4V, $V_{35} = V_{32}$, V_{39} = 4V V_{38} = 6V V_{38} = 2V	 TBD TBD	 0.48 0.48	 	
Keytrack	Keystone versus V-POS control (tracking between V-POS and EW) A/B Ratio B/A Ratio	V_{28} = 2V, V_{29} grounded, V_{31} = 6V, V_{38} = 4V, V_{39} = 6V V_{33} = 2V, $V_{35} = V_{32}$ V_{33} = 6V, $V_{35} = V_{32}$	 	 0.54 0.54	 	

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Notes : 1. When Pin 36 > V_{REF} - 0.5V, Vfly input is inhibited and vertical blanking on composite blanking output is replaced by vertical sawtooth discharge time.

2. These parameters are not tested on each unit. They are measured during our internal qualification procedure which includes characterization on batches comming from corners of our processes and also temperature characterization.

Dynamic Horizontal Phase Control Function

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$DHPC_{DC}$	DC Ouput Voltage (see Figure 3)	V_{33} = 4V, $V_{35} = V_{32}$, V_{41} = 4V		4		V
$TDDHPC_{DC}$	DC Output Voltage Thermal Drift	See Note		100		ppm/°C
SPBpara	Side Pin Balance Parabola Amplitude (see Figure 3)	V_{28} = 2V, V_{29} grounded, V_{31} = 6V, V_{33} = 4V, $V_{35} = V_{32}$, V_{41} = 4V V_{42} = 6V V_{42} = 2V	 TBD	 +1.45 - 1.45	 TBD	 V V
SPBtrack	Side Pin balance Parabola Amplitude versus V-amp Control (tracking between V-amp and SPB)	V_{28} = 2V, V_{29} grounded, V_{33} = 4V, $V_{35} = V_{32}$, V_{41} = 4V, V_{42} = 6V V_{31} = 2V V_{31} = 4V V_{31} = 6V	 	 0.36 0.82 1.45	 	 V V V
ParAdj	Parallelogram Adjustment Capability A/B ratio (see Figure.3) B/A ratio	V_{28} = 2V, V_{29} grounded, V_{31} = 6V, V_{33} = 4V, $V_{35} = V_{32}$, V_{42} = 6V V_{41} = 6V V_{41} = 2V	 TBD TBD	 0.12 0.12	 	
Partrack	Parallelogram versus V-pos Control (tracking between V-pos and DHPC) A/B ratio B/A ratio	V_{28} = 2V, V_{29} grounded, V_{31} = 6V, V_{41} = 4V, V_{42} = 6V V_{33} = 2V, $V_{35} = V_{32}$, V_{33} = 6V, $V_{35} = V_{32}$	 	 0.53 0.53	 	

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VERTICAL SECTION (continued)

Vertical Dynamic Focus Function

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDF_{DC}	DC Output Voltage (see Figure 4)	V_{33} = 4V, V_{35} = V_{32}		6		V
$TDVDF_{DC}$	DC Output Voltage Thermal Drift	See Note		100		ppm/C
VDFAMP	Parabola Amplitude versus V-amp (tracking between V-amp and VDF) (see Figure 4)	V_{28} = 2V, V_{29} grounded, V_{33} = 4V, V_{35} = V_{32},				
		V_{31} = 2V	-0.84	-0.72	-0.6	V
		V_{31} = 4V	-1.78	-1.57	-1.36	V
		V_{31} = 6V	-3.14	-2.85	-2.56	V
VDFKEY	Parabola Assymetry versus V-pos Control (tracking between V-pos and VDF)	V_{28} = 2V, V_{29} grounded, V_{31} = 6V,				
	A/B ratio	V_{33} = 2V, V_{35} = V_{32},	0.42	0.52	0.62	
	B/A ratio	V_{33} = 6V, V_{35} = V_{32}	0.48	0.58	0.68	

9105-11.TBL

Note : These parameters are not tested on each unit. They are measured during our internal qualification procedure which includes characterization on batches comming from corners of our processes and also temperature characterization.

Figure 1 : Testing Circuit

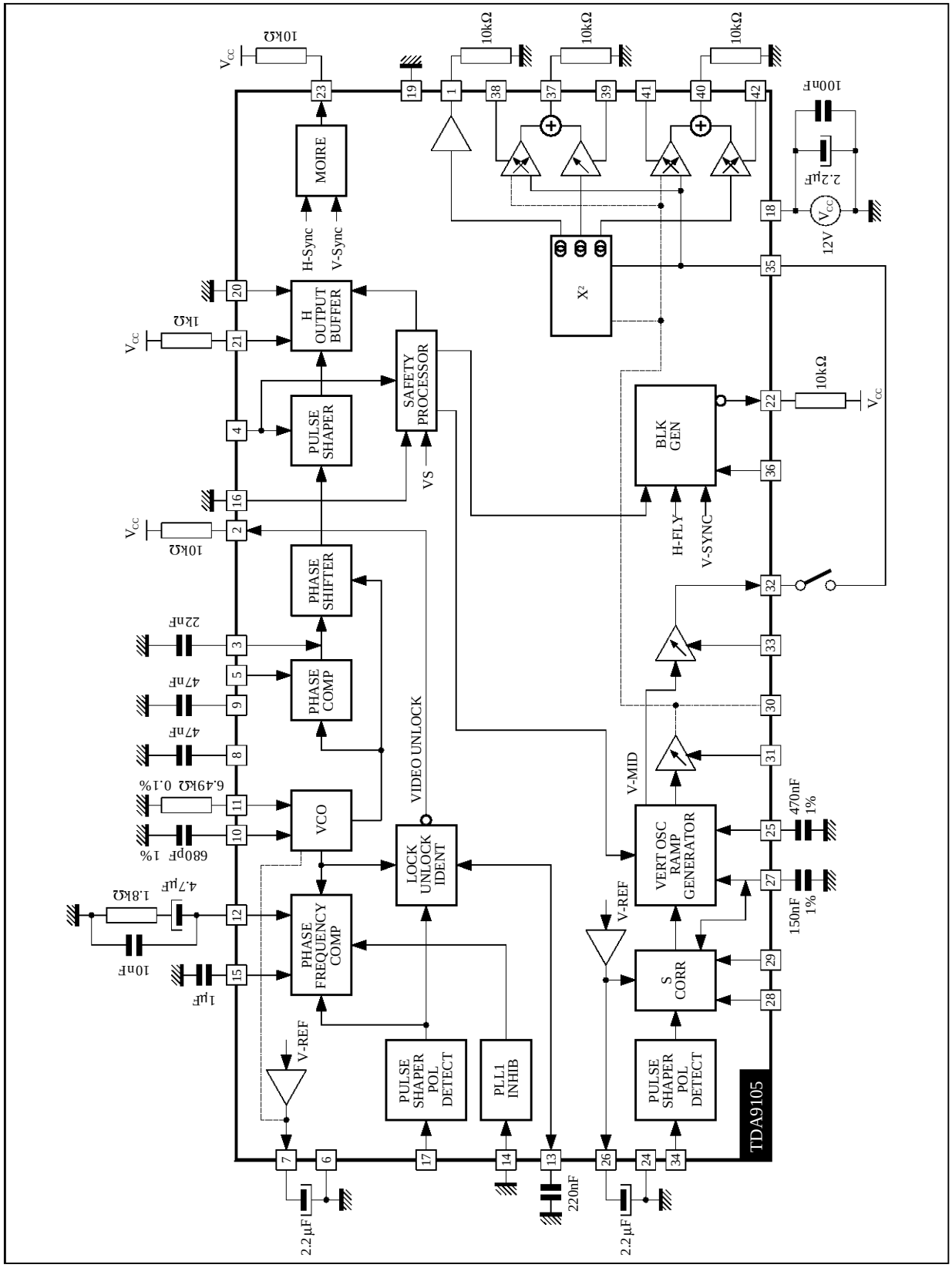


Figure 2 : E/W Output

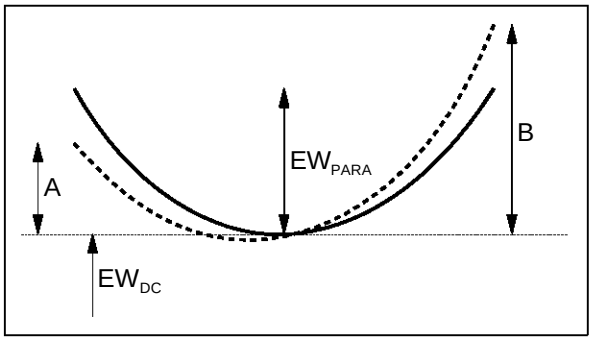


Figure 3 : Dynamic Horizontal Phase Control Output

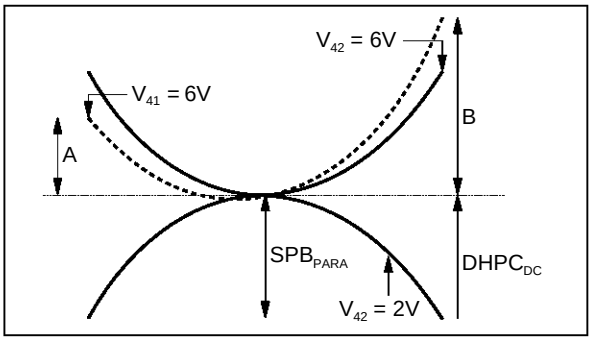
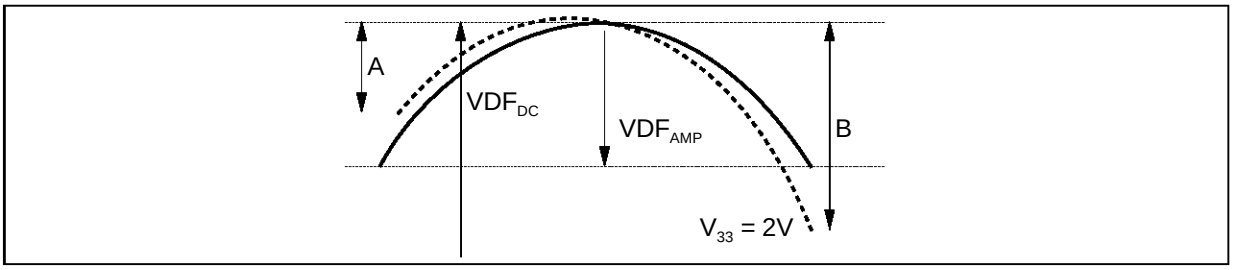
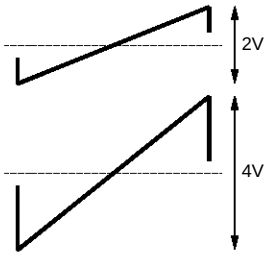
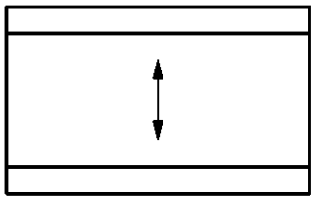
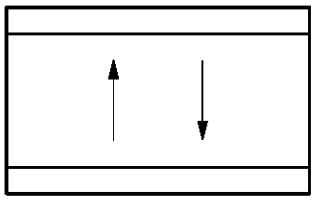
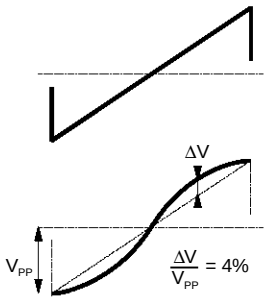
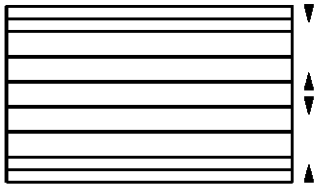
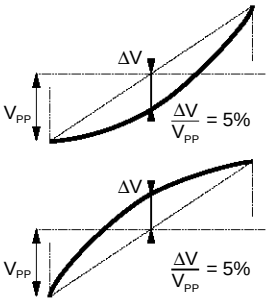
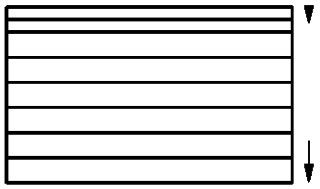


Figure 4 : Vertical Dynamic Focus Function

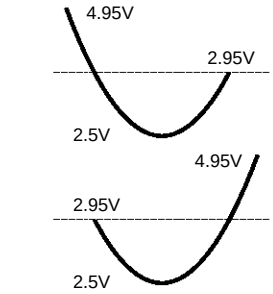
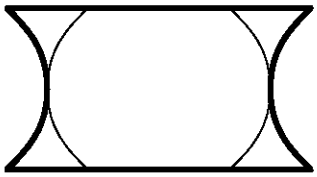
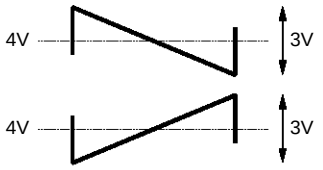
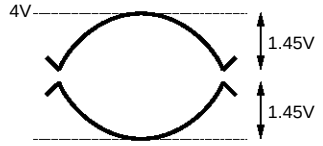
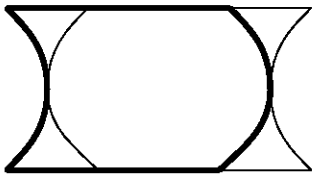


TYPICAL VERTICAL OUTPUT WAVEFORMS

Function	Control Pin	Output Pin	Control Voltage	Specification	Picture Image
Vertical Size	31	30	2V 6V		
Vertical Position DC Control	33	32	2V 4V 6V	3.2V 3.5V 3.8V	
Vertical DC In/Out	35	1 37 40		This terminal is a Pin controlling the center position of geometric correction signals. When connected to Pin 32, "Autotracking" occurs.	
Vertical S Linearity	25	30	2V 6V		
Vertical C Linearity	29	30	2V 6V		

9105-13.TBL / 9105-07.EPS TO 9105-13.EPS

TYPICAL GEOMETRY OUTPUT WAVEFORMS

Function	Control Pin	Output Pin	Control Voltage	Specification	Picture Image
Trapezoid Control	38	37	V_{39} = 4V 2V 6V		
Pin Cushion Control	39	37	V_{38} = 4V 2V 6V		
Parrallelogram Control	41	40	V_{42} = 4V 2V 6V		
Side Pin Balance Control	42	40	V_{41} = 4V 2V 6V		
Vertical Dynamic Focus		1			

9105-14.TBL / 9105-14.EPS TO 9105-22.EPS

Note : The specification of Output voltage is indicated on $4V_{PP}$ vertical sawtooth output condition.The output voltage depends on vertical sawtooth output voltage.

OPERATING DESCRIPTION

GENERAL CONSIDERATIONS

Power Supply

The typical value of the power supply voltage V_{CC} is 12V. Perfect operation is obtained if V_{CC} is maintained in the limits : 10.8V $\rightarrow$ 13.2V.

In order to avoid erratic operation of the circuit during the transient phase of V_{CC} switching on, or switching off, the value of V_{CC} is monitored and the outputs of the circuit are inhibited if V_{CC} < 7.6 typically.

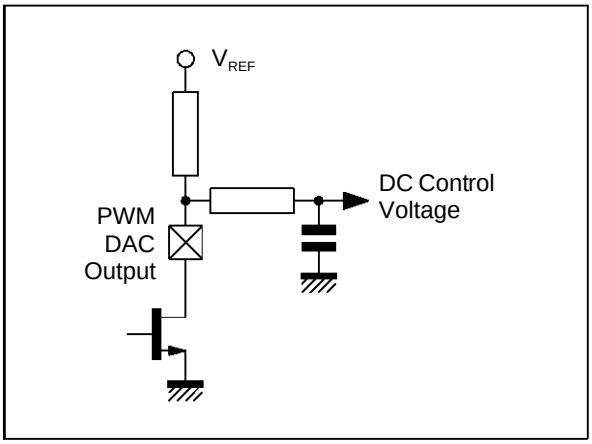
In order to have a very good power supply rejection, the circuit is internally powered by several internal voltage references (The unique typical value of which is 8V). Two of these voltage references are externally accessible, one for the vertical part and one for the horizontal part. These voltage references can be used for the DC control voltages applied on the concerned pins by the way of potentiometers or digital to analog converters (DAC's). Furthermore it is necessary to filter the a.m. voltage references by the use of external capacitor connected to ground, in order to minimize the noise and consequently the "jitter" on vertical and horizontal output signals.

DC Control Adjustments

The circuit has 10 adjustment capabilities : 2 for the horizontal part, 2 for the E/W correction, 4 for the vertical part, 2 for the Dynamic Horizontal phase control.

The corresponding inputs of the circuit has to be driven with a DC voltage typically comprised between 2 and 6V for a value of the internal voltage reference of 8V.

Figure 5 : Example of Practical DC Control Voltage Generation



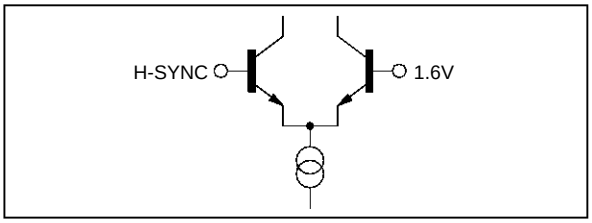
In order to have a good tracking with the voltage reference value, it's better to maintain the control voltages between $V_{REF}/4$ and $3/4 \cdot V_{REF}$.
The input current of the DC control inputs is typically very low (about a few µA). Depending on the internal structure of the inputs, it can be positive or negative (sink or source).

HORIZONTAL PART

Input section

The horizontal input is designed to be sensitive to TTL signals typically comprised between 0 and 5V. The typical threshold of this input is 1.6V. This input stage uses an NPN differential stage and the input current is very low.

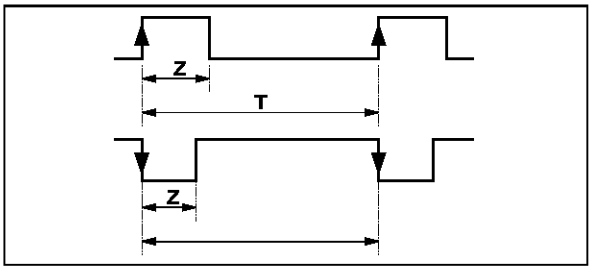
Figure 6 : Input Structure



Concerning the duty cycle of the input signal, the following signals may be applied to the circuit.

Using internal integration, both signals are recognized on condition that Z/T ≤ 25%. Synchronisation occurs on the leading edge of the internal sync signal. The minimum value of Z is 0.7µs.

Figure 7

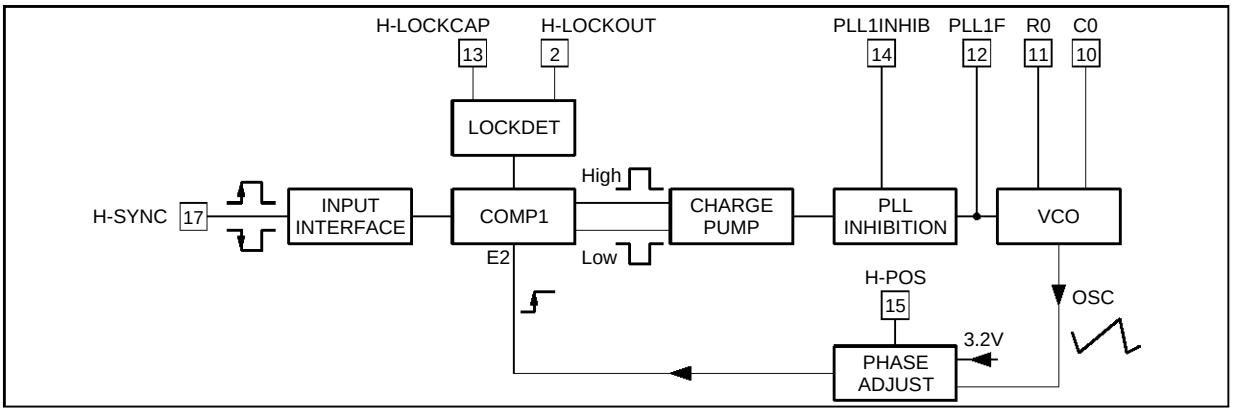


PLL1

The PLL1 is composed of a phase comparator, an external filter and a Voltage Controlled Oscillator (VCO).
The phase comparator is a "phase frequency" type, designed in CMOS technology. This kind of phase detector avoids locking on false frequencies. It is followed by a "charge pump", composed of 2 current sources sink and source (I = 1mA typ.)

OPERATING DESCRIPTION (continued)

Figure 8 : Principle Diagram



The dynamic behaviour of the PLL is fixed by an external filter which integrates the current of the charge pump. A "CRC" filter is generally used (see Figure 9).

PLL1 is inhibited by applying a high level on Pin 14 (PLLinhib) which is a TTL compatible input. The inhibition results from the opening of a switch located between the charge pump and the filter (see Figure 8).

The VCO uses an external RC network. It delivers a linear sawtooth obtained by charge and discharge of the capacitor, by a current proportionnal to the current in the resistor. typical thresholds of sawtooth are 1.6V and 6.4V (see Figure 10).

The control voltage of the VCO is typically comprised between 1.6V and 6V (see Figure 10). The theoretical frequency range of this VCO is in the ratio 1 → 3.75, but due to spread and thermal drift of external components and the circuit itself, the effective frequency range has to be smaller (e.g. 30kHz → 85kHz). In the absence of synchronisation signal the control voltage is equal to 1.6V typ. and the VCO oscillates on its lowest frequency (free frequency). The synchro frequency has to be always higher than the free frequency and a margin has to be taken. As an example for a synchro range from 30kHz to 85kHz, the suggested free frequency is 27kHz.

Figure 9

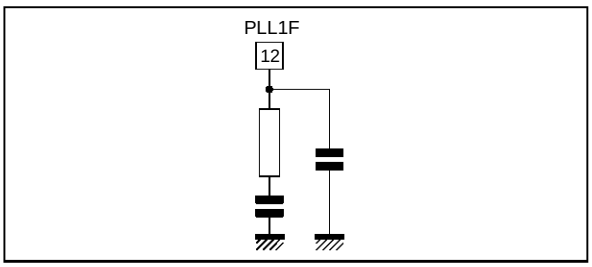
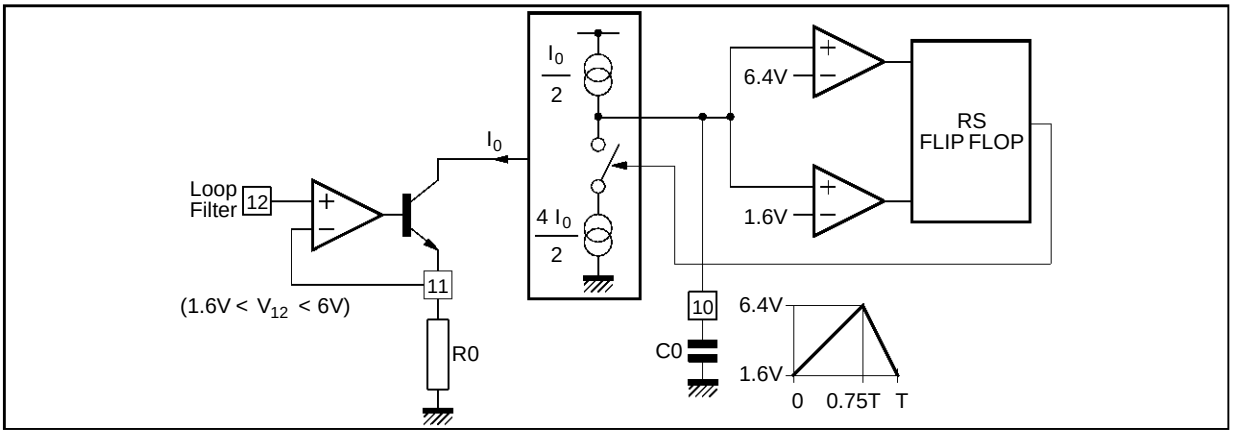


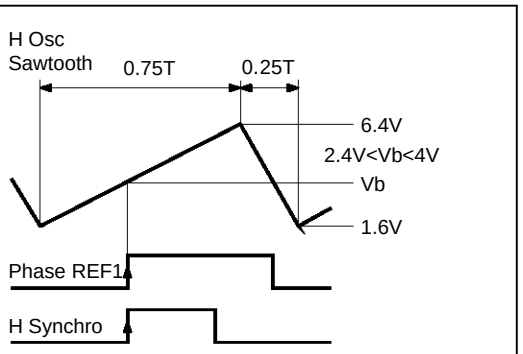
Figure 10 : Details of VCO



OPERATING DESCRIPTION (continued)

The PLL1 ensures the coincidence between the leading edge of the synchro signal and a phase reference obtained by comparison between the sawtooth of the VCO and an internal DC voltage adjustable between 2.4V and 4V (by Pin 15). So a ±45° phase adjustment is possible (see Figure 11).

Figure 11 : PLL1 Timing Diagram



Phase REF1 is obtained by comparison between the sawtooth and a DC voltage adjustable between 2.4V and 4V. The PLL1 ensures the exact coincidence between the signals phase REF and HSYNS. A ± T/8 phase adjustment is possible.

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The two VCO threshold can be filtered by connecting capacitor on Pins 8-9.

The TDA9103 also includes a LOCK/UNLOCK identification block which senses in real-time whether the PLL is locked on the incoming horizontal sync signal or not. The resulting information is available on HLOCKOUT output (Pin 2). The block diagram of the LOCK/UNLOCK function is described in Figure 12.

The NOR1 gate is receiving the phase comparator output pulses (which also drive the charge pump).

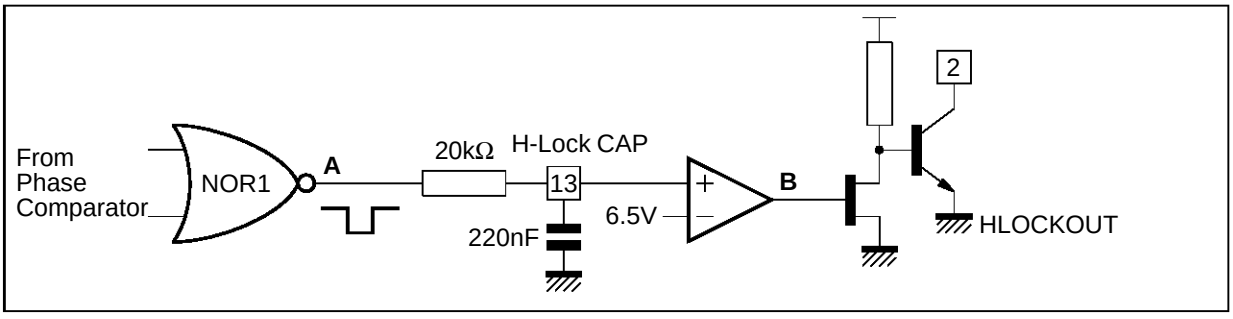
When the PLL is locked, on point **A** there is a very small negative pulse (100ns) at each horizontal cycle, so after R-C filter, there is a high level on Pin 13 which force HLOCKOUT to high level (provided that HLOCKOUT is pulled up to V_{CC}).

When the PLL is unlocked, the 100ns negative pulse on **A** becomes much larger and consequently the average level on Pin 13 will decrease. When it reaches 6.5V, point **B** goes to low level forcing HLOCKOUT output to "0".

The status of Pin 13 is approximately the following :
- Near 0V when there is no H-SYNC,
- Between 0 and 4V with H-SYNC frequency different from VCO,
- Between 4 and 8V when H-SYNC frequency = VCO frequency but not in phase,
- Near to 8V when PLL is locked.

It is important to notice that Pin 13 is not an output pin and must only be used for filtering purpose (see Figure 12).

Figure 12 : LOCK/UNLOCK Block Diagram

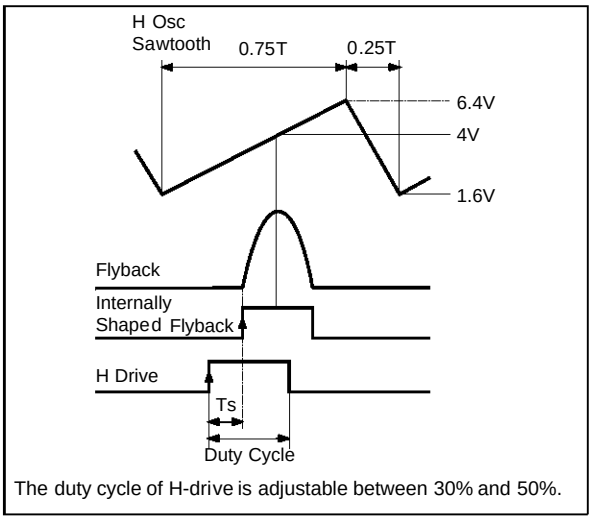


9105-30.EPS

OPERATING DESCRIPTION (continued)

PLL2

Figure 13 : PLL2 Timing Diagram



The PLL2 ensures a constant position of the shaped flyback signal in comparison with the sawtooth of the VCO (see Figure 13).

The phase comparator of PLL2 is followed by a charge pump with a ±0.5mA (typ.) output current.

The flyback input is composed of an NPN transistor. This input has to be current driven.

The maximum recommanded input current is 2mA (see Figures 14 and 15).

Figure 14 : Flyback Input Electrical Diagram

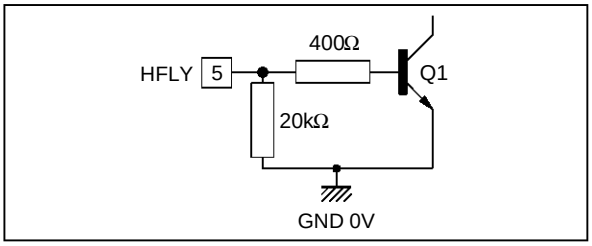
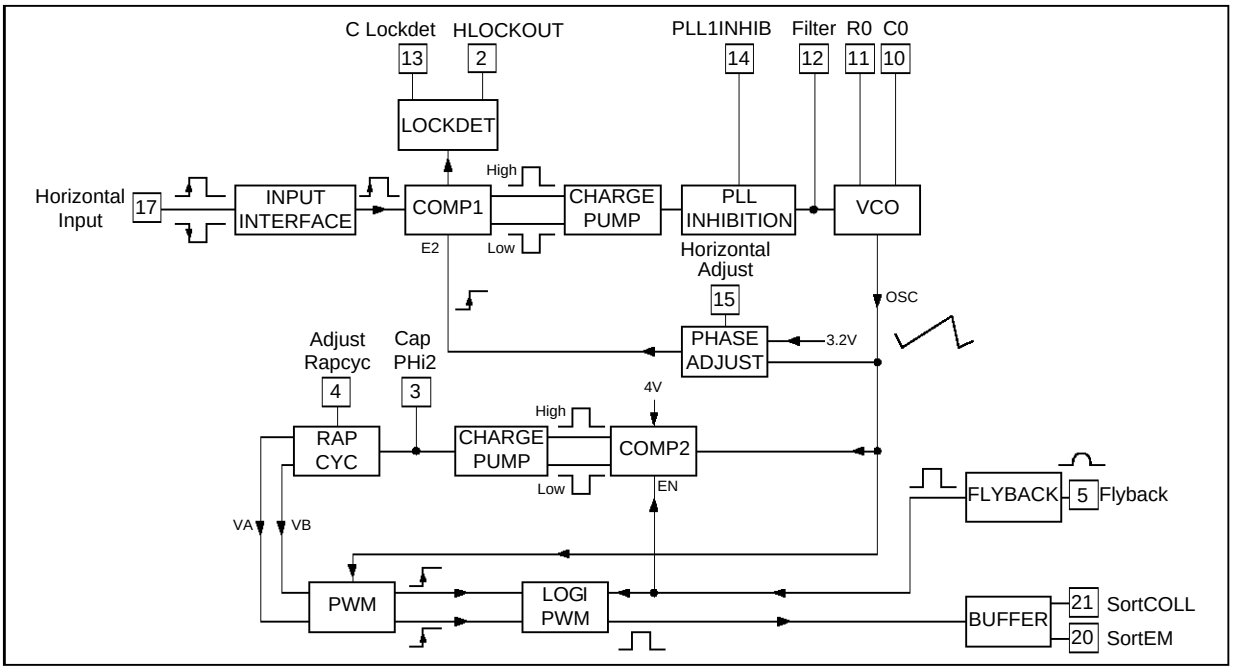


Figure 15 : Dual PLL Block Diagram



OPERATING DESCRIPTION (continued)

Output Section

The H-drive signal is transmitted to the output through a shaping block ensuring a duty cycle adjustable from 30% to 50%. In order to ensure a reliable operation of the scanning power part, the output is inhibited in the following circumstances :

- V_{CC} too low,
- Xray protection activated,
- During the horizontal flyback,
- Output voluntarily inhibited through Pin 4.

The output stage is composed of a Darlington NPN bipolar transistor. Both the collector and the emitter are accessible (see Figure 16).

The output Darlington is in off-state when the power scanning transistor is also in off-state.

The maximum output current is 20mA, and the corresponding voltage drop of the output darlington is 1.1V typically.

It is evident that the power scanning transistor cannot be directly driven by the integrated circuit. An interface has to be designed between the circuit and the power transistor which can be of bipolar or MOS type.

Outputs inhibition

The application of a voltage lower than 1V (typ.) on Pin 4 (duty cycle adjust) inhibits the horizontal and vertical outputs. This is not memorised.

X-RAY PROTECTION : the activation of the X-ray protection is obtained by application of a high level on the X-ray input (>8V). Consequences of X-ray protection are :

- Inhibition of H drive output,
- Activation of composite blanking output.

The reset of this protection is obtained by V_{CC} switch off (see Figure 17).

Figure 16 : Output stage simplified diagram, showing the two possibilities of connection

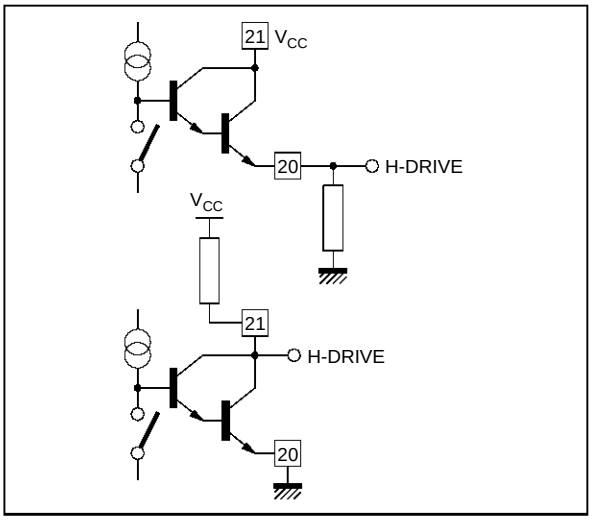
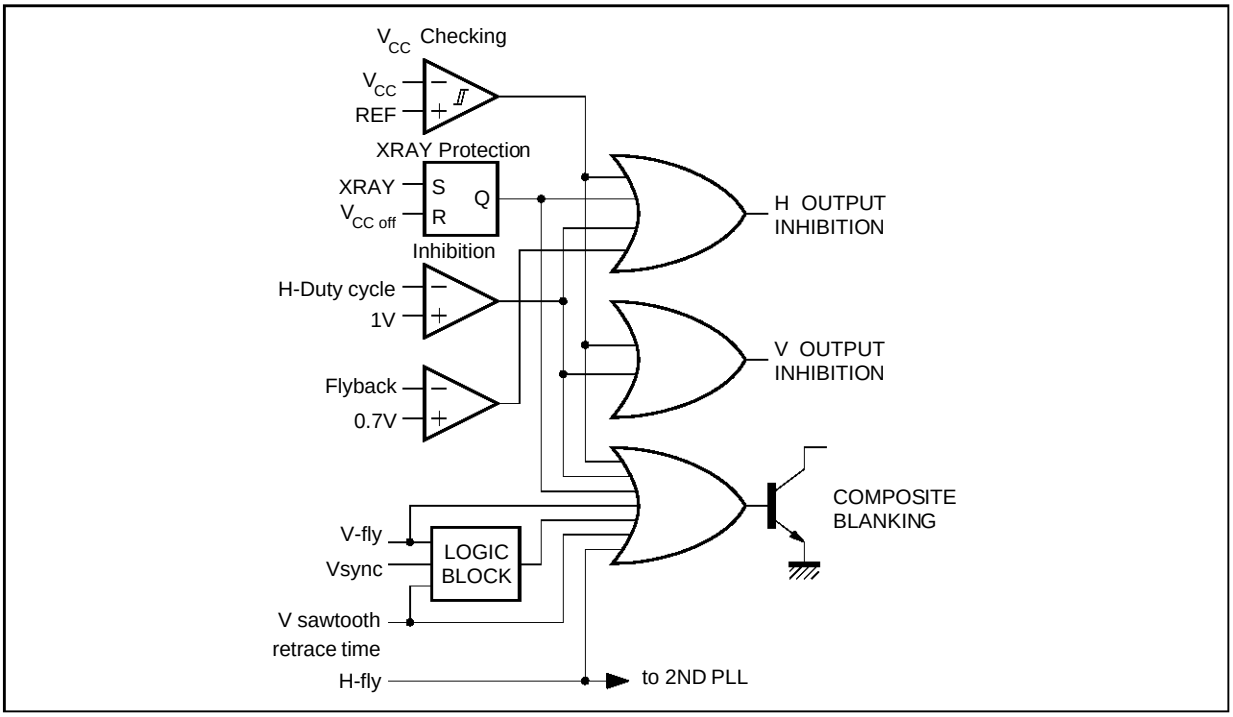


Figure 17 : Safety Functions Block Diagram



OPERATING DESCRIPTION (continued)

Moire Function

Figure 18 : Moire Function Block Diagram

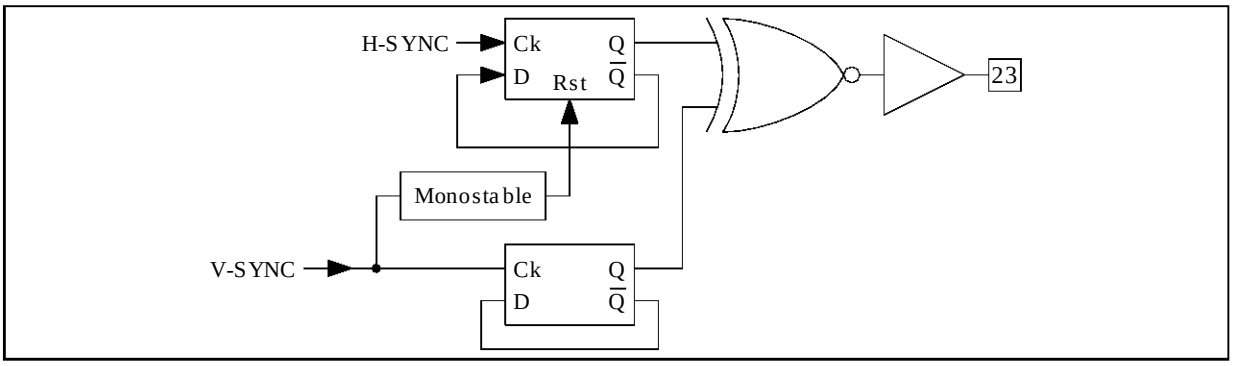
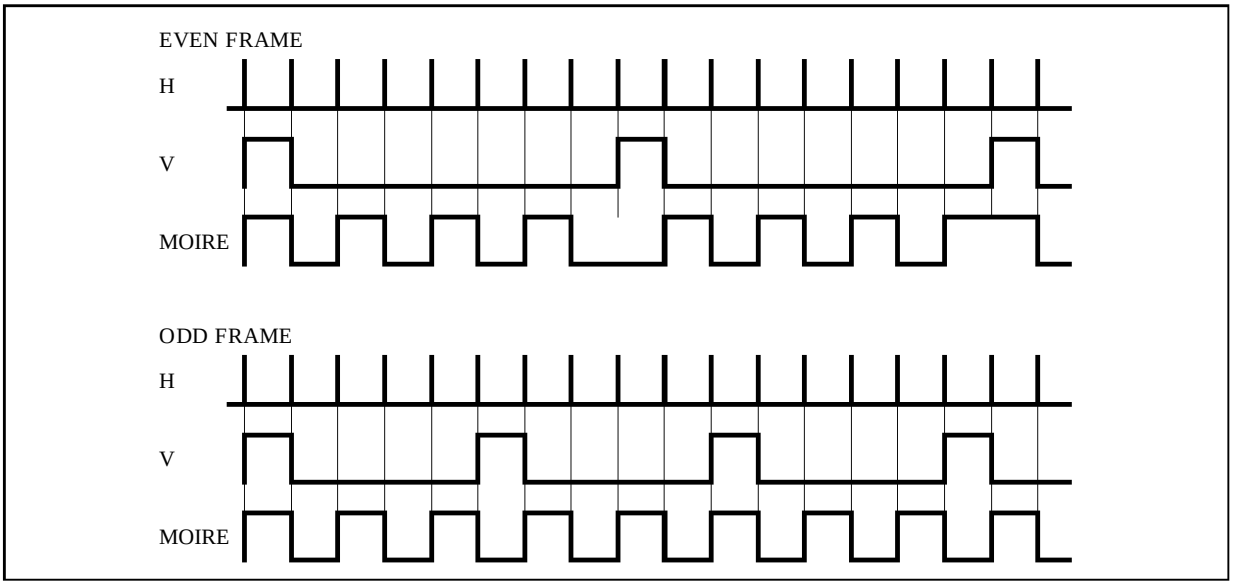


Figure 19 : Moire Output Waveform



Geometric Corrections

The principle is represented in Figure 20.

Starting from the vertical ramp, a parabola shaped is generated for E/W correction, dynamic horizontal phase control correction, and vertical dynamic Focus correction.

The core of the parabola generator is an analog multiplier. The output current of which is equal to :

$$\Delta I = k\,(V_{RAMP} - V_{DCIN})^2.$$

Where V_{RAMP} is the vertical ramp, typically comprised between 2 and 5V, V_{DCIN} is a vertical DC input adjustable in the range 3.2V $\rightarrow$ 3.8V in order to generate a dissymmetric parabola if required (keystone adjustment).

In order to keep good screen geometry for any end user preferences adjustment we implemented the possibility to have "**geometry tracking**". To enable the "tracking" function, the V_{DCOUT} must be connected to V_{DCIN}.

It is possible to inhibit V_{POS} tracking by applying a fixed DC voltage on the V_{DCIN} Pin.

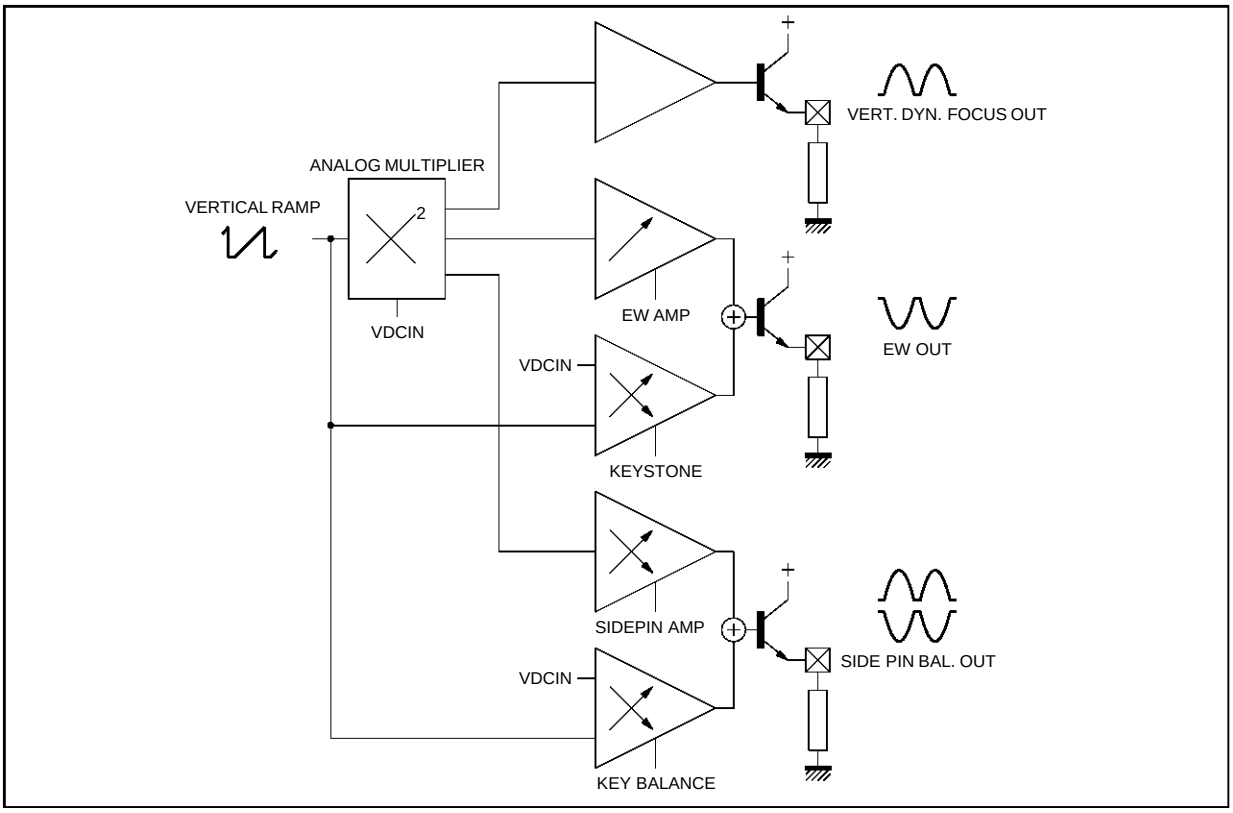
This DC voltage in that case must be taken from the vertical reference and adjusted to 3.5V with an external bridge resistor.

Due to large output stages voltage range (E/W, BALANCE, FOCUS), the combination of tracking function with maximum vertical amplitude max. or min. vertical position and maximum gain on the DC control inputs may leads to the output stages saturation. This must be avoided by limiting the output voltage by apropriate DC control voltages.

OPERATING DESCRIPTION (continued)

Geometric Corrections (continued)

Figure 20 : Geometric Corrections Principle



For E/W part and Dynamic Horizontal phase control part, a sawtooth shaped differential current in the following form is generated : $\Delta I' = k' (V_{RAMP} - V_{DCIN})$. Then ΔI and $\Delta I'$ are added together and converted into voltage.

These two parabola are respectively available on Pin 37 and Pin 40 by the way of an emitter follower which has to be biased by an external resistor (10kΩ). They can be DC coupled with external circuitry.

EW $V_{OUT} = 2.5V + K_1' (V_{RAMP} - V_{DCIN}) + K_1 (V_{RAMP} - V_{DCIN})^2$

K_1 is adjustable by EW amp control (Pin 39)
K_1' is adjustable by KEYST control (Pin 38)

Dyn. Hor. Phase Control $V_{OUT} = 4V + K_2' (V_{RAMP} - V_{DCIN}) + K_2 (V_{RAMP} - V_{DCIN})^2$

K_2 is adjustable by SPB amp control (Pin 42)
K_2' is adjustable by KEYBAL control (Pin 41)

For vertical dynamic focus part, only a constant amplitude parabola is generated in the form :

$$V_{OUT} = 6V - 0.75 \times (V_{AMP} - V_{DCIN})^2.$$

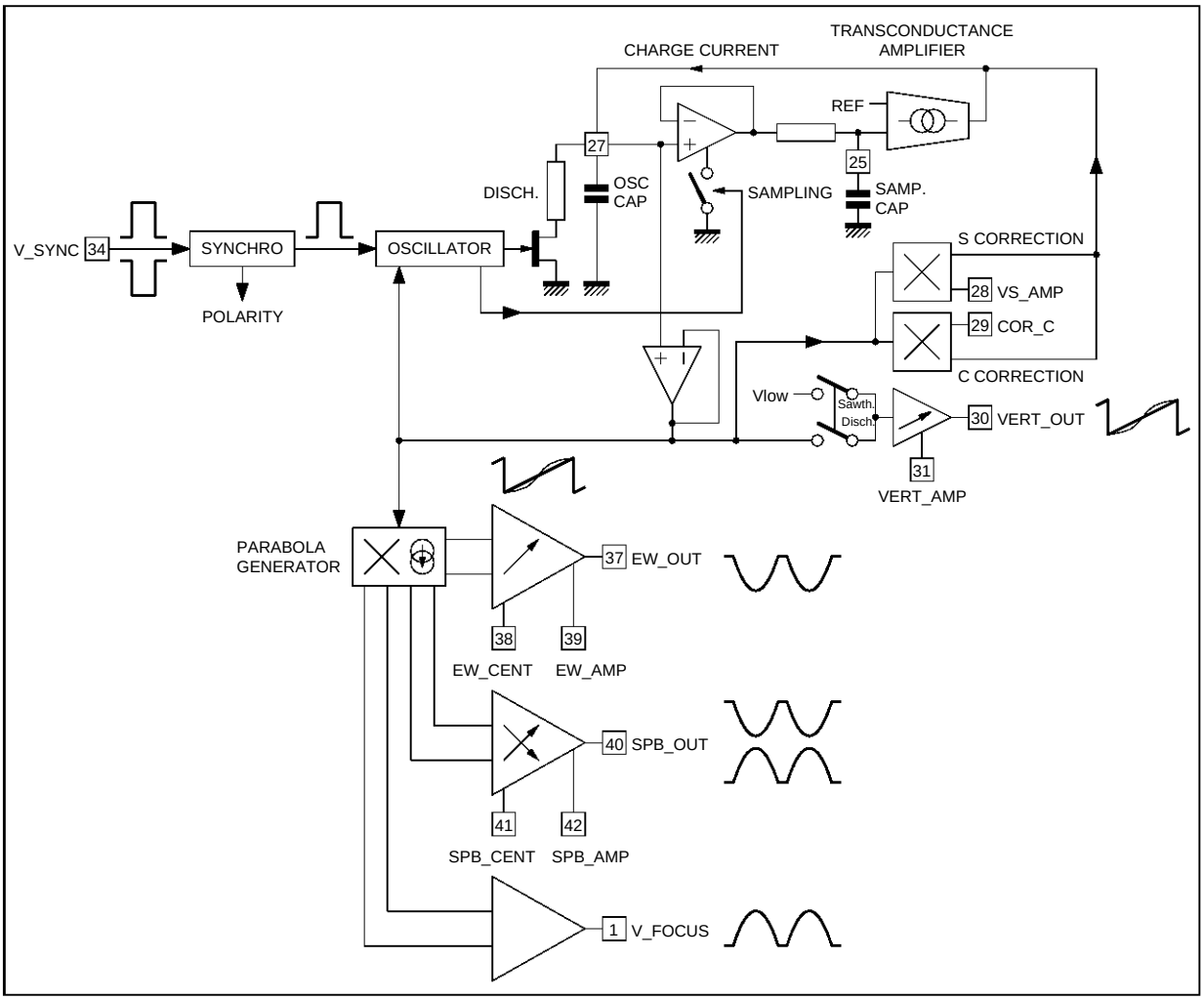
The output connection is the same as the two other corrections (Pins 37-40).

It is important to note that the parasitic parabola during the discharge of the vertical oscillator capacitor is suppressed.

OPERATING DESCRIPTION (continued)

VERTICAL PART

Figure 21 : Vertical Part Block Diagram



The vertical part generates a fixed amplitude ramp which can be affected by a S and C correction shape. Then, the amplitude of this ramp is adjusted to drive an external power stage.

The internal reference voltage used for the vertical part is available between Pin 26 and Pin 24. It can be used as voltage reference for any DC adjusment to keep a high accuracy to each adjustment. Its typical value is :

$$V_{26} = V_{REF} = 8V.$$

The charge of the external capacitor on Pin 27 (V_{CAP}) generates a fixed amplitude ramp between the internal voltages, V_L ($V_L = V_{REF}/4$) and V_H ($V_H = 5/8 \cdot V_{REF}$).

OPERATING DESCRIPTION (continued)

VERTICAL PART (continued)

Function

When the synchronisation pulse is not present, an internal current source sets the free running frequency. For an external capacitor, C_{OSC} = 150nF, the typical free running frequency is 100Hz.

Typical free running frequency can be calculated by :

$$f_0\,(Hz) = 1.5 \cdot 10^{-5} \cdot \frac{1}{C_{OSC}\,(nF)}$$

A negative or positive TTL level pulse applied on Pin 34 (VSYNC) can synchronise the ramp in the frequency range [fmin, fmax]. This frequency range depends on the external capacitor connected on Pin 27. A capacitor in the range [150nF, 220nF] is recommanded for application in the following range : 50Hz to 120Hz.

Typical maximum and minimum frequency, at 25°C and without any correction (S correction or C correction), can be calculated by :
$f_{max} = 2.5 \cdot f_0$ and $f_{min} = 0.33 \cdot f_0$

If S or C corrections are applied, these values are slighty affected.

If an external synchronisation pulse is applied, the internal oscillator is automaticaly caught but the amplitude is no more constant. An internal correction is activated to adjust it in less than half a second: the highest voltage of the ramp on Pin 27 is sampled on the sampling capacitor connected on Pin 25 (VAGCCAP) at each clock pulse and a transconductance amplifier generates the charge current of the capacitor. The ramp amplitude becomes again constant.

It is recommanded to use a AGC capacitor with low leakage current. A value lower than 100nA is mandatory.

Pin 36, Vfly is the vertical flyback input used to generate the composite blanking signal. If Vfly is not used, (V_{REF} - 0.5), at minimum, must be connected to this input.

DC Control Adjustments

Then, S and C correction shapes can be added to this ramp. This frequency independent S and C corrections are generated internally; their amplitude are DC adjustable on Pin 28 (V_{SAMP}) and Pin 29 (COR-C).

S correction is non effective for V_{SAMP} lower than $V_{REF}/4$ and maximum for $V_{SAMP} = 3/4 \cdot V_{REF}$.

C correction is non effective for COR-C grounded and maximum for :
COR-C = $V_{REF}/4$ or COR-C = $3/4 \cdot V_{REF}$.

Endly, the amplitude of this S and C corrected ramp can be adjusted by the voltage applied on Pin 31 (V_{AMP}). The adjusted ramp is available on Pin 30 (V_{OUT}) to drive an external power stage. The gain of this stage is typically ±30% when voltage applied on Pin 31 is in the range $V_{REF}/4$ to $3/4 \cdot V_{REF}$. The DC value of this ramp is kept constant in the frequency range , for any correction applied on it. Its typical value is : $V_{DCOUT} = V_{MID} = 7/16 \cdot V_{REF}$.

A DC voltage is available on Pin 32 (V_{DCOUT}). It is driven by the voltage applied on Pin 33 (V_{POS})

For a voltage control range between $V_{REF}/4$ and $3/4 \cdot V_{REF}$, the voltage available on Pin 32 is :
$V_{DCOUT} = 7/16 \cdot V_{REF} \pm 300mV$.

So, the V_{DCOUT} voltage is correlated with DC value of V_{OUT}. It increases the accuracy when temperature varies.

Basic Equations

In first approximation, the amplitude of the ramp on Pin 30 (V_{OUT}) is :

$$V_{OUT} - V_{MID} = (V_{CAP} - V_{MID})\,[1 + 0.16 \cdot (V_{AMP} - V_{REF}/2)]$$

with $V_{MID} = 7/16 \cdot V_{REF}$; typically 3.5V
V_{MID} is the middle value of the ramp on Pin 27
$V_{CAP} = V_{27}$, ramp with fixed amplitude.

On Pin 32 (V_{DCOUT}), the voltage (in volts) is calculated by : $V_{DCOUT} = V_{MID} + 0.16 \cdot (V_{POS} - V_{REF}/2)$.
V_{POS} is the voltage applied on Pin 33.

The current available on Pin 27
(when $V_{SAMP} = V_{REF}/4$) is :
$I_{OSC} = 3/8 \cdot V_{REF} \cdot C_{OSC} \cdot f$
C_{OSC} : capacitor connected on Pin 27
f synchronisation frequency

The recommanded capacitor value on Pin 25 (V_{AGC}) is 470nF. Its ensures a good stability of the internal closed loop.

INTERNAL SCHEMATICS

Figure 22

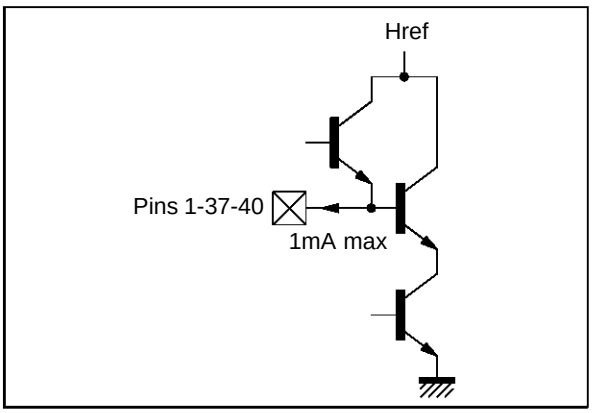


Figure 23

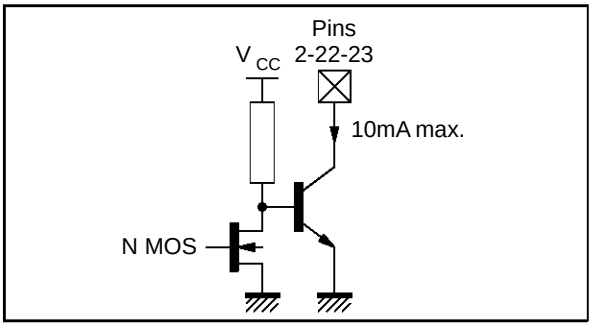


Figure 24

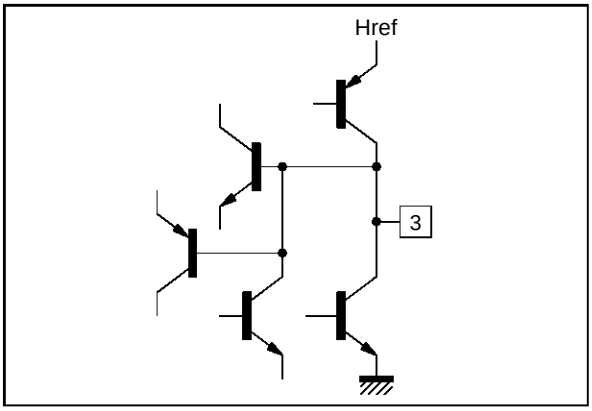
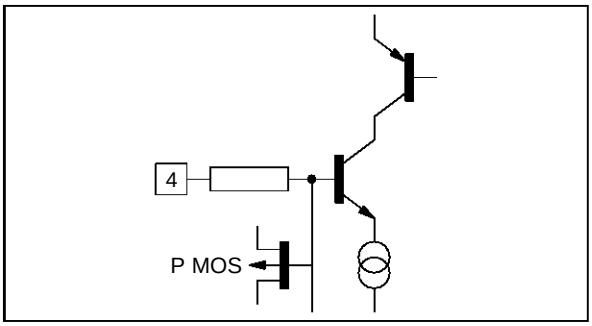


Figure 25



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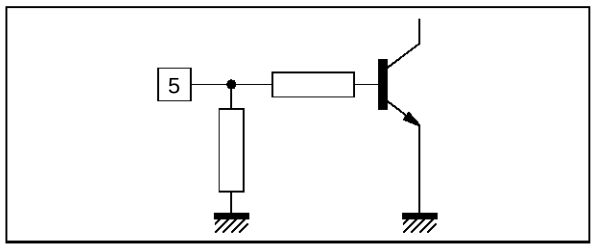

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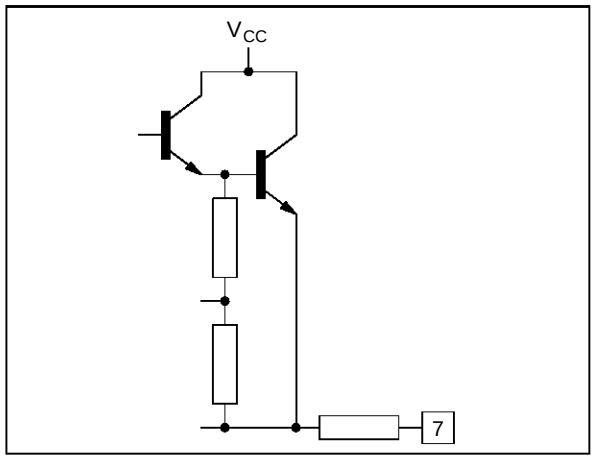

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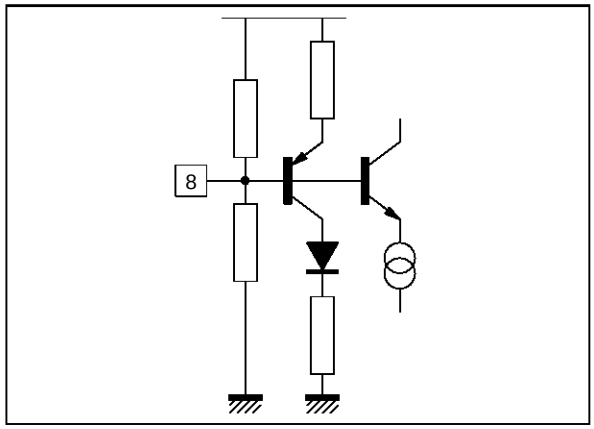
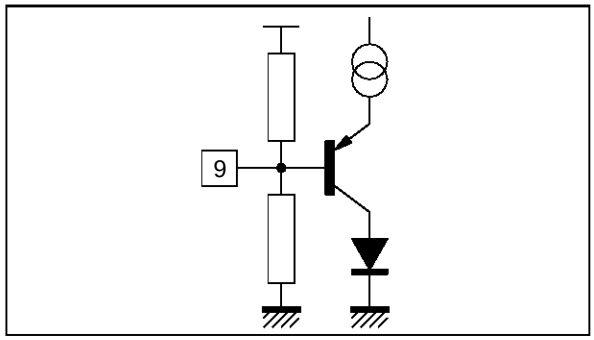
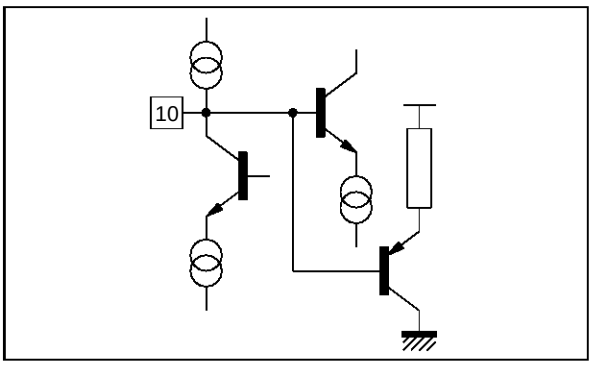


Figure 29



INTERNAL SCHEMATICS (continued)

Figure 30



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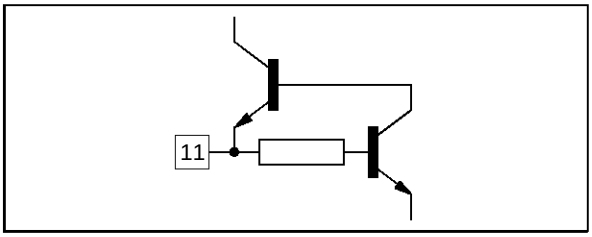


Figure 32

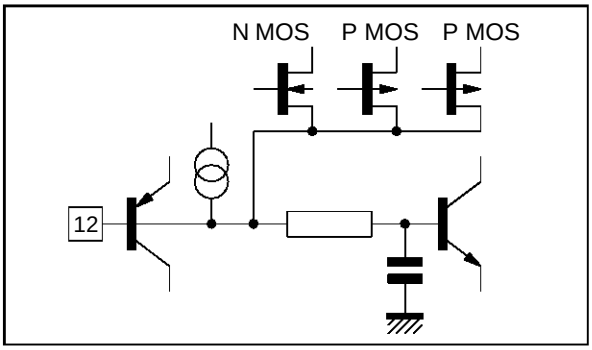


Figure 33

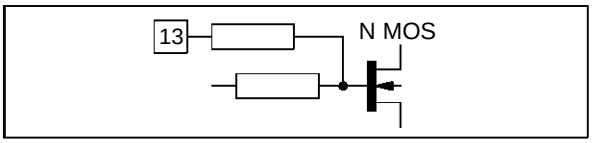


Figure 34

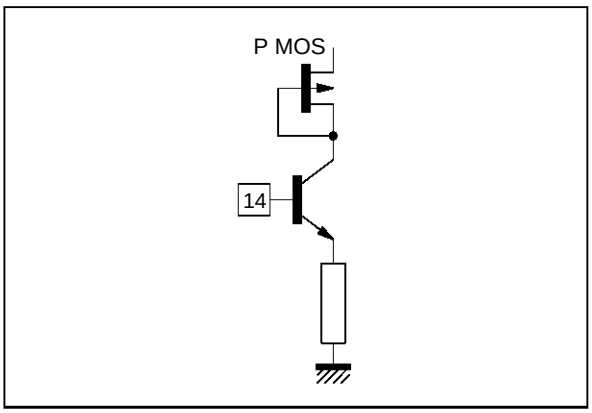


Figure 35

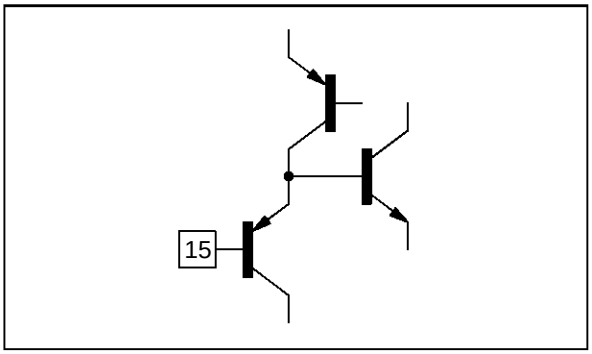
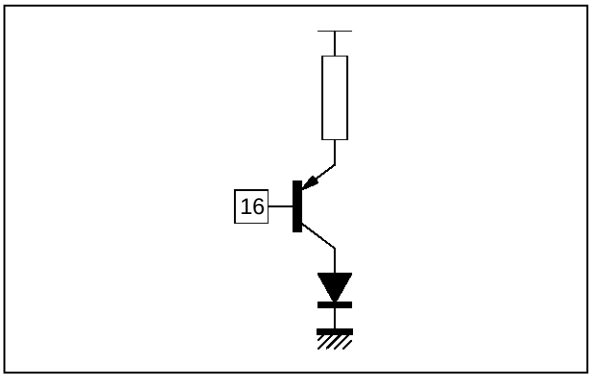


Figure 36



INTERNAL SCHEMATICS (continued)

Figure 37

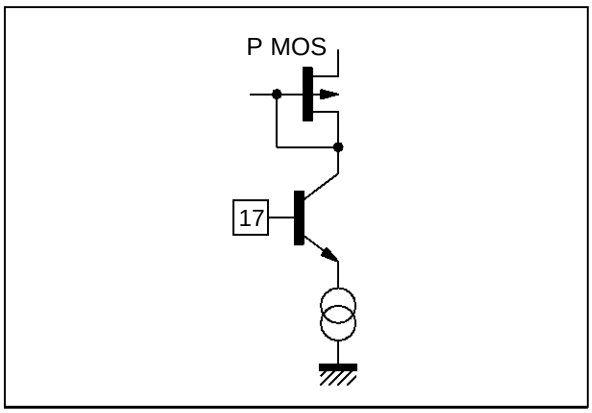


Figure 38

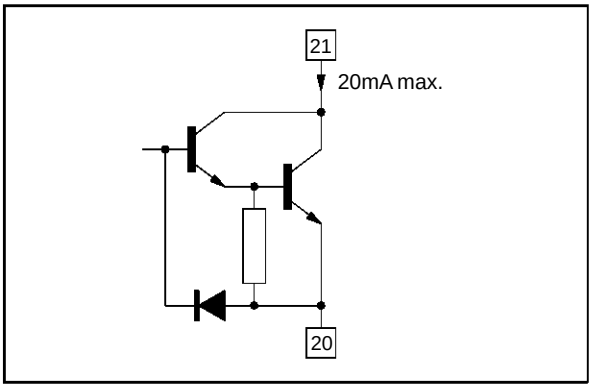


Figure 39

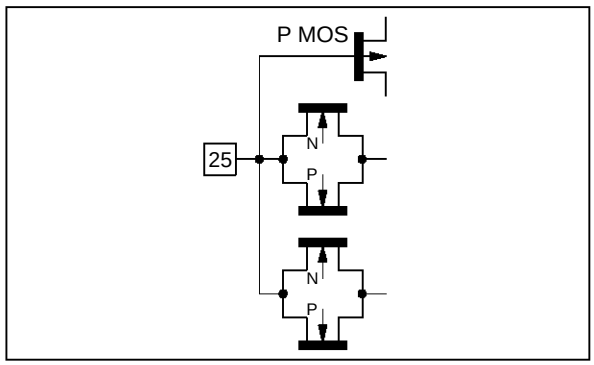


Figure 40

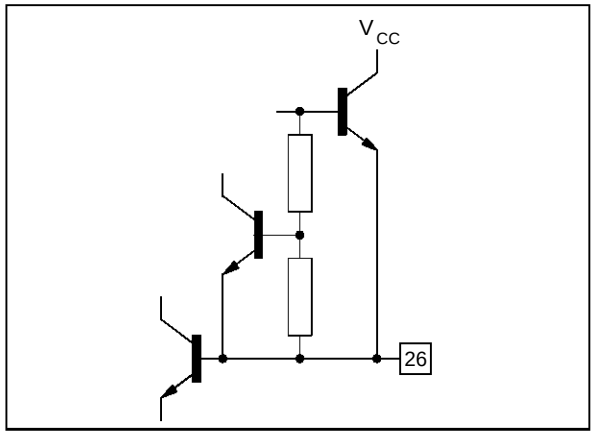
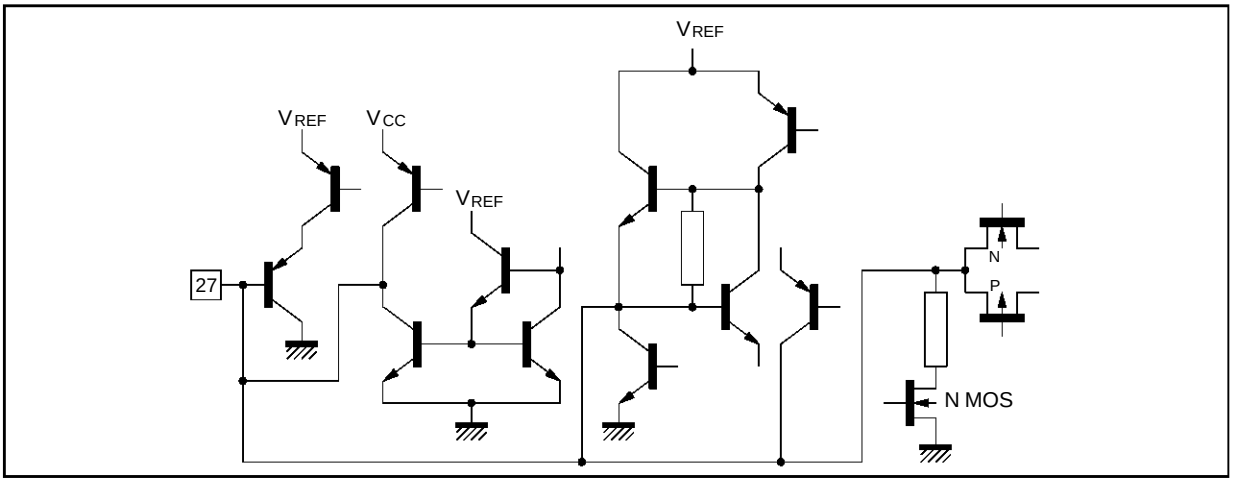
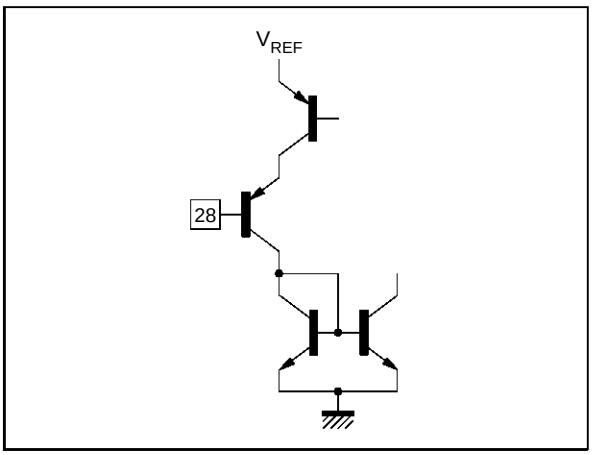


Figure 41



INTERNAL SCHEMATICS (continued)

Figure 42



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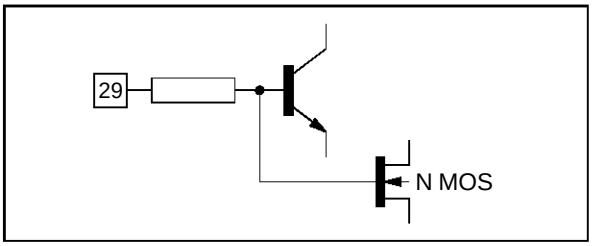

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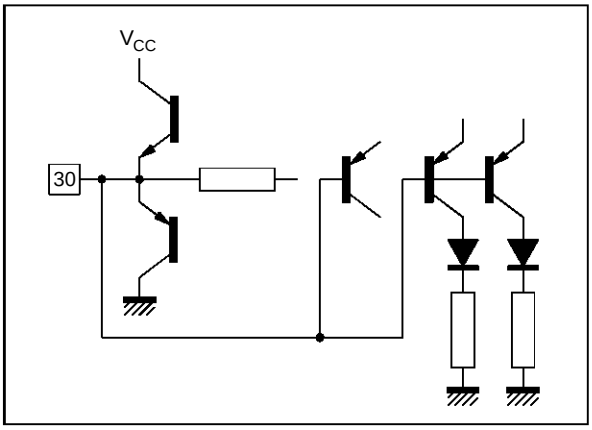

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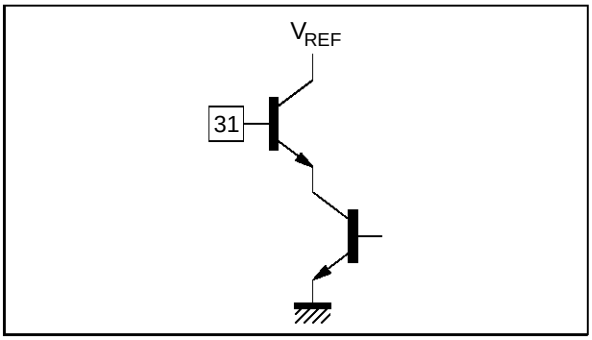

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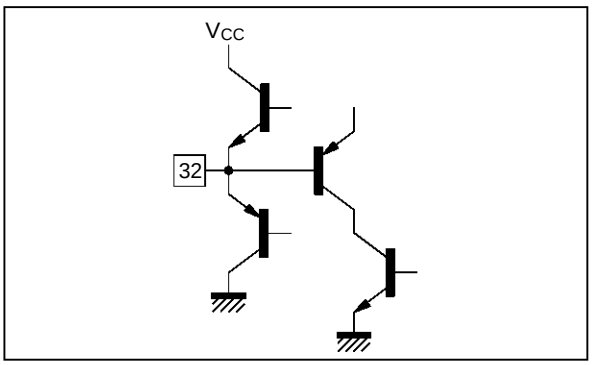
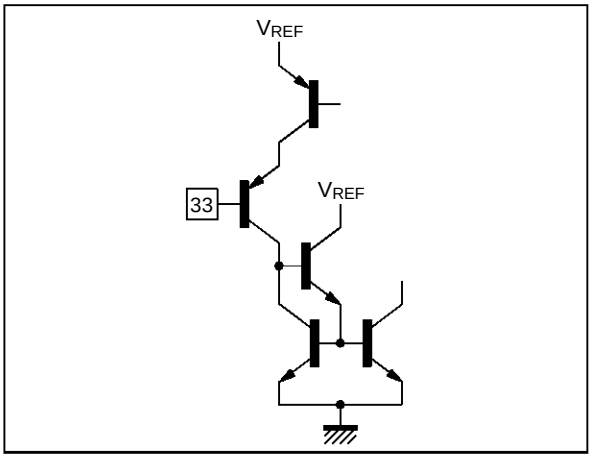


Figure 47



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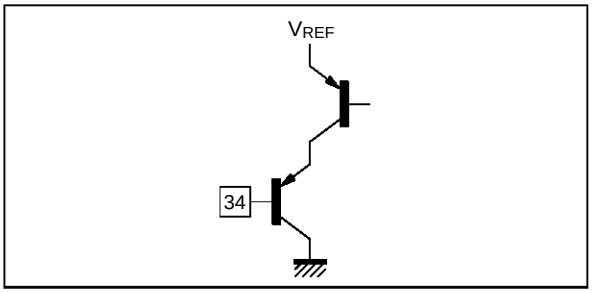
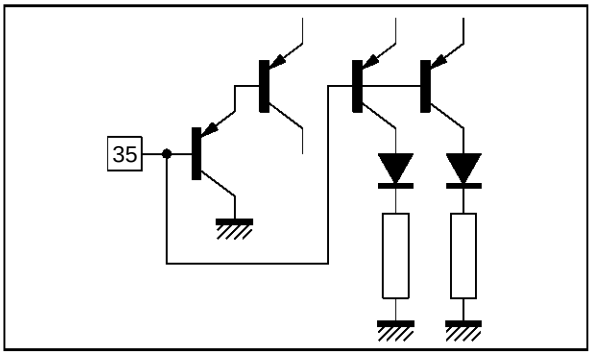


Figure 49



INTERNAL SCHEMATICS (continued)

Figure 50

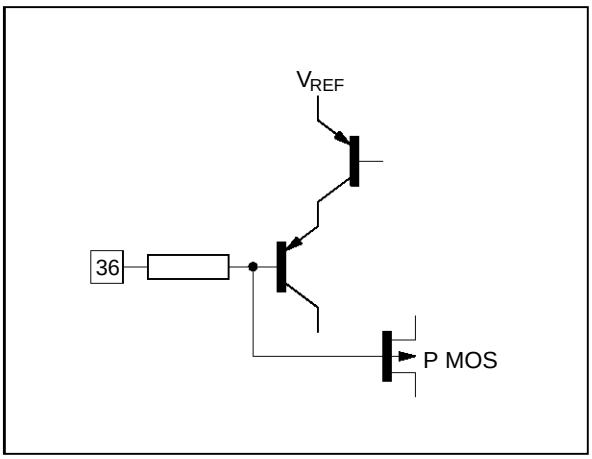
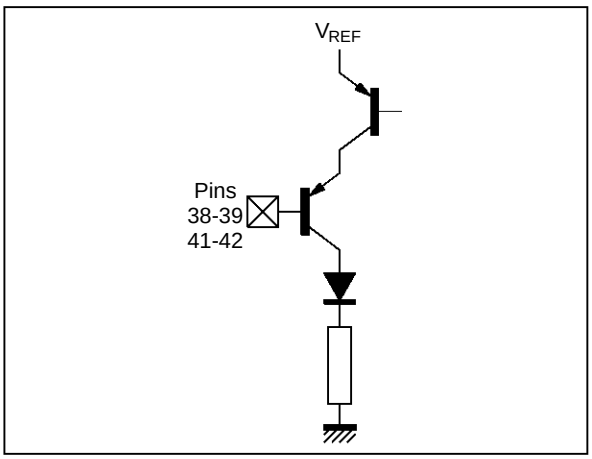
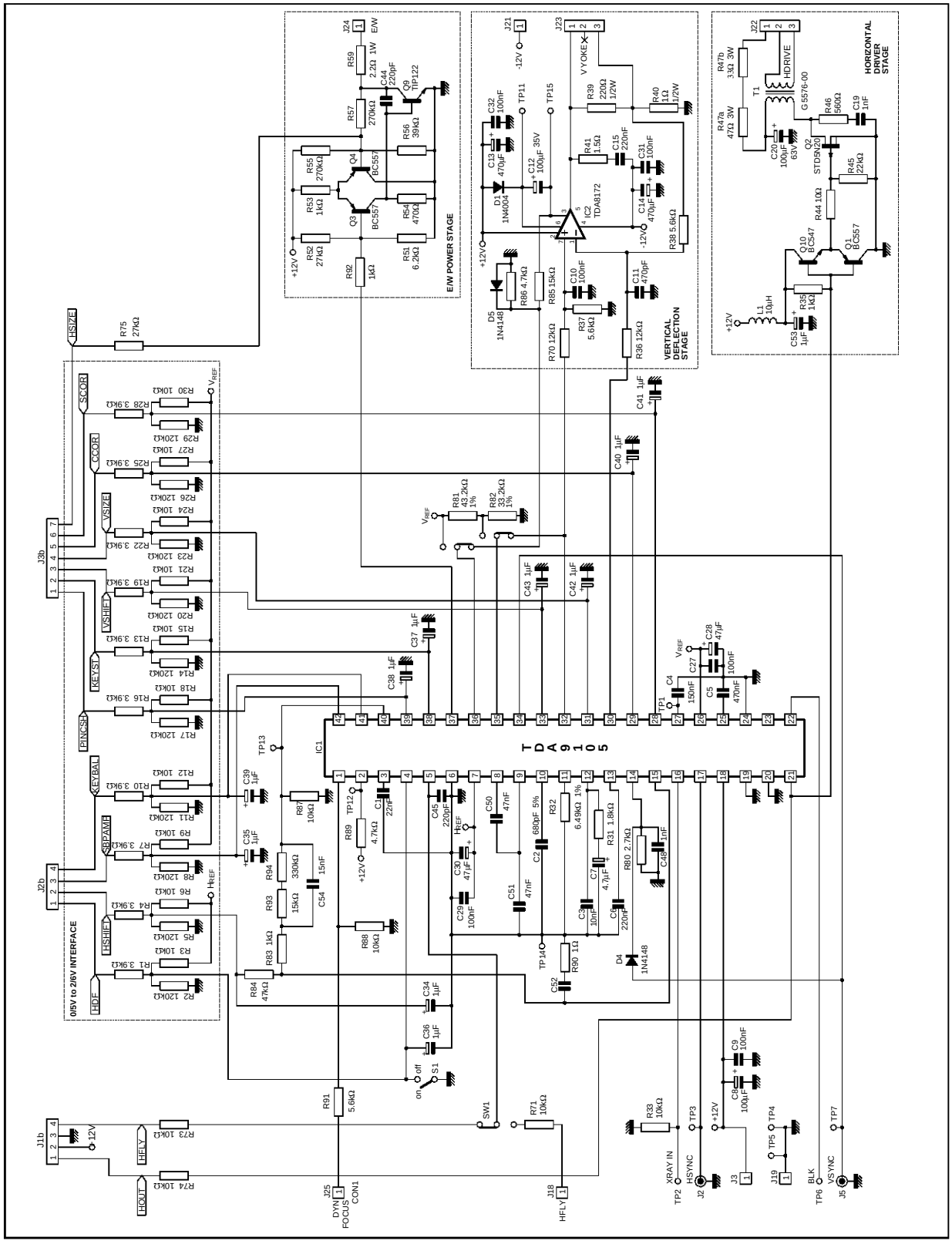


Figure 51



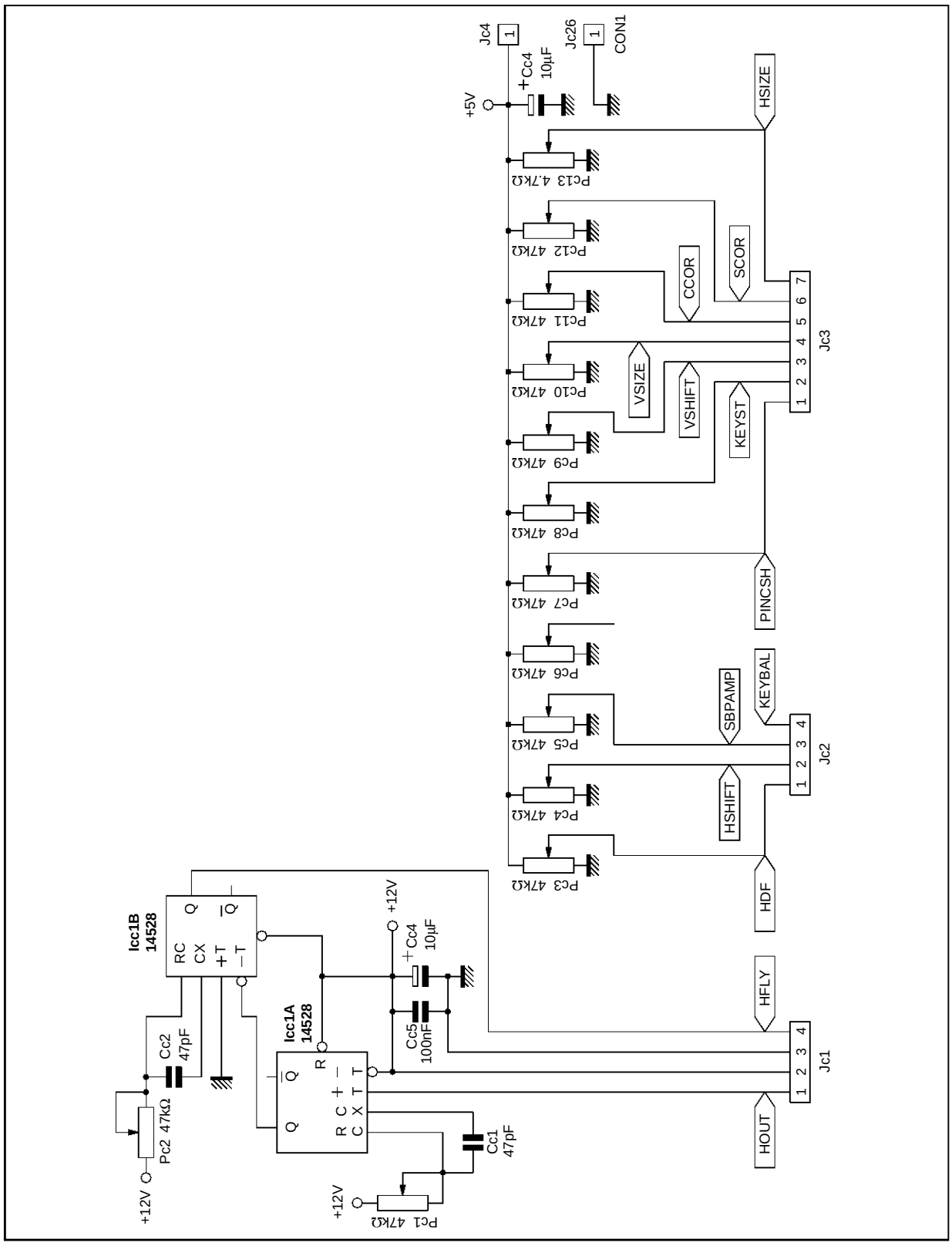
APPLICATION DIAGRAMS

Figure 52 : Demonstration Board



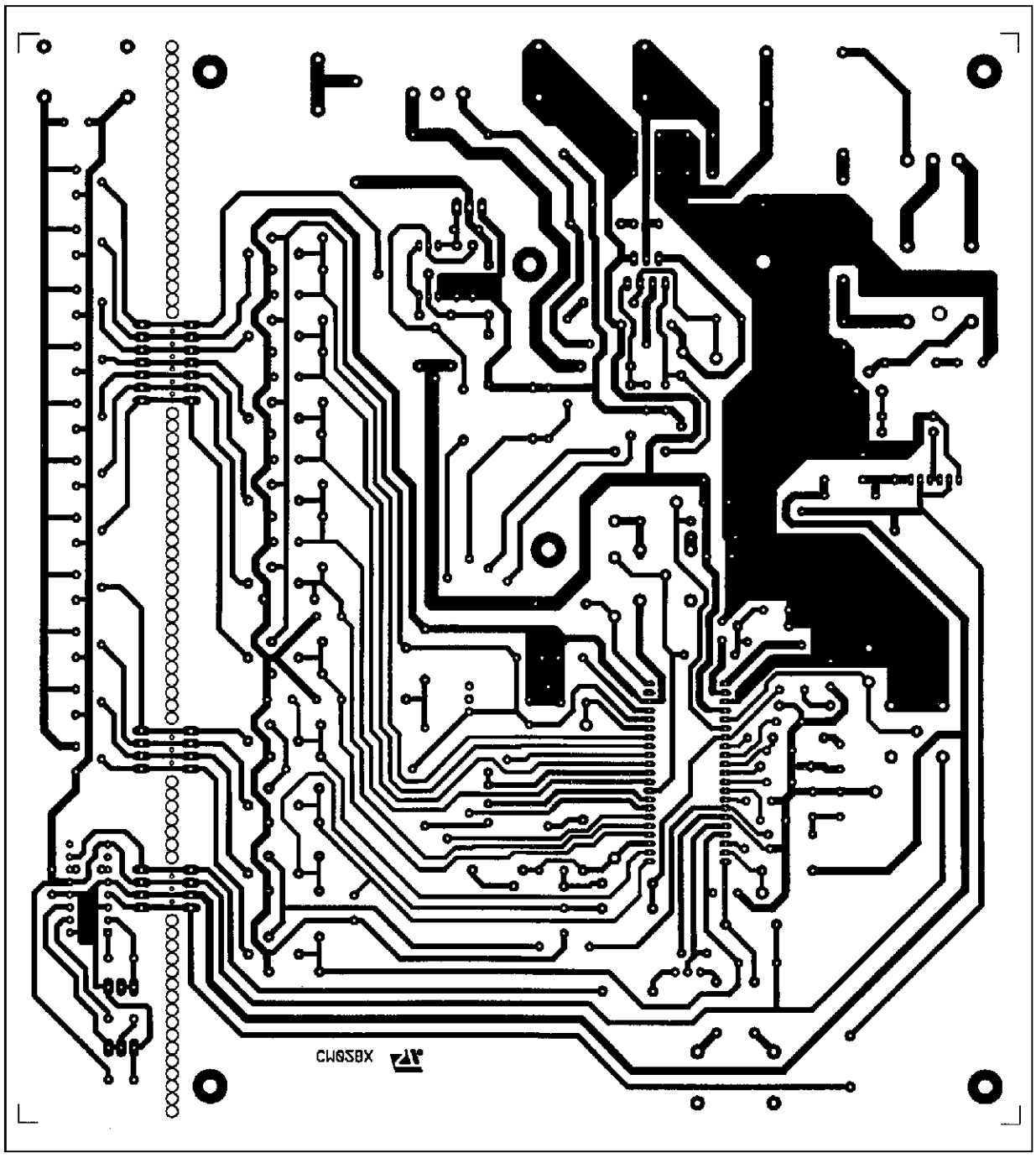
APPLICATION DIAGRAMS

Figure 53 : Control Board



APPLICATION DIAGRAMS

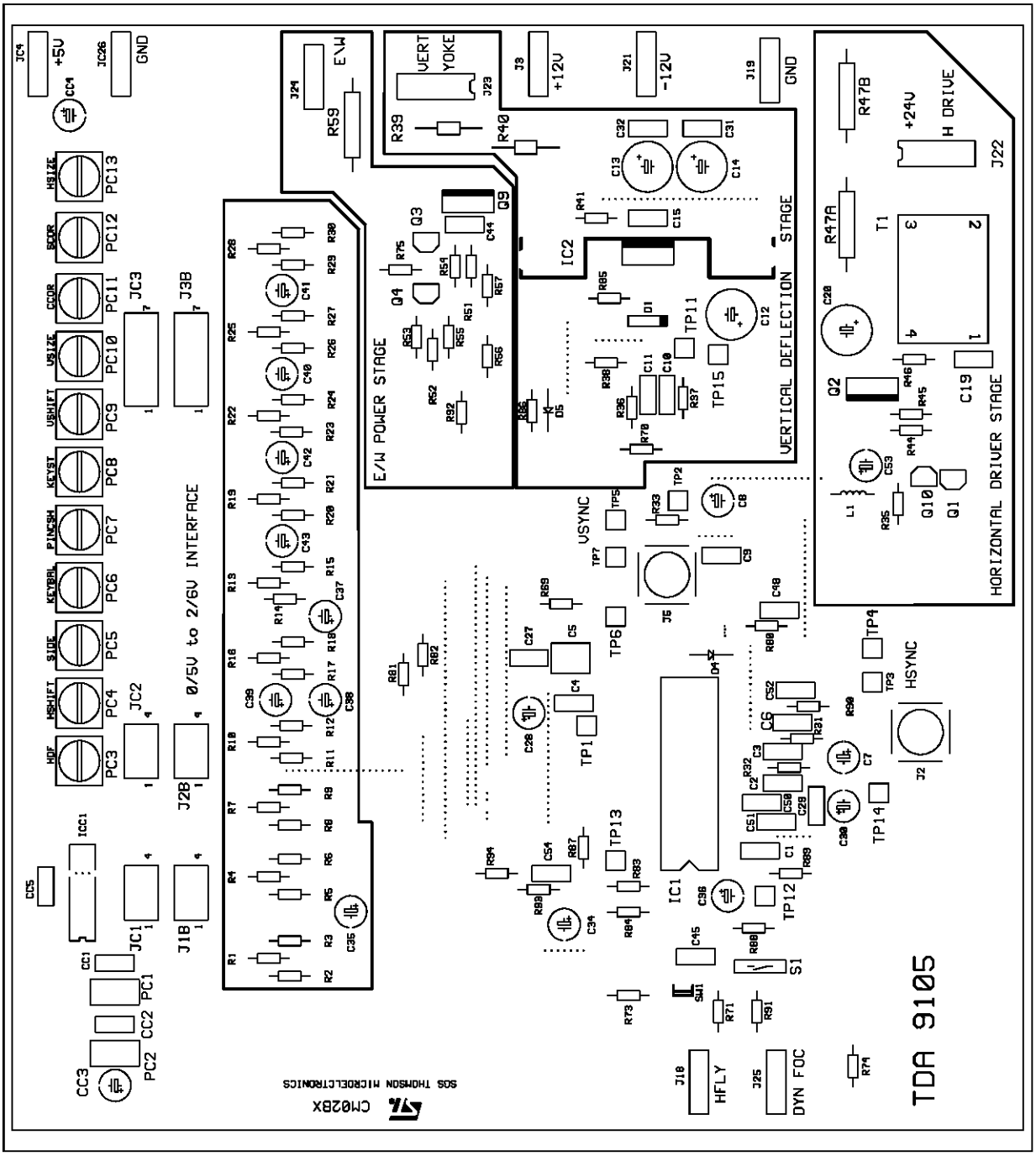
Figure 54 : PCB Layout



9105-72.TIF

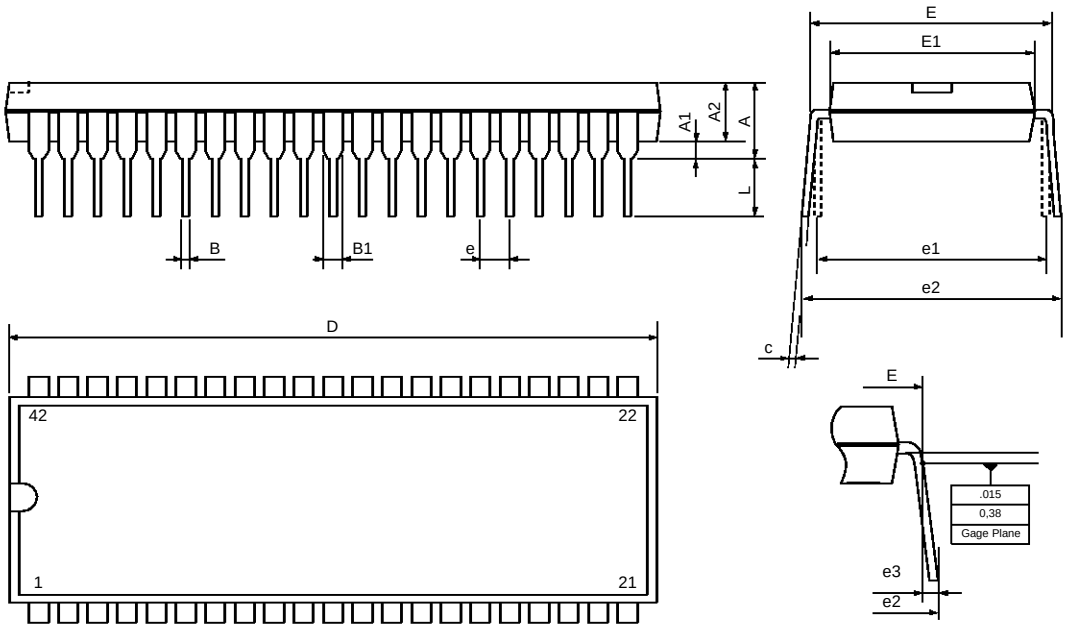
APPLICATION DIAGRAMS

Figure 55 : Components Layout



PACKAGE MECHANICAL DATA

42 PINS - PLASTIC SHRINK DIP



PMSDIP42.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.08			0.200
A1	0.51			0.020		
A2	3.05	3.81	4.57	0.120	0.150	0.180
B	0.36	0.46	0.56	0.0142	0.0181	0.0220
B1	0.76	1.02	1.14	0.030	0.040	0.045
c	0.23	0.25	0.38	0.0090	0.0098	0.0150
D	37.85	38.10	38.35	1.490	1.5	1.510
E	15.24		16.00	0.60		0.629
E1	12.70	13.72	14.48	0.50	0.540	0.570
e		1.778			0.070	
e1		15.24			0.60	
e2			18.54			0.730
e3			1.52			0.060
L	2.54	3.30	3.56	0.10	0.130	0.140

SDIP42.TBL