DATA SHEET

TDA8798
Dual 8-bit, 100 Msps A/D converter with DPGA

Objective specification
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Dual 8-bit, 100 Msps A/D converter with DPGA

TDA8798

FEATURES

- Dual 8-bit Analog-to-Digital Converter (ADC)
- Sampling rate up to 100 million samples per second (Msps)
- Dual 34 dBV 6-bit Digitally Programmable Gain Amplifier (DPGA) with optional power-off
- Optional external equalization filter with capacitive coupling between DPGA and ADC
- Serial Interface (SI) for DPGA gain control using either parallel load mode or count-up/count-down mode
- 3.3 V TTL/CMOS compatible I/O
- Differential or single-ended TTL/CMOS clock interface
- AC or DC coupling for DPGA inputs.

APPLICATIONS

- High-dynamic range acquisition front-ends
- Digital data storage read channels.

GENERAL DESCRIPTION

The TDA8798 is a dual 8-bit ADC with DPGA.
The 100 Msps maximum sampling rate and 34 dBV DPGA gain range optimizes the ADC for high dynamic range applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		3.15	3.3	3.45	V
V_{DDD}	digital supply voltage		3.0	3.3	3.6	V
V_{DDO}	output stage supply voltage		2.7	3.3	3.6	V
I_{DDA}	analog supply current	with DPGAEN LOW	–	106	–	mA
		with DPGAEN HIGH	–	tbf	–	mA
I_{DDD}	digital supply current		–	30	–	mA
I_{DDO}	output stage supply current		–	3	–	mA
INL	DC integral non-linearity	from IC analog input to digital output; ramp input; f_{CLK} = 100 MHz				
		with DPGA at $G_{(min)}$	–	±3.0	tbf	LSB
		without DPGA	–	±1.0	tbf	LSB
DNL	DC differential non-linearity	from IC analog input to digital output; ramp input; f_{CLK} = 100 MHz				
		with DPGA at $G_{(min)}$	–	±0.5	tbf	LSB
		without DPGA	–	±0.5	tbf	LSB
$V_{n(o)(rms)}$	output referred noise (RMS value)	DPGA at $G_{(max)}$; Z_i = 50 Ω; noise bandwidth = 15 MHz	–	tbf	2	mV_{rms}
$B_{(-3dB)(ADC)}$	ADC –3 dB analogue bandwidth	at $V_{i(dif)(FS)}$	–	120	–	MHz
$B_{(-3dB)(DPGA)}$	DPGA –3 dB bandwidth	at $V_{i(dif)(max)}$	30	tbf	–	MHz
$f_{(sample)(max)}$	maximum sampling rate		100	–	–	Msps
P_{tot}	total power dissipation	with DPGAEN LOW	–	460	500	mW
		with DPGAEN HIGH	–	tbf	tbf	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8798HL	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

BLOCK DIAGRAM

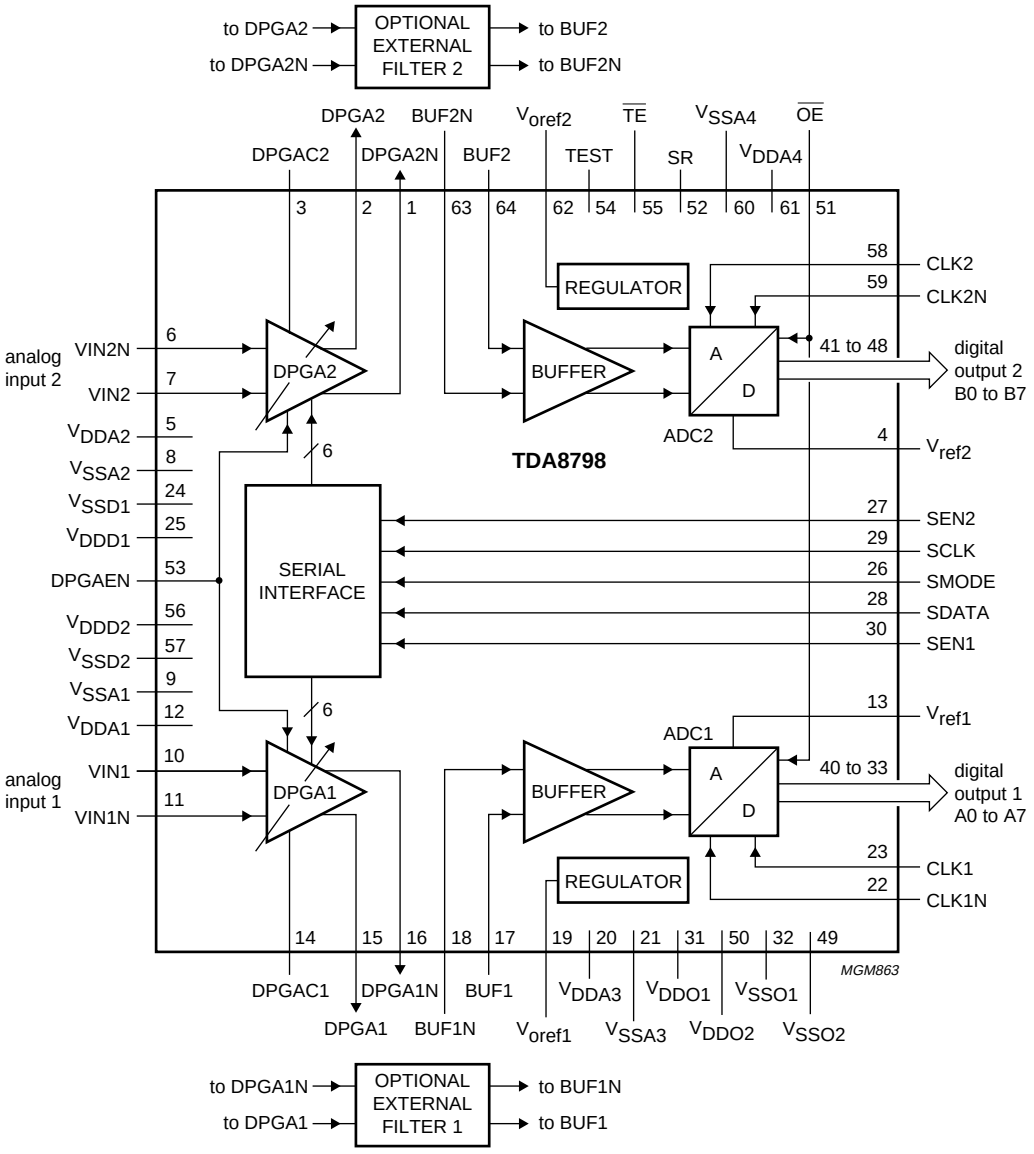
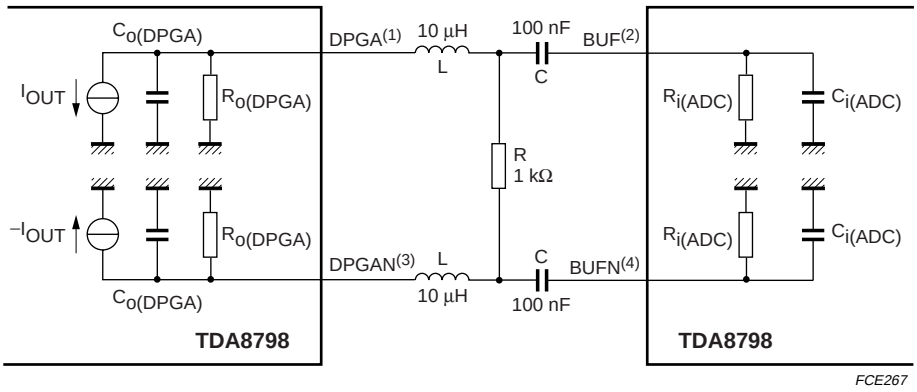


Fig.1 Block diagram.



External filtering may be used between DPGA and ADC to limit the noise bandwidth.

The external filter has a low-pass cut-off frequency of $f_{l(-3dB)} \approx \frac{1}{2\pi} \times \frac{R/2 + R_{o(DPGA)}}{L}$.

and a high-pass cut-off frequency of $f_{h(-3dB)} \approx \frac{1}{2\pi} \times \frac{1}{R_{i(ADC)} \times C}$.

Other types of filter may be used if DC biasing is correct.

(1) DPGA1/DPGA2
(2) BUF1/BUF2
(3) DPGA1N/DPGA2N
(4) BUF1N/BUF2N

Fig.2 External filter.

PINNING

SYMBOL	PIN	DESCRIPTION
DPGA2N	1	DPGA2 inverting output
DPGA2	2	DPGA2 non-inverting output
DPGAC2	3	DPGA2 bandwidth limitation control
V_{ref2}	4	ADC2 reference output
V_{DDA2}	5	DPGA2 analog supply voltage
VIN2N	6	DPGA2 inverting input voltage
VIN2	7	DPGA2 non-inverting input voltage
V_{SSA2}	8	DPGA2 analog ground
V_{SSA1}	9	DPGA1 analog ground
VIN1	10	DPGA1 non-inverting input voltage
VIN1N	11	DPGA1 inverting input voltage
V_{DDA1}	12	DPGA1 analog supply voltage
V_{ref1}	13	ADC1 reference output
DPGAC1	14	DPGA1 bandwidth limitation control
DPGA1	15	DPGA1 non-inverting output
DPGA1N	16	DPGA1 inverting output

SYMBOL	PIN	DESCRIPTION
BUF1	17	buffer1 non-inverting input
BUF1N	18	buffer1 inverting input
V_{oref1}	19	buffer1 common mode reference output
V_{DDA3}	20	ADC1 analog supply voltage 3
V_{SSA3}	21	ADC1 analog ground 3
CLK1N	22	ADC1 inverting clock input
CLK1	23	ADC1 non-inverting clock input
V_{SSD1}	24	digital ground 1
V_{DDD1}	25	digital supply voltage 1
SMODE	26	serial interface mode input
SEN2	27	serial interface enable 2 (active low)
SDATA	28	serial interface data input
SCLK	29	serial interface clock input
SEN1	30	serial interface enable 1 (active low)
V_{DDO1}	31	output stage supply voltage 1
V_{SSO1}	32	output stage ground 1
A7	33	channel 1 output bit 7 (MSB)
A6	34	channel 1 output bit 6
A5	35	channel 1 output bit 5
A4	36	channel 1 output bit 4
A3	37	channel 1 output bit 3
A2	38	channel 1 output bit 2
A1	39	channel 1 output bit 1
A0	40	channel 1 output bit 0 (LSB)
B0	41	channel 2 output bit 0 (LSB)
B1	42	channel 2 output bit 1
B2	43	channel 2 output bit 2
B3	44	channel 2 output bit 3
B4	45	channel 2 output bit 4
B5	46	channel 2 output bit 5
B6	47	channel 2 output bit 6
B7	48	channel 2 output bit 7 (MSB)
V_{SSO2}	49	output stage ground 2
V_{DDO2}	50	output stage supply voltage 2
$\overline{OE}$	51	digital output enable (active LOW)
SR	52	digital output bit slew-rate control
DPGAEN	53	DPGA enable (active LOW)
TEST	54	test input (to be grounded)
$\overline{TE}$	55	track-and-hold enable (active LOW)
V_{DDD2}	56	digital supply voltage 2
V_{SSD2}	57	digital ground 2

SYMBOL	PIN	DESCRIPTION
CLK2	58	ADC2 non-inverting clock input
CLK2N	59	ADC2 inverting clock input
V_{SSA4}	60	ADC2 analog ground 4
V_{DDA4}	61	ADC2 analog supply voltage 4
V_{oref2}	62	buffer2 common mode reference output
BUF2N	63	buffer2 inverting input
BUF2	64	buffer2 non-inverting input

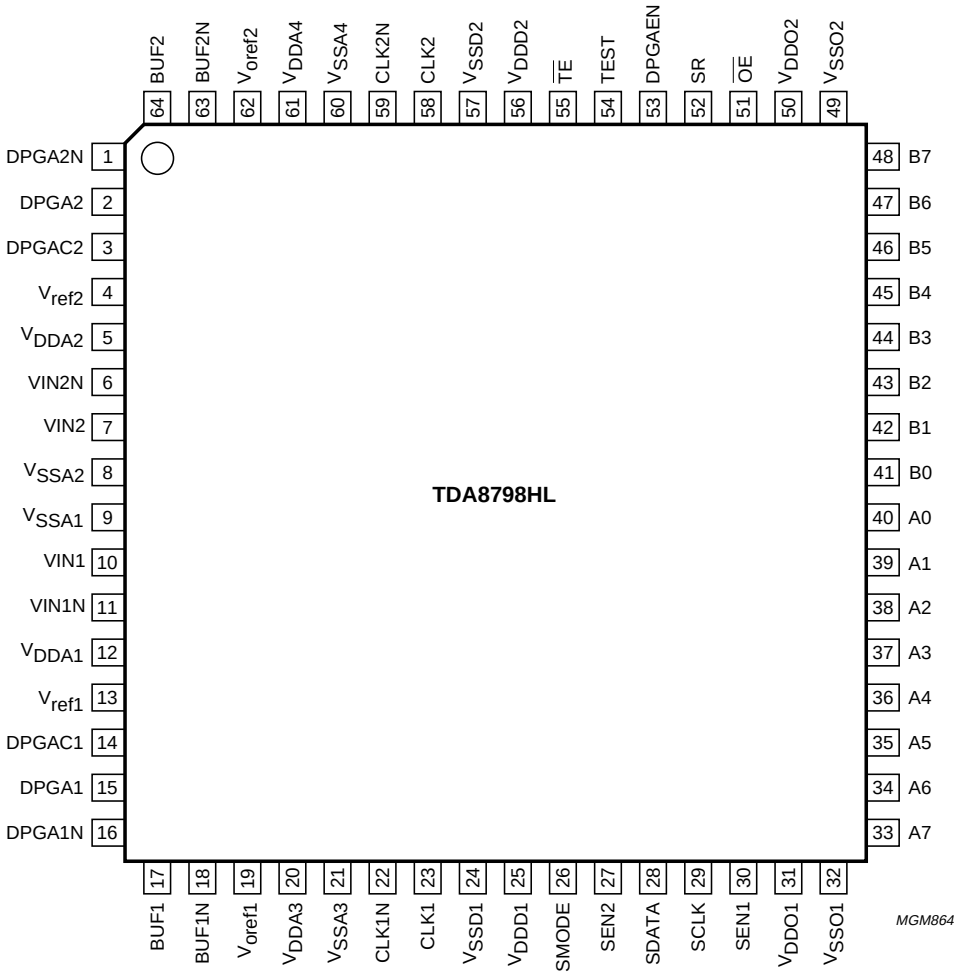


Fig.3 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA8798 comprises two independent fully differential signal chains each having a DPGA and a high-speed ADC. A serial interface allows the gain of each DPGA to be controlled independently. To improve signal conditions, an AC-coupled external filter can be connected between a DPGA and ADC. The TDA8798 can be used as a dual 8-bit ADC without DPGA functionality, using less power.

Digitally Programmable Gain Amplifier (DPGA)

The gain of the differential DPGA is programmable from 0 to 34 dBV in 63 equal steps by a 6-bit word output in parallel from a gain control register in the SI. For all gain settings, the DPGA signal bandwidth exceeds 30 MHz. The settling time between gain changes can be adjusted by an external decoupling capacitor connected to DPGAC1 (pin 14) and/or DPGAC2 (pin 3). The analog input signals can be either AC or DC coupled. When used only as a dual 8-bit ADC, both DPGAs can be disabled to reduce power consumption.

Analog-to-Digital Converter (ADC)

The 8-bit ADC converts the differential analog input signal into a binary output format at a maximum conversion rate of 100 Msps. All digital input and output signals are TTL/CMOS compatible.

The ADC clock signal can be from either a differential or a single-ended source; when single-ended, the unused clock input pin should be decoupled externally. The analog input to the ADC is AC coupled.

When used only as a dual ADC, the ADC can be externally biased by regulator output V_{oref1} (pin 19) and/or V_{oref2} (pin 62) using series resistors of, for example, 50 Ω, connected to the ADC buffer inputs providing a lower input impedance. This requires V_{oref1} and/or V_{oref2} to be decoupled to ground by a 10 nF capacitor.

V_{ref1} (pin 13) and/or V_{ref2} (pin 4) provide a voltage corresponding to the bias of the ADC which can be used as a reference output to an external control circuit. Alternatively, an external control voltage can be applied to these pins to adjust the full-scale range of the ADC.

Serial Interface (SI)

The SI allows the gain of each DPGA to be controlled independently using either a parallel load mode or a count-up/count-down mode. The gain control mode is selected by the state of SMODE. The operation of DPGA gain control is shown in Timing diagram, (see Fig.4).

Parallel load mode

This mode loads gain control data serially into a decoder in the SI. Each of the six bits are loaded on the rising edge of SCLK. After the load has completed, SEN goes inactive, loading the data in parallel to a gain control register in the SI, changing the gain of the DPGA.

Count-up/count-down mode

Count-up/count-down mode is selected when SMODE is in the opposite state to parallel load mode. This mode either increments or decrements the SI gain control register in one-bit steps when SEN and SCLK are both active; the state of SDATA determines the count direction (up or down). This allows the gain of the DPGA to be changed asynchronously and intermittently.

ADC digital outputs

Digital noise on the internal supply lines increases when the V_{DDO} voltage increases, affecting the crosstalk between channels. This effect can be reduced by making SR (pin 52) HIGH, changing the slew-rate of the ADC digital outputs.

Table 1 Serial interface truth table; see notes 1 and 2

SMODE	SCLK	SEN1	SEN2	SDATA	ACTION
0	X, ↓	1	1	U	WAIT
0	↑	1	1	Di	SISR: SISR ← Di
0	↑	0	1	1	SISR: SISR ← 1 GCR1: GCR1 + 1
0	↑	0	1	0	SISR: SISR ← 0 GCR1: GCR1 – 1
0	↑	1	0	1	SISR: SISR ← 1 GCR2: GCR2 + 1
0	↑	1	0	0	SISR: SISR ← 0 GCR2: GCR2 – 1
0	↑	0	0	1	SISR: SISR ← 1 GCR1: GCR1 + 1 GCR2: GCR2 + 1
0	↓	0	0	0	SISR: SISR ← 0 GCR1: GCR1 – 1 GCR2: GCR2 – 1
1	X, ↓	X, ↓	X, ↓	U	WAIT
1	↑	X, ↓	X, ↓	Di	SISR: SISR ← Di
1	X, ↓	↑	X, ↓	U	GCR1: SISR
1	X, ↓	X, ↓	↑	U	GCR2: SISR
1	X, ↓	↑	↑	U	GCR1: SISR GCR2: SISR

Notes

1. '← Di': shifting LSB and loading new LSB with value Di.
2. In count-up/count-down mode, the gain control register cannot be incremented above the maximum gain value of 63, or decremented below the minimum gain value of 0.

Table 2 Abbreviations

SYMBOL	DESCRIPTION
GCR1	DPGA1 gain control register value
GCR2	DPGA2 gain control register value
SISR	Serial interface shift register value
X	can be either logic state 0 or logic state 1
	rising edge
	falling edge
U	can be either undefined logic state X rising edge or falling edge
Di	Data input

Table 3 $\overline{TE}$ truth table

$\overline{TE}$	ADC TRACK-AND-HOLD
0	track-and-hold enabled
1	track enabled

Table 4 SR truth table

SR	ADC DIGITAL OUTPUT SLEW RATE
0	maximum
1	minimum

Table 5 DPGAEN truth table

DPGAEN	DPGA FUNCTIONALITY
0	enabled
1	disabled

Table 6 Gain Control

GAIN CONTROL REGISTER VALUE	GAIN (dBV)
000000	0.00
000001	0.54
000010	1.08
...	...
...	...
...	...
111110	33.46
111111	34.00

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage		–0.3	+7.0	V
V_{DDD}	digital supply voltage		–0.3	+7.0	V
V_{DDO}	output stage supply voltage		–0.3	+7.0	V
ΔV_{DDX}	supply voltage differences between				
	V_{DDA} and V_{DDD}		–1.0	+1.0	V
	V_{DDO} and V_{DDD}		–1.0	+1.0	V
	V_{DDA} and V_{DDO}		–1.0	+1.0	V
$V_{i(VIN)}$	input voltage range on VIN1 and VIN2 (pins 10 and 7)	referenced to V_{SSA}	–0.3	+7.0	V
I_O	output current		–	10	mA
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		0	70	°C
T_j	junction temperature		–	104	°C

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	68	K/W

CHARACTERISTICS

$V_{DDA} = V_5$ (or V_{12} or V_{20} or V_{61}) to V_8 (or V_9 or V_{21} or V_{60}) = 3.15 to 3.45 V; $V_{DDD} = V_{25}$ (or V_{56}) to V_{24} (or V_{57}) = 3.0 to 3.6 V; $V_{DDO} = V_{31}$ (or V_{50}) to V_{32} (or V_{49}) = 2.7 to 3.6 V; V_{SSA}, V_{SSD} and V_{SSO} shorted together; V_{DDA} to V_{DDD} = –0.25 to +0.25 V; V_{DDD} to V_{DDO} = –0.25 to +0.90 V; V_{DDA} to V_{DDO} = –0.25 to +0.75 V; T_{amb} = 0 to 70 °C; typical values measured at $V_{DDA} = V_{DDD} = V_{DDO}$ = 3.3 V and T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDA}	analog supply voltage		3.15	3.3	3.45	V
V_{DDD}	digital supply voltage		3.0	3.3	3.6	V
V_{DDO}	output stage supply voltage		2.7	3.3	3.6	V
I_{DDA}	analog supply current	DPGAEN LOW	–	106	–	mA
		DPGAEN HIGH	–	tbf	–	mA
I_{DDD}	digital supply current		–	30	–	mA
I_{DDO}	output stage supply current	f_{CLK} = 100 MHz; ramp input	–	3	–	mA
Digital programmable gain amplifiers						
ANALOG INPUTS (VIN1, VIN1N, VIN2 AND VIN2N)						
$V_{i(dif)(max)(p-p)}$	maximum differential input voltage (peak-to-peak value)	at $G_{(min)}$	–	0.5	–	V
		at $G_{(max)}$	–	10	–	mV
$V_{i(cm)(DPGA)}$	common mode input voltage		tbf	2.8	tbf	V
$I_{i(DPGA)}$	input current	at $V_{i(cm)(DPGA)}$	–	tbf	–	µA
$R_{i(DPGA)}$	input resistance		1	–	–	kΩ
$C_{i(DPGA)}$	input capacitance		–	–	5	pF
ANALOG OUTPUTS (DPGA1, DPGA1N, DPGA2 AND DPGA2N)						
$V_{o(dif)(max)(p-p)}$	maximum differential output voltage (peak-to-peak value)	at $G_{(min)}$	–	0.5	–	V
		at $G_{(max)}$	–	0.5	–	V
$V_{o(cm)(DPGA)}$	common mode output voltage		–	3.1	–	V
$R_{o(DPGA)}$	output resistance	at $V_{o(cm)(DPGA)}$	–	115	160	Ω
$C_{o(DPGA)}$	output capacitance		–	–	5	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
BANDWIDTH AND SETTLING						
$B_{(-3dB)(DPGA)}$	DPGA −3 dB bandwidth	at $V_{i(dif)(max)}$	30	tbf	–	MHz
t_{st}	settling time	full-scale transition 10% to 90%	40	–	–	ns
$t_{d(g)}$	group delay	f_i up to 15 MHz				
		at $G_{(min)}$	–	tbf	–	ps
		at $G_{(max)}$	–	tbf	–	ps
GAIN						
$G_{(min)}$	minimum gain setting		tbf	0	tbf	dBV
$G_{(max)}$	maximum gain setting		tbf	34	tbf	dBV
G_{step}	gain step size		–	0.54	–	dBV
$G_{step(L)}$	gain step size linearity (actual gain step/average − 1)		−0.75	–	+0.75	dBV
$G_{(m)(c-c)}$	channel-to-channel gain matching	at $G_{(min)}$	–	tbf	–	dB
		at $G_{(max)}$	–	tbf	–	dB
$\Delta G/\Delta T$	amplifier gain stability as a function of temperature	at $G_{(min)}$	–	8	tbf	mdB/°C
		at $G_{(max)}$	–	8	tbf	mdB/°C
$\Delta G/\Delta V_{DD}$	amplifier gain stability as a function of power supply voltage	at $G_{(min)}$	–	0.4	tbf	dB/V
		at $G_{(max)}$	–	0.8	tbf	dB/V
GAIN SWITCHING; T_{AMB} = 25 °C						
$t_{st(G-G)}$	settling time between two consecutive gain settings	C_L = 68 pF	–	160	–	ns
t_{PD}	propagation delay		–	–	20	ns
REJECTION						
PSRR	power supply rejection ratio	DC to 15 MHz at $G_{(min)}$	40	–	–	dB
CMRR	common mode rejection ratio		40	–	–	dB
HARMONICS; T_{AMB} = 25 °C						
HD2	second harmonic distortion	f_i = 15 MHz; at $V_{o(dif)(max)}$; at gain control register:				
		00H	40	tbf	–	dB
		20H	40	tbf	–	dB
		3FH	–	tbf	–	dB
HD3	third harmonic distortion	f_i = 15 MHz; at $V_{o(dif)(max)}$; at gain control register:				
		00H	tbf	50	–	dB
		20H	tbf	50	–	dB
		3FH	–	50	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
NOISE						
$V_{n(o)(rms)}$	output referred noise (RMS value)	DPGA at $G_{(max)}$; Z_i = 50 Ω; noise bandwidth = 15 MHz	–	tbf	2	mV_{rms}
ADC (without DPGA; f_{CLK} = 100 MHz; from buffer input to digital output)						
ANALOG INPUTS (BUF1, BUF1N, BUF2 AND BUF2N)						
$V_{i(dif)(FS)(p-p)}$	differential input voltage full-scale amplitude; (peak-to-peak value)		–	500	–	mV
$V_{i(cm)(ADC)}$	common mode input voltage		–	tbf	–	V
$I_{i(ADC)}$	input current	at $V_{i(cm)(ADC)}$	–	tbf	–	µA
$R_{i(ADC)}$	input resistance		–	20	–	kΩ
$C_{i(ADC)}$	input capacitance		–	3	–	pF
STATIC LINEARITY						
$NL_{dc(i)}$	DC integral non-linearity	ramp input;				
		without DPGA	–	±1.0	tbf	LSB
		with DPGA at $G_{(min)}$	–	±3.0	tbf	LSB
$NL_{dc(dif)}$	DC differential non-linearity	ramp input;				
		without DPGA	–	±0.5	tbf	LSB
		with DPGA at $G_{(min)}$	–	±0.5	tbf	LSB
DYNAMIC PERFORMANCE						
THD	total harmonic distortion	f_i = 4.43 MHz	–	–55	–	dB
S/N	signal-to-noise ratio	without harmonics	–	–46	–	dB
BANDWIDTH						
$B_{(-3dB)(ADC)}$	ADC –3 dB analog bandwidth		–	120	–	MHz
CROSSTALK BETWEEN ADC1 AND ADC2						
α_{ct}	crosstalk between channels		–	–40	–	dB
CLOCK INPUTS: CLK1, CLK1N, CLK2 AND CLK2N; note 1						
V_{IL}	LOW-level clock input voltage		–	–	0.8	V
V_{IH}	HIGH-level clock input voltage		2.0	–	V_{DDD}	V
I_{IH}	HIGH-level clock input current		–	–	100	µA
I_{IL}	LOW-level clock input current		–100	–	–	µA
DIGITAL CONTROL INPUTS ($\overline{OE}$, $\overline{TE}$, TEST, DPGAEN AND SR)						
V_{IL}	LOW-level input voltage		–	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	V_{DDD}	V
I_{IH}	HIGH-level input current		–5	–	+5	µA
I_{IL}	LOW-level input current		–5	–	+5	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DIGITAL OUTPUTS (A0 TO A7 AND B0 TO B7)						
V_{OL}	LOW-level output voltage	I_O = 1 mA	–	–	0.4	V
V_{OH}	HIGH-level output voltage	I_O = –1 mA	V_{DDO} – 0.4 V	–	–	V
I_{OZ}	output current in 3-state mode	V_O > 0.4 V; V_O < (V_{DDO} – 0.4 V)	–20	–	+20	µA
ADC CLOCK TIMING						
$f_{CLK(max)}$	maximum clock frequency		100	–	–	MHz
$t_{W(CLKL)}$	clock pulse width LOW duration		4.0	–	–	ns
$t_{W(CLKH)}$	clock pulse width HIGH duration		4.0	–	–	ns
$t_{r(CLK)}$	clock pulse rise time		0.75	1	2	ns
$t_{f(CLK)}$	clock pulse fall time		0.75	1	2	ns
DATA TIMING (see Fig.4); F_{CLK} = 100 MHz; C_{DPGAC} = 10 pF						
$t_{d(s)(D)}$	data sampling delay time		–	–	tbf	ns
$t_{d(Q)}$	data output delay time	SR HIGH	–	5.0	tbf	ns
		SR LOW	–	tbf	tbf	ns
$t_{h(Q)}$	data output hold time	SR HIGH	tbf	5.0	–	ns
		SR LOW	tbf	tbf	–	ns
3-STATE OUTPUT DELAY TIMES (see Fig.6)						
t_{dZH}	output delay enable at logic HIGH	SR HIGH	–	tbf	tbf	ns
		SR LOW	–	tbf	tbf	ns
t_{dZL}	output delay enable at logic LOW	SR HIGH	–	tbf	tbf	ns
		SR LOW	–	tbf	tbf	ns
t_{dHZ}	output delay disable at logic HIGH	SR HIGH	–	tbf	tbf	ns
		SR LOW	–	tbf	tbf	ns
t_{dLZ}	output delay disable at logic LOW	SR HIGH	–	tbf	tbf	ns
		SR LOW	–	tbf	tbf	ns
ADC REFERENCE OUTPUTS (V_{REF1} AND V_{REF2})						
$V_{o(ref)}$	ADC reference output voltage		–	1.24	–	V
$R_{o(ref)}$	ADC reference output resistance	at $V_{o(ref)}$	–	–	10	Ω
$I_{o(ref)(max)}$	ADC reference maximum output current		–	4.0	–	mA
$C_{o(ref)}$	ADC reference output capacitance		–	–	3	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
COMMON MODE REFERENCE OUTPUTS (V_{OREF1} AND V_{OREF2})						
$V_{o(ref)}$	reference output voltage		–	V_{DDA} – 0.42 V	–	V
$R_{o(ref)}$	reference output resistance	at $V_{o(cm)(ref)}$	–	400	–	Ω
$I_{o(ref)}$	reference maximum output current	at $V_{o(cm)(ref)}$ – 0.2 V	–	170	–	µA
$C_{o(ref)}$	reference output capacitance		–	–	3	pF
Serial Interface						
DIGITAL INPUTS (SEN1, SEN2, SCLK, SDATA AND SMODE)						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	V_{DDD}	V
I_{IH}	HIGH-level input current		–5	0	+5	µA
I_{IL}	LOW-level input current		–5	0	+5	µA
GAIN CONTROL DATA TIMING (see Fig.4)						
$f_{SCLK(max)}$	maximum clock frequency		5	–	–	MHz
$t_{W(SCLKH)}$	clock pulse width HIGH		20	–	–	ns
$t_{W(SCLKL)}$	clock pulse width LOW		20	–	–	ns
$t_{su(SEN-SCLK)}$	SEN to SCLK set-up time		5	–	–	ns
$t_{h(SEN-SCLK)}$	SEN to SCLK hold time		5	–	–	ns
$t_{su(SDATA-SCLK)}$	SDATA to SCLK set-up time		5	–	–	ns
$t_{h(SMODE-SCLK)}$	SMODE to SCLK hold time		5	–	–	ns
$t_{h(SMODE-SEN)}$	SMODE to SEN hold time		5	–	–	ns
$t_{d(SEN-Q)}$	delay SEN rising edge to change gain control register value		–	–	5	ns
$t_{d(SCLK-Q)}$	delay SCLK rising edge to change gain control register value		–	–	5	ns

Note

1. Single-ended clock signal sources are allowed. The unused clock input is internally biased at the logical threshold (1.65 V for nominal supply conditions), and should be correctly decoupled.

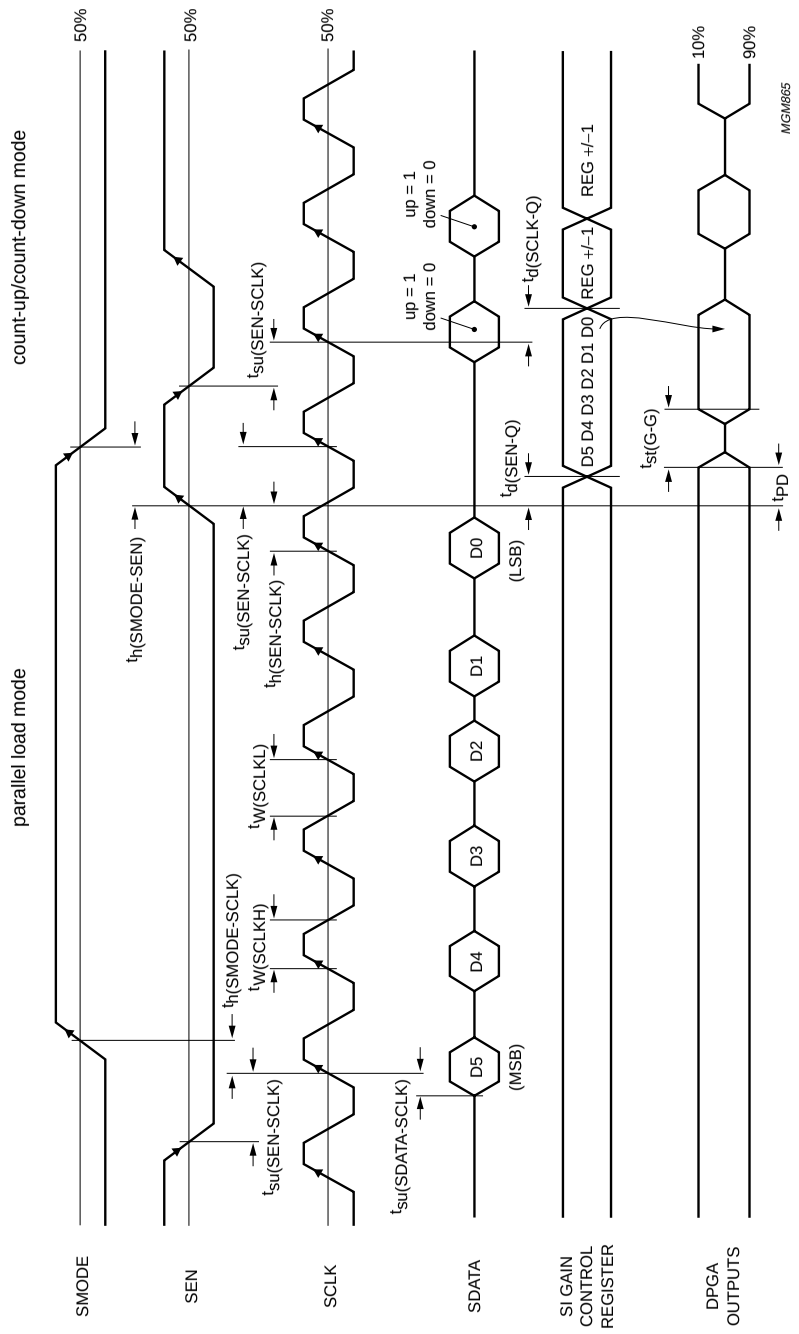


Fig.4 Timing diagram of serial interface.

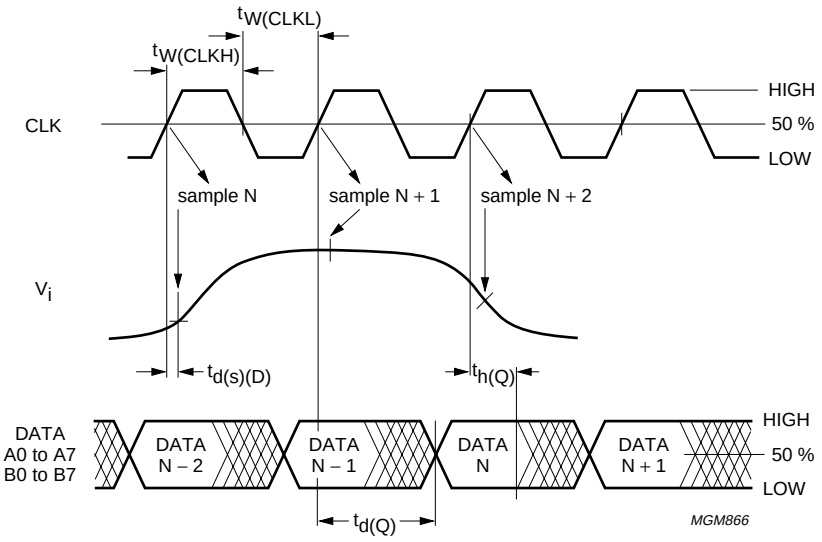


Fig.5 Timing diagram for the ADC.

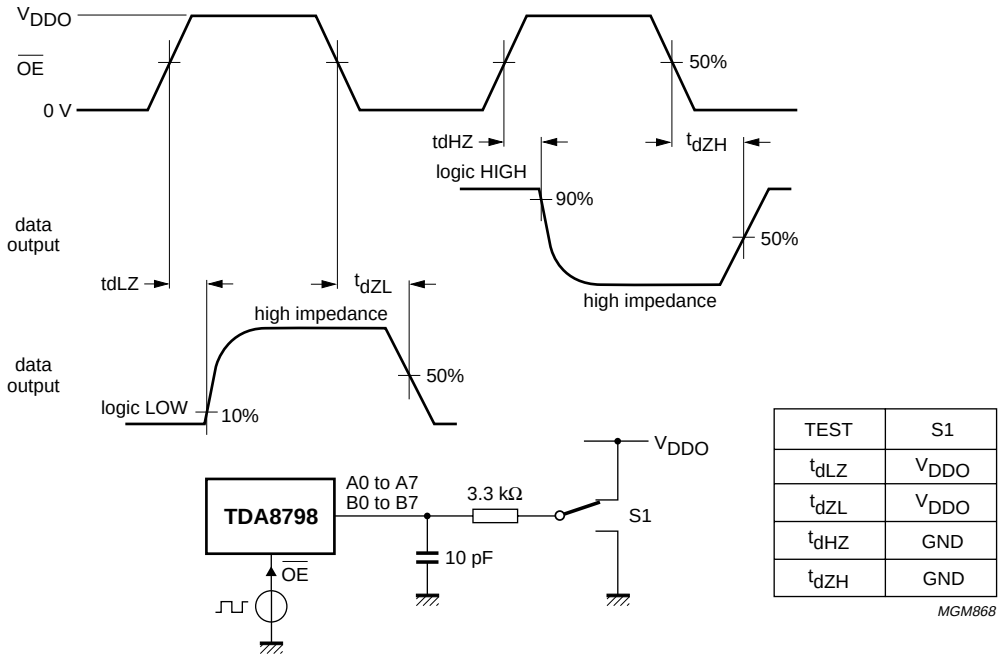
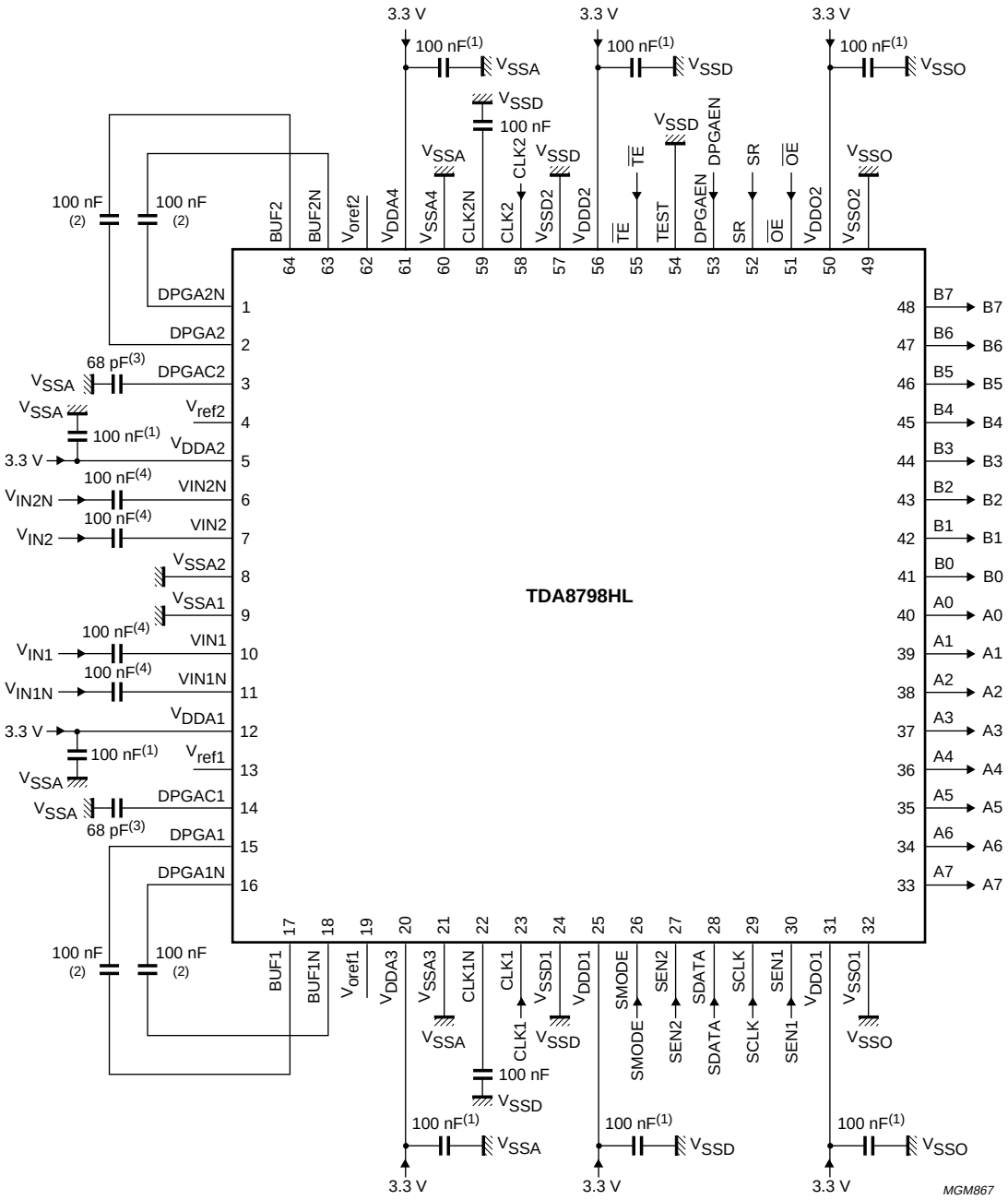


Fig.6 Timing diagram and test conditions of 3-state output delay time.

TEST AND APPLICATION INFORMATION



Analog and digital supplies must be separate and decoupled.

(1) Supply decoupling capacitor must be placed as close as possible to the chip's pin. Value may need changing depending on the external filter characteristics.

(2) Capacitor may be replaced when an external filter is used with AC coupling.

(3) Capacitor value may be changed to adjust settling time between DPGA gain changes.

(4) Capacitor value may need changing depending on the high-pass cut-off frequency of the external filter.

Fig.7 Application diagram.

INTERNAL PIN CONFIGURATIONS

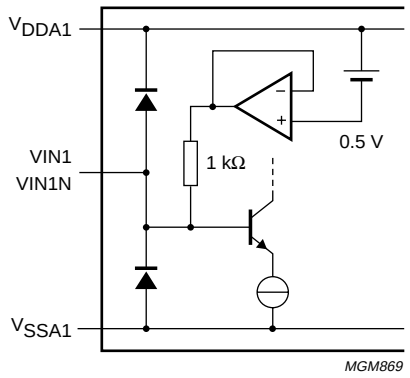


Fig.8 DPGA1 analog input.

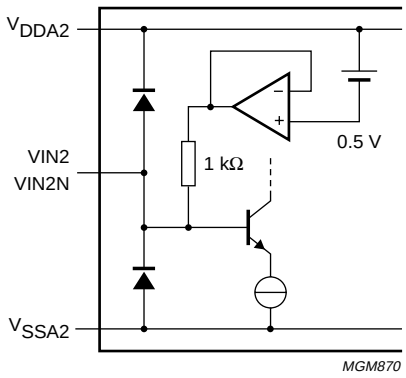


Fig.9 DPGA2 analog input.

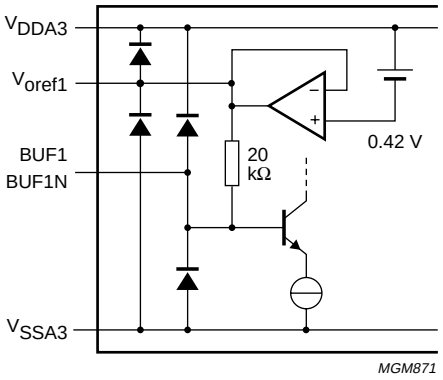


Fig.10 ADC1 buffer input and V_{oref1} output.

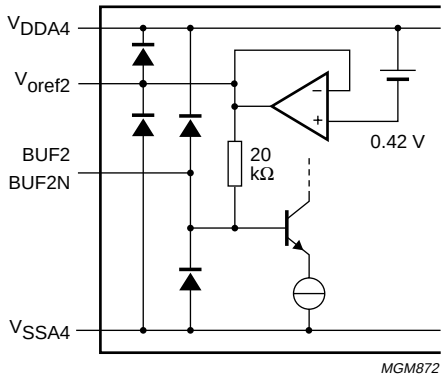


Fig.11 ADC2 buffer input and V_{oref2} output.

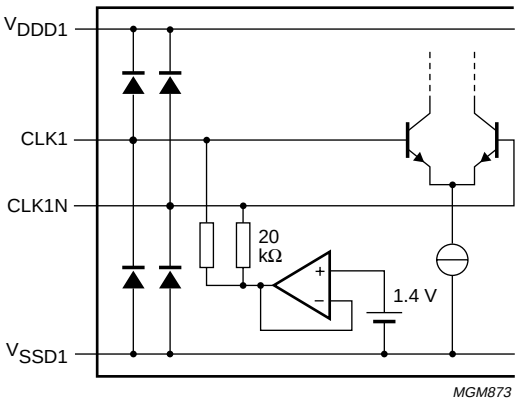


Fig.12 ADC1 clock buffer input.

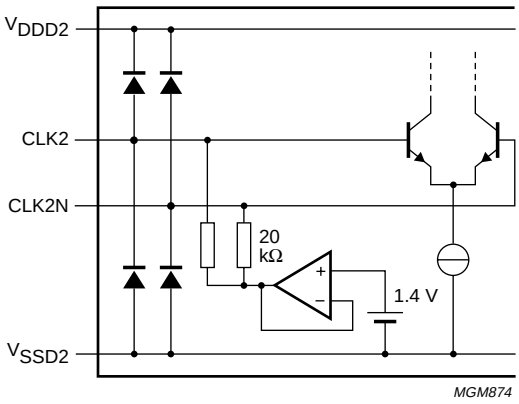


Fig.13 ADC2 clock buffer input.

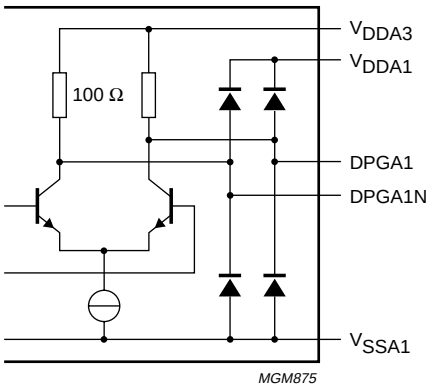


Fig.14 DPGA1 buffer output.

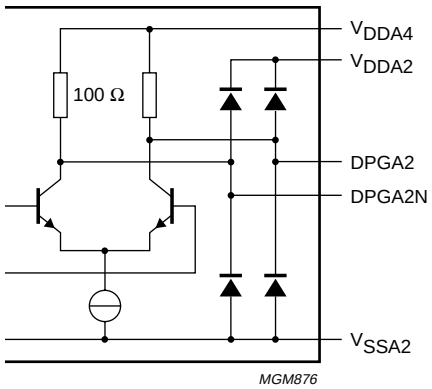


Fig.15 DPGA2 buffer output.

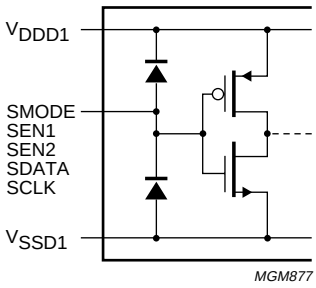


Fig.16 Serial Interface inputs.

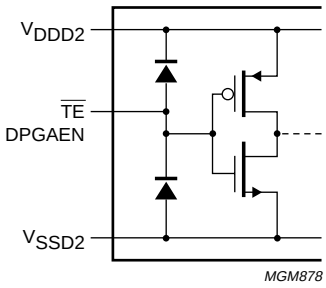


Fig.17 $\overline{TE}$ and DPGAEN inputs.

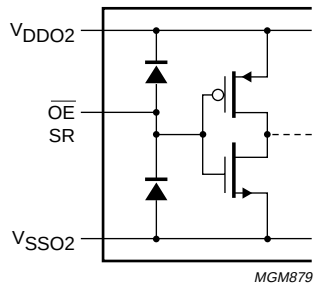


Fig.18 $\overline{OE}$ and SR inputs.

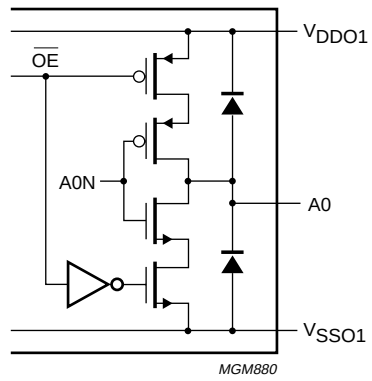


Fig.19 ADC1 A0 to A7 outputs.

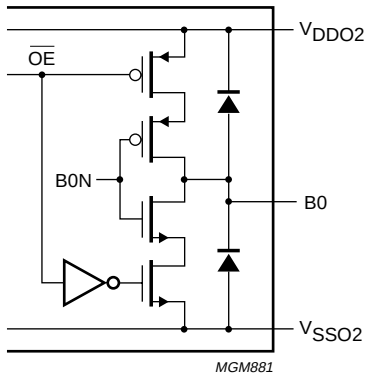


Fig.20 ADC2 B0 to B7 outputs.

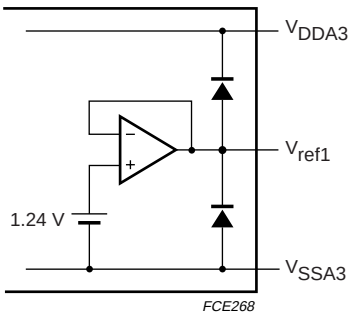


Fig.21 V_{ref1} output.

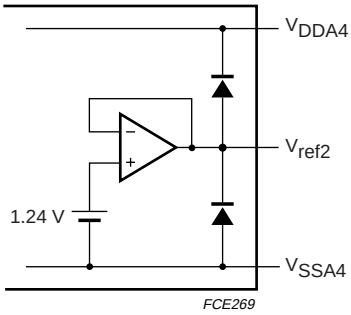
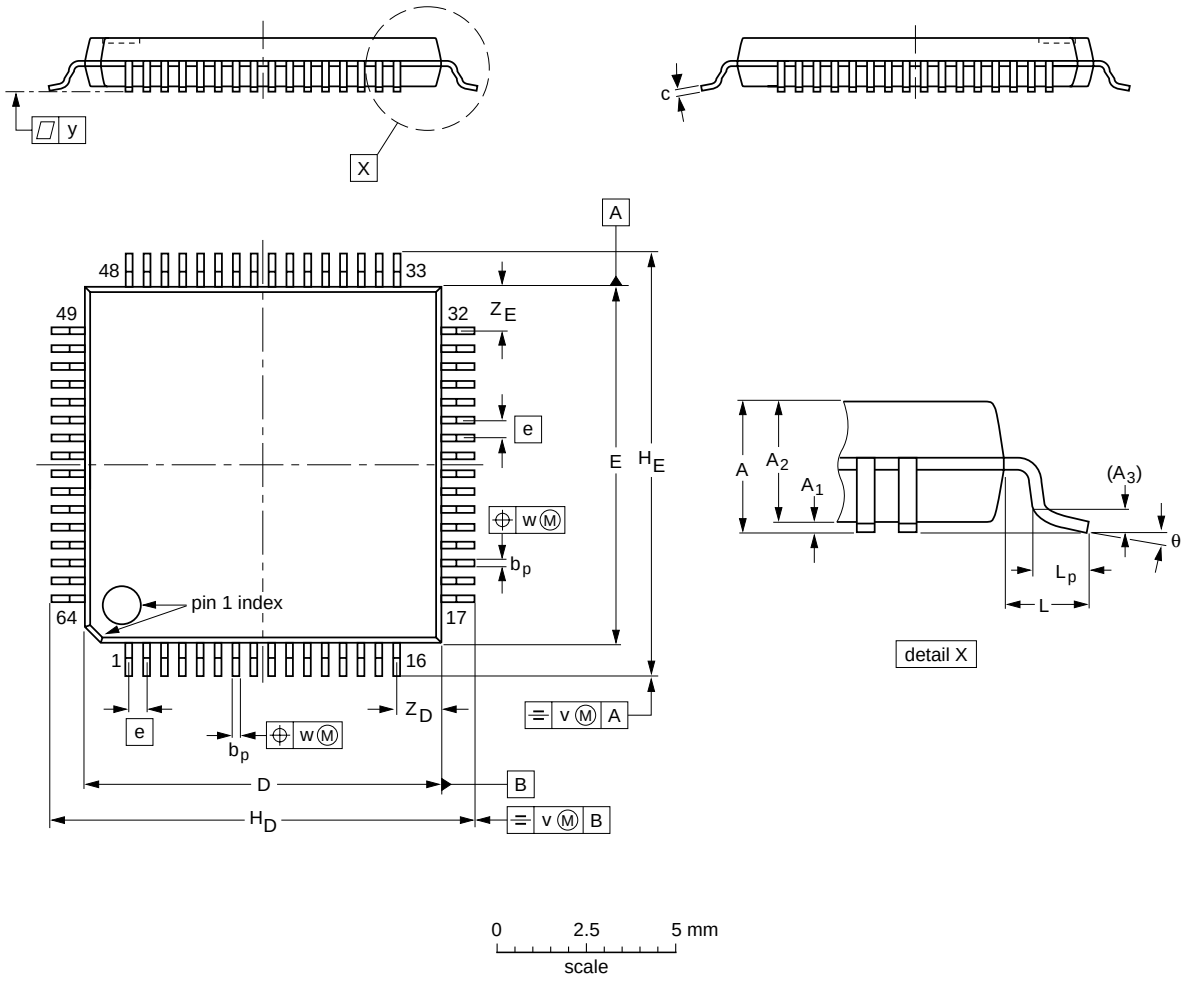


Fig.22 V_{ref2} output.

PACKAGE OUTLINE

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1.0	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT314-2						~~95-12-19~~ 97-08-01

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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