DATA SHEET

TDA8742; TDA8742H
Satellite sound circuit with noise reduction

Product specification
Supersedes data of November 1992
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Philips Semiconductors

PHILIPS

Satellite sound circuit with noise reduction TDA8742; TDA8742H

FEATURES

- Demodulation of main audio signal using wide band PLL (lock range selectable)
- HF input selection: two-out-of-eight secondary audio signals can be selected
- Demodulation of secondary audio signals using wide band PLL
- Noise reduction of the secondary audio signals
- Output selection: stereo, language 1, language 2, main audio and external
- Mute control
- Line outputs (SCART level).

APPLICATIONS

- Satellite receivers
- TV sets
- Video recorders.

GENERAL DESCRIPTION

The TDA8742; TDA8742H is a multi-function sound IC for use in satellite receivers, television sets and video recorders. The pin numbers given in parenthesis throughout this document refer to the QFP44 package.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		8	12	13.2	V
Main channel						
$V_{IN3(rms)}$	input sensitivity pin 18 (14) (RMS value)	S/N(A) = 40 dB	–	1.0	2.0	mV
Δf_{OM}	lock range PLL demodulator					
	either		5.5	–	7.5	MHz
	or		10.0	–	11.5	MHz
V_{OM}	output voltage pin 23 (19)		–9	–6	–4	dBV
S/N(A)	signal-to-noise ratio	A-weighted	62	70	–	dB
Secondary channels						
$V_{IN1,IN2(rms)}$	input sensitivity pins 2, 4, 6, 8, 10, 12, 14 and 16 (1, 3, 5, 7, 9, 11, 40 and 42) (RMS value)	S/N(A) = 40 dB	–	0.8	1.5	mV
$\Delta f_{OS1,2}$	lock range PLL demodulators		10.0	–	11.5	MHz
$V_{OR,OL}$	output voltage pins 24 and 25 (20 and 21)		–8	–6	–4	dBV
S/N(A)	signal-to-noise ratio	A-weighted	72	80	–	dB
Crosstalk						
$\alpha_{S/M}$	crosstalk from secondary to main channel		–	74	–	dB
$\alpha_{M/S}$	crosstalk from main to secondary channel		–	74	–	dB
$\alpha_{S/S}$	crosstalk between secondary channels		–	74	–	dB

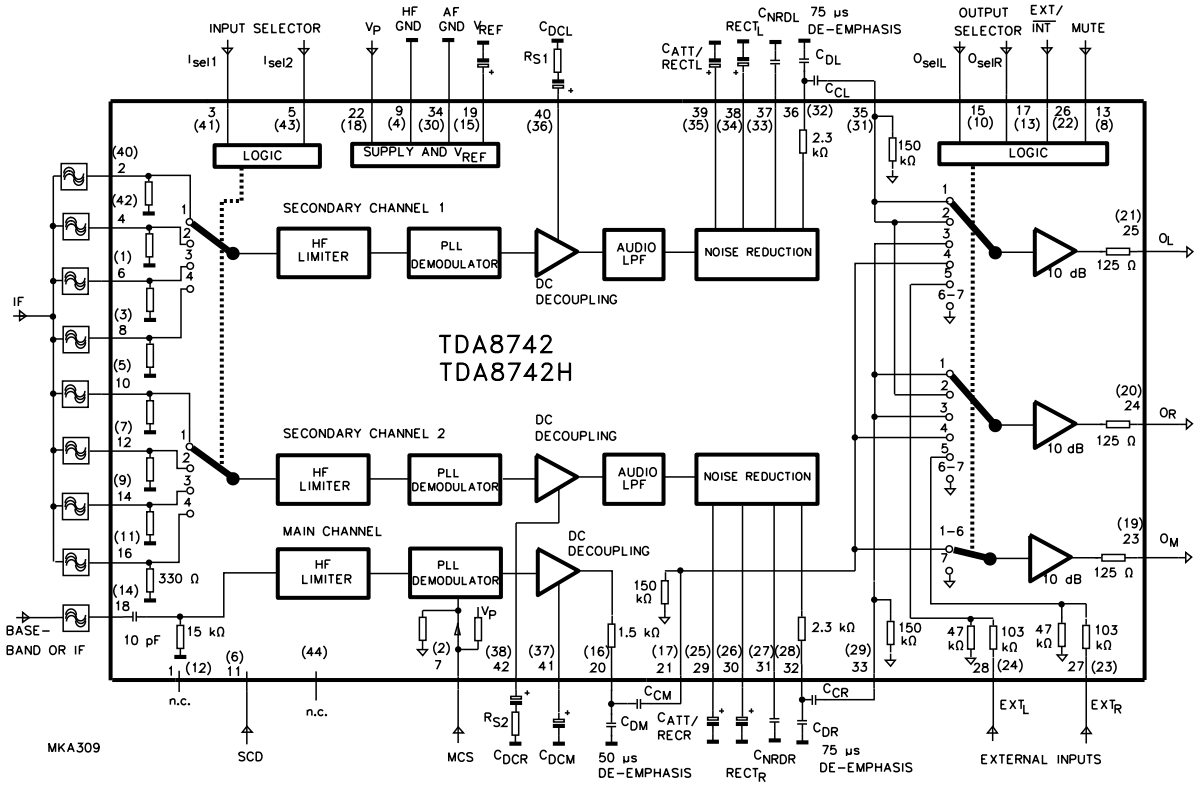
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8742	SDIP42	plastic shrink dual in-line package; 42 leads (600 mil)	SOT270-1
TDA8742H	QFP44[1]	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

Note

1. When using IR reflow soldering it is recommended that the Drypack instructions in the *"Quality Reference Handbook"* (order number 9398 510 63011) are followed.

BLOCK DIAGRAM



The pin numbers in parenthesis refer to the QFP44 package.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN SDIP42	PIN QFP44	DESCRIPTION
n.c.	1	39	not connected
IN-1A	2	40	intercarrier input A for Channel 1 (left)
$I_{sel\ 1}$	3	41	input select switch bit 1
IN-1B	4	42	intercarrier input B for Channel 1 (left)
$I_{sel\ 2}$	5	43	input select switch bit 2
IN-1C	6	1	intercarrier input C for Channel 1 (left)
MCS	7	2	main channel PLL lock-in range select/disable
IN-1D	8	3	intercarrier input D for Channel 1 (left)
HFGND	9	4	ground for HF section
IN-2A	10	5	intercarrier input A for Channel 2 (right)
SCD	11	6	secondary channels PLLs disable
IN-2B	12	7	intercarrier input B for Channel 2 (right)
MUTE	13	8	mute switch
IN-2C	14	9	intercarrier input C for Channel 2 (right)
$O_{sel\ L}$	15	10	output select switch bit 1 (left)
IN-2D	16	11	intercarrier input D for Channel 2 (right)
$O_{sel\ R}$	17	13	output select switch bit 2 (right)
IN-3	18	14	intercarrier input for main channel
V_{REF}	19	15	decoupling capacitor for reference voltage
$C_{D\ M}$	20	16	de-emphasis capacitor for main channel
$C_{C\ M}$	21	17	audio pass-through capacitor input for main channel
V_P	22	18	positive supply voltage
O_M	23	19	main channel output
O_R	24	20	right channel output
O_L	25	21	left channel output
EXT/$\overline{INT}$	26	22	output switch bit 3 (external/internal)
EXT_R	27	23	external audio input (right)
EXT_L	28	24	external audio input (left)
$C_{ATT/REC\ R}$	29	25	attack/recovery capacitor (right)
$RECT_R$	30	26	rectifier DC decoupling (right)
$C_{NR\ D\ R}$	31	27	noise reduction de-emphasis capacitor (right)
$C_{D\ R}$	32	28	fixed de-emphasis capacitor (right)
$C_{C\ R}$	33	29	audio pass-through capacitor input for right channel
AFGND	34	30	ground for AF section
$C_{C\ L}$	35	31	audio pass-through capacitor input for left channel
$C_{D\ L}$	36	32	fixed de-emphasis capacitor (left)
$C_{NR\ D\ L}$	37	33	noise reduction de-emphasis capacitor (left)
$RECT_L$	38	34	rectifier DC decoupling (left)
$C_{ATT/REC\ L}$	39	35	attack/recovery capacitor (left)

SYMBOL	PIN SDIP42	PIN QFP44	DESCRIPTION
$C_{DC\ L}$	40	36	DC decoupling capacitor (left)
$C_{DC\ M}$	41	37	DC decoupling capacitor (main)
$C_{DC\ R}$	42	38	DC decoupling capacitor (right)
n.c.	–	12	not connected
n.c.	–	44	not connected

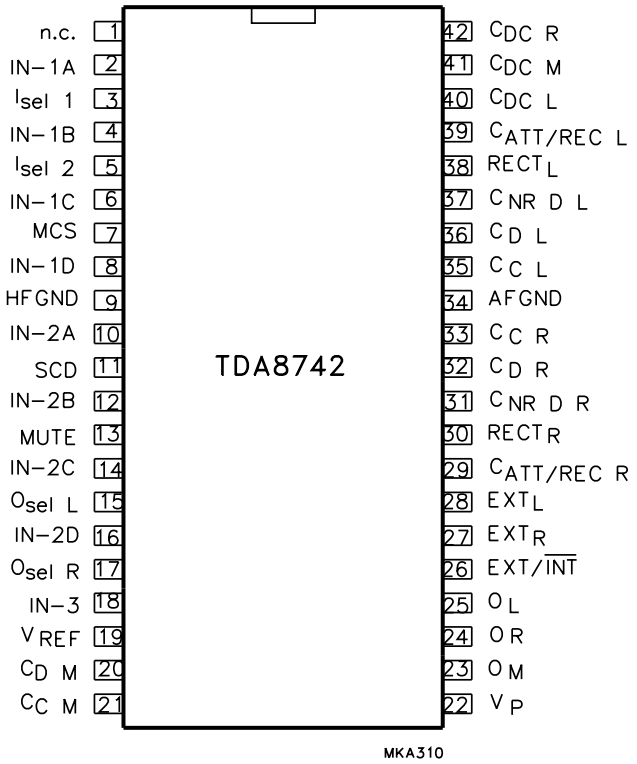


Fig.2 Pin configuration (SDIP42).

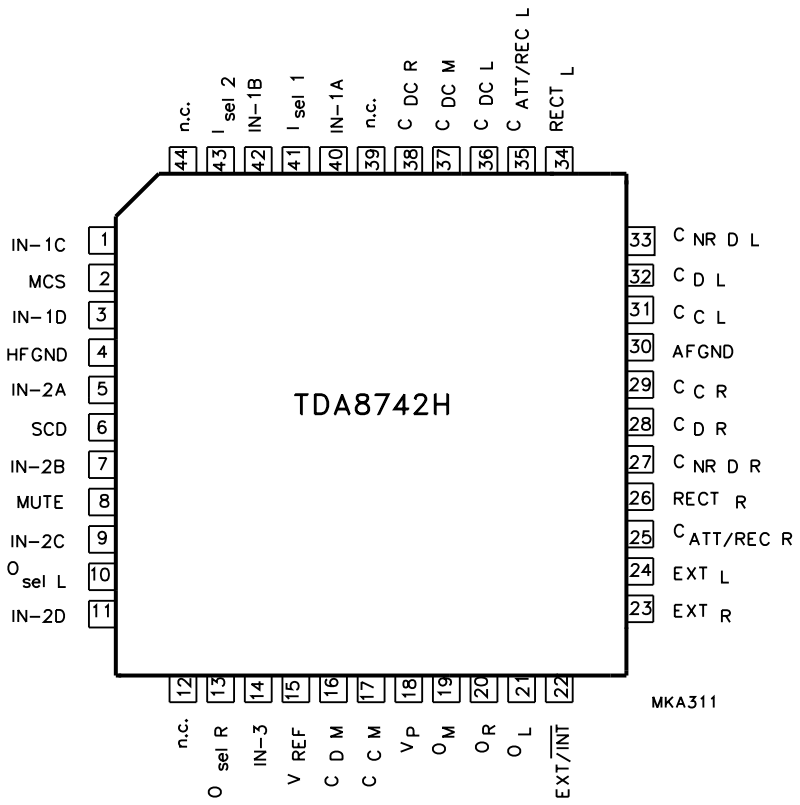


Fig.3 Pin configuration (QFP44).

FUNCTIONAL DESCRIPTION

Satellite sound

The baseband signal coming from a satellite tuner contains the demodulated video signal plus a number of sound carriers to facilitate reception of a PAL/NTSC/SECAM satellite signal.

Nearest to the video signal is the main sound carrier which carries the single channel sound related to the video. This is an FM modulated carrier with a fixed pre-emphasis. The carrier frequency can be in the range of 5.8 to 6.8 MHz.

Additionally, a number of optional secondary sound carriers may be present which can be used for stereo or multi-language sound related to the video, or for unrelated radio sound. These carriers are also FM modulated, but for better sound quality (improved signal-to-noise performance) broadcast satellites (e.g. 'ASTRA') use a noise reduction system (adaptive pre-emphasis circuit, combined with a fixed pre-emphasis).

These secondary carrier frequencies can be in the range of 6.30 to 8.28 MHz.

The TDA8742; H contains all circuitry for processing the main channel and for two secondary channels, from baseband signal to line (SCART) output drivers. The desired frequencies can be routed to the device via bandpass filters.

Main channel (see Fig.1)

The lock-in range of the main channel PLL can be switched between 5.5 to 7.5 MHz, PLL off and 10.0 to 11.5 MHz using the MCS signal at pin 7 (2) [when pin 7 (2) is at logic 0, being a voltage from 0 to 1.2 V, the lock-in range = 5.5 to 7.5 MHz; when pin 7 (2) is at logic 1, being a voltage from 3.5 V until V_P, the lock-in range = 10.0 to 11.5 MHz; when pin 7 (2) is in the mid voltage position, being a voltage from 1.8 to 2.8 V, the main channel PLL is switched off]. The voltage is then determined by the resistor divider at this pin between V_P and ground.

If only one fixed carrier frequency for the main channel is to be demodulated (e.g. 6.5 MHz), the lock-in range of the PLL should be switched to 5.5 to 7.5 MHz. The baseband signal is applied to the main channel input, pin 18 (14) via a 6.5 MHz ceramic bandpass filter. Alternatively, if there is a requirement to demodulate different main channel frequencies, these frequencies can be transferred to a fixed intermediate frequency (e.g. 10.7 MHz) using an external mixer and oscillator-frequency synthesizer. In this event the lock-in range of the PLL should be switched to 10.0 to 11.5 MHz. The IF signal is applied to the main channel input, pin 18 (14) via a 10.7 MHz ceramic bandpass filter.

The filtered signal is AC-coupled to a limiter/amplifier and then to a PLL demodulator. The PLL FM demodulator ensures that the demodulator is alignment-free. High gain and DC error signals from the PLL, which are superimposed on the demodulator output, require DC decoupling. A buffer amplifier is used to amplify the signal to the same level as the secondary channels and decouples DC using an electrolytic capacitor connected to pin 41 (37). The demodulator output signal is fed to pin 20 (16) via an internal resistor. The output signal can be de-emphasized by means of this resistor and an external capacitor connected to ground.

Capacitor value = de-emphasis time constant per1500 (for 50 μs: 33 nF).

From here the signal is fed to the output selectors. The signal is amplified to 500 mV (RMS) (i.e. −6 dBV) in the output amplifiers.

Secondary channels

Up to eight secondary channels are available at pins 2, 4, 6, 8, 10, 12, 14 and 16 (1, 3, 5, 7, 9, 11, 40 and 42). External ceramic bandpass filters, tuned to the required secondary sound carrier frequencies, route these signals to the inputs. This enables the demodulation of eight different channel; frequencies, which are derived from the baseband, by using an external mixer and oscillator frequency synthesizer.

For stereo applications the TDA8742; TDA8742H contains two identical secondary sound processing channels. For each channel it is possible to select from four inputs (IN-A, IN-B, IN-C and IN-D) using the input selector (see Table 1). With the input switch several stereo signals or languages can be selected for demodulation. It should be noted that the inputs are identical and can be freely interchanged Secondary Channel 1 will also be referred to as 'LEFT' or 'LANGUAGE 1' and secondary Channel 2 will also be referred to as 'RIGHT' or 'LANGUAGE 2'.

From the input selector switch the signals are coupled to limiter/amplifiers and then to the PLL demodulators. Processing is similar to the main channel. The demodulator output signal is amplified in a buffer amplifier and DC decoupled using electrolytic capacitors connected to pins 40 (36) (left) and 42 (38) (right). The output level is set with a 220 Ω resistor connected in series with the capacitor.

High frequency components in the amplified PLL output signal are filtered out in the audio LPF block (4th order Butterworth low-pass filter) to prevent unwanted influence on the noise reduction.

NOISE REDUCTION (NR)

The noise reduction can be regarded as an input level-dependent low-pass filter (adaptive de-emphasis system) followed by a fixed de-emphasis. With maximum input level (0 dB) the frequency response of the first part (i.e. without the fixed de-emphasis) is virtually flat. As the input level is lowered by x-dB, the higher output frequencies will be reduced an extra x-dB with respect to the lower frequencies (1 : 2 expansion).

The NR output signal is fed to pin 36 (32) (left) and pin 32 (28) (right) via an internal resistor.

Fixed de-emphasis is achieved by these resistors and external capacitors connected to ground. The signals are DC decoupled via pins 36/35 (32/31) and 32/33 (28/29) and then routed to the output selectors.

OUTPUT SELECTION

With the output selector (see Table 2) the outputs at pins 25 and 24 (21 and 20) can be switched to the different channels. Both outputs can be switched to both secondary channels, to the main channel and to the external inputs at pin 28 and 27 (24 and 23) for IC chaining purposes.

Pin 23 (19) is a separate output which delivers the main channel only, thereby creating the possibility of having three different output channels simultaneously e.g. for use in hi-fi VCRs.

The outputs at pins 25 and 24 (21 and 20) can be muted by setting the MUTE signal at pin 13 (8) to logic 1 (switch positions 6 and 7).

The output at pin 23(19) can be muted by setting the MUTE signal and the EXT/$\overline{\text{INT}}$ signal at pin 26 (22) both logic 1 (switch position 7).

All outputs at pins 23, 24 and 25 (19, 20 and 21) are line drivers with SCART level capability and are short-circuit protected by 125 Ω output resistors.

Output level of all channels = –6 dBV typical when frequency deviation of FM signal is 54% of maximum frequency deviation (i.e. 0.54×85 kHz = 46 kHz for the main channel and 0.54×50 kHz = 27 kHz for the secondary channels) at 1 kHz modulation frequency (reference level).

ABBREVIATIONS

f_{MOD} = modulating frequency.

Δf_M = frequency deviation of the main Channel.

Δf_{S1} = frequency deviation of secondary Channel 1 (left).

Δf_{S2} = frequency deviation of secondary Channel 2 (right).

f_{OM} = carrier frequency of main Channel.

f_{OS1} = carrier frequency of secondary Channel 1.

f_{OS2} = carrier frequency of secondary Channel 2.

LPF = Low-Pass Filter.

NR = Noise Reduction.

PLL = Phase-Locked-Loop.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage	note 1	0	13.2	V
V_n	voltage level on pins 2, 4, 6, 8, 10, 12, 14 and 16 (1, 3, 5, 7, 9, 11, 40 and 42)	note 2	0	1	V
V_n	voltage on pins 3, 5, 11, 13, 15, 17, 20, 21, 23 to 26, 31, 33, 35, 37, 40, 41, and 42 (6, 8, 10, 13, 16, 17, 19, 20 to 22, 27, 29, 31, 33, 36, 37, 38, 41 and 43)	note 2	0	9	V
V_n	voltage on pins 7, 18, 19, 27 to 30, 32, 36, 38 and 39 (2, 14, 15, 23 to 26, 28, 32, 34 and 35)	note 1	0	V_P	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–20	+70	°C

Notes

1. All voltages referenced to ground pins 9 and 34 (4 and 30).
2. All voltages referenced to ground pins 9 and 34 (4 and 30). These voltages must not exceed V_P or maximum value at any time.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SDIP42	53	K/W
	QFP44	69	K/W

DC CHARACTERISTICS

All voltages referenced to ground at pins 9 and 34 (4 and 30). Measured in test circuit Fig.4; V_P = 12 V; T_{amb} = 25 °C; $\Delta f_M = \Delta f_{S1} = \Delta f_{S2}$ = 0 kHz (no modulation); f_{OM} = 6.5 MHz; f_{OS1} = 10.52 MHz; f_{OS2} = 10.7 MHz; HF level at pin 18 (14): 40 mV (RMS); HF level at selected secondary inputs: 20 mV (RMS); MCS = logic 0 [V_7 (V_2) = 0 V]; SCD = logic 0 [V_{11} (V_6) = 0 V]; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	8.0	12	13.2	V
I_P	supply current	–	38	45	mA
P_{tot}	total power dissipation	–	–	600	mW
V_n	voltage on pins 20, 21, 23, 24, 25, 27, 28, 30, 32, 33, 35, 36 and 38 (16, 17, 19, 20, 21, 23, 24, 26, 28, 29, 31, 32 and 34)	–	3.8	–	V
V_{REF}	input reference voltage on pin 19 (15)	3.7	3.8	3.9	V
V_n	voltage on pins 2, 4, 6, 8, 10, 12, 14 and 16 (1, 3, 5, 7, 9, 11, 40 and 42)	–	0	–	V
$V_{CDCL,CDCR}$	voltage on pins 40 and 42 (36 and 38)	–	2.7	–	V
V_{CDCM}	voltage on pin 41 (37)	–	2.8	–	V
I_{IN3}	input current at pin 18 (14)	–	–	1	µA

AC CHARACTERISTICS

All voltages referenced to ground at pins 9 and 34 (4 and 30). Measured in test circuit Fig.4; V_P = 12 V; T_{amb} = 25 °C; f_{MOD} = 1 kHz; f_{OM} = 6.5 MHz; Δf_M = 46 kHz; $\Delta f_{S1} = \Delta f_{S2}$ = 27 kHz (reference levels); f_{OS1} = 10.52 MHz; f_{OS2} = 10.7 MHz; HF level at pin 18 (14): 40 mV (RMS); HF level at selected secondary inputs: 20 mV (RMS); MCS = logic 0 [V_7 (V_2) = 0 V]; SCD = logic 0 [V_{11} (V_6) = 0 V]; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Main channel - HF input pin 18 (14) and limiter						
$V_{IN3(rms)}$	input sensitivity (RMS value)	S/N(A) = 40 dB	–	1.0	2.0	mV
$V_{IN3(rms)}$	input signal level (RMS value)		–	–	200	mV
R_{IN3}	input resistance		–	15	–	kΩ
Main channel - PLL FM demodulator and DC decoupling amplifier						
f_{CCO}	free-running frequency		–	6.5	–	MHz
		MCS = logic 1	–	10.7	–	MHz
Δf_{OM}	lock range of PLL	note 1	5.5	–	7.5	MHz
		MCS = logic 1; note 1	10.0	–	11.5	MHz
R_{CDM}	output resistance for 50 µs de-emphasis pin 20 (16)		1.24	1.5	1.7	kΩ
V_{CDM}	output voltage pin 20 (16)		–18.5	–16.0	–14.5	dBV
ΔV_{CDM}	spread of PLL output voltage over lock range pin 20 (16)		–	–	±1	dB
R_{CCM}	input resistance of output amplifier pin 21 (17)		95	150	200	kΩ
Main channel - overall performance (output selector in position 4)						
$V_{OM,OR,OL}$	output voltage pins 23, 24 and 25 (19, 20 and 21)	all PLLs locked	–9	–6	–4	dBV
UBM	unbalance voltage outputs pins 23 to 25 (19 to 21)	output selector in position 4	–0.5	–	+0.5	dB
THD	total harmonic distortion	all PLLs locked	–	0.1	0.5	%
S/N(A)	signal-to-noise ratio	A-weighted; all PLLs locked	62	70	–	dB
$\frac{V_{OM\,(15\ kHz)}}{V_{OM\,(1\ kHz)}}$	15 kHz frequency response with respect to 1 kHz pin 23 (19)	no de-emphasis connected	–0.5	0	+0.5	dB
$R_{OM,OR,OL}$	output resistance pins 23, 24 and 25 (19, 20 and 21)		92	125	150	Ω
$\alpha_{S/M}$	crosstalk attenuation from secondary channels to main	note 2	–	74	–	dB
$MUTE_{att}$	mute attenuation	output selector in position 7	74	–	–	dB
SVRR	supply voltage ripple rejection	V_{RR} = 100 mV; f_i = 70 Hz	–	35	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Secondary channels 1 and 2 - HF inputs pins 2, 4, 6, 8, 10, 12, 14 and 16 (1, 3, 5, 7, 9, 11, 40 and 42) and limiters						
$V_{IN1,IN2(rms)}$	input sensitivity (RMS value)	S/N(A) = 40 dB	–	0.8	1.5	mV
$V_{i(rms)}$	input signal level (RMS value)		–	–	200	mV
R_i	input resistance		260	330	380	Ω
Secondary channels 1 and 2 - PLL FM demodulators (input selector in position 1)						
f_{CCO1}	free running frequency PLL1		–	10.7	–	MHz
f_{CCO2}	free running frequency PLL2		–	10.52	–	MHz
$\Delta f_{OS1/2}$	lock range of PLLs	note 3	10	–	11.5	MHz
$R_{S1, S2}$	series resistance for optimum frequency response adjustment		0	0.68	2.2	kΩ
$V_{CDCL,CDCR(rms)}$	PLL output voltage pins 40 and 42 (36 and 38) (RMS value)	pins to be left open-circuit	–	9	–	mV
$\Delta V_{CDCL,CDCR}$	spread of PLL output voltage over lock range		–	–	±1	dB
Secondary channels - overall performance of LPF and NR (output selectors in position 1)						
R_o	output resistance for 75 μs de-emphasis pins 36 and 32 (32 and 28)		1.9	2.3	2.6	kΩ
R_i	input resistance of output amplifiers pins 35 and 33 (31 and 29)		95	150	200	kΩ
$V_{OL,OR}$	output voltage level pins 25 and 24 (21 and 20)	note 4	–8	–6	–4	dBV
UBS	unbalance voltage outputs pins 25 and 24 (21 and 20)	note 4	–1	–	+1	dB
THD	total harmonic distortion	note 4	–	0.1	0.5	%
S/N(A)	signal-to-noise ratio	A-weighted; note 4	72	80	–	dB
R_o	output resistance pins 25 and 24 (21 and 20)	note 4	92	125	150	Ω
$MUTE_{att}$	mute attenuation	output selector in position 6; note 4	74	–	–	dB
$\alpha_{S/S}$	crosstalk attenuation between secondary channels	note 5	–	74	–	dB
$\alpha_{M/S}$	crosstalk attenuation from main channel to secondary	note 6	–	74	–	dB
$V_{offset(DC)}$	DC offset voltage on attack/recovery capacitors pins 29, 39 (25, 35)	all PLLs locked; $\Delta f = 0$	14	16	20	mV
SVRR	supply voltage ripple rejection	V_{RR} = 100 mV; f_i = 70 Hz	–	25	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Secondary channels - low-pass filter pins 38 and 30 (34 and 26)						
$\frac{V_{RECTL, RECTR\,(50\ kHz)}}{V_{RECTL, RECTR\,(1\ kHz)}}$	50 kHz frequency response with respect to 1 kHz	note 7	–25	–16	–9	dB
Secondary channels - noise reduction pins 25 and 24 (21 and 20); note 4						
$V_{OL, OR}$	output voltage at 0 dB noise reduction input level	$\Delta f_{S1} = \Delta f_{S2} = 50$ kHz; no fixed de-emphasis connected	–1	+1	+3	dBV
$\frac{V_{OL, OR\,(15\ kHz)}}{V_{OL, OR\,(1\ kHz)}}$	15 kHz frequency response with respect to 1 kHz at 0 dB noise reduction input level	$\Delta f_{S1} = \Delta f_{S2} = 50$ kHz; no fixed de-emphasis connected	–2	0	+2	dB
$V_{OL,OR}$	output voltage at –20 dB noise reduction input level	$\Delta f_{S1} = \Delta f_{S2} = 5$ kHz; no fixed de-emphasis connected	–29	–26	–23	dBV
$\frac{V_{OL, OR\,(15\ kHz)}}{V_{OL, OR\,(1\ kHz)}}$	15 kHz frequency response with respect to 1 kHz at –20 dB noise reduction input level	$\Delta f_{S1} = \Delta f_{S2} = 5$ kHz; no fixed de-emphasis connected	–13	–11.5	–10	dB
External inputs - pin 28 (24) (left) and pin 27 (23) (right) - overall performance (output selector in position 5)						
$V_{EXTR,EXTL}$	input signal level		–	–	6	dBV
R_i	input resistance		95	150	200	kΩ
$V_{OL,OR}$	output level	$V_{EXTR, EXTL} = -6$ dBV	–6.5	–6.0	–5.5	dBV
THD	total harmonic distortion	$V_{EXTR, EXTL} = -6$ dBV; $f_i = 1$ kHz	–	–	0.1	%
S/N(A)	signal-to-noise ratio	A-weighted; $V_{EXTR, EXTL} = -6$ dBV	80	–	–	dB
$\alpha_{L/R}, \alpha_{R/L}$	crosstalk	$f_i = 1$ kHz	–	80	–	dB
Input selector control circuit pins 3 and 5 (41 and 43) (see also Table 1) and secondary channels PLLs disable [SCD pin 11 (6)]; pin 11 (6); pins left open-circuit = logic HIGH						
V_{IL}	LOW level input voltage		0	–	1.2	V
V_{IH}	HIGH level input voltage		3.5	–	9	V
R_i	input resistance	connected to V_P	65	100	130	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output selector control circuit (see also Table 2) and main channel PLL lock-in select [MCS pin 7 (2)]; pins 15, 17, 26, 13 and 7 (10, 13, 22, 8 and 2) MOS inputs and should not be left open-circuit						
V_{IL}	LOW level input voltage limits		0	–	1.2	V
V_{IM}	MID level input voltage limits for MCS pin only		1.8	–	2.8	V
V_{IMF}	MID level input voltage on MCS pin if MCS pin is floating	V_P must be 1.8 to 13.2 V	17	19	21	$\%V_P$
V_{IH}	HIGH level input voltage limits		3.5	–	V_P	V
R_{IL}	low input resistance MCS pin to ground		12	19	26	kΩ
R_{IH}	high input resistance MCS pin to V_P		52	80	108	kΩ
I_{IL}	LOW level input current (not MCS pin)	V_{IL} = 0 V	–	<–1	–	μA
I_{IH}	HIGH level input current (not MCS pin)	V_{IH} = 5 V	–	<1	–	μA

Notes

1. At pin 20 (16) the demodulated 1 kHz signal should be present with a typical level of 158 mV (RMS) (–16 dBV), and THD of maximum 0.5%; V_P = 8 to 3.2 V; T_{amb} = –20 to +70 °C.
2. Modulation of main channel is OFF; modulation of secondary channels is ON.
3. The electrolytic capacitors at pins 40 and 42 (36 and 38) are removed and 1500 pF capacitors between pin 40 (36) and ground and between pin 42 (38) and ground are connected. At pins 40 and 42 (36 and 38) the demodulated 1 kHz signals should be present with typical levels of 9 mV (RMS) and THD of maximum 0.5%; V_P = 8 to 3.2 V; T_{amb} = –20 to +70 °C.
4. All PLLs locked; $R_{S1} = R_{S2}$ = 0.68 kΩ.
5. Modulation of secondary channel being measured and main channel is OFF; modulation of other secondary channel is ON.
6. Modulation of main channel is ON; modulation of secondary channels is OFF.
7. Measured at pins 38 (34) (left) and 30 (26) (right) and no electrolytic capacitors connected to these pins.

Table 1 Truth table for input selection

SWITCH POSITION	STATE	PIN 3 (41)	PIN 5 (43)
1	pins 2 and 10; IN-A (pins 40 and 5)	0	0
2	pins 4 and 12; IN-B (pins 42 and 7)	0	1
3	pins 6 and 14; IN-C (pins 1 and 9)	1	0
4	pins 8 and 16; IN-D (pins 3 and 12	1	1

Table 2 Truth table for output selection (note 1)

SWITCH POSITION	STATE	PIN 15 (10)	PIN 17 (13)	PIN 26 (22)	PIN 13 (8)
		OUTSEL L	OUTSEL R	EXT/$\overline{\text{INT}}$	MUTE
1	stereo	1	1	0	0
2	left	1	0	0	0
3	right	0	1	0	0
4	main	0	0	0	0
5	external	X	X	1	0
6	mute secondary	X	X	0	1
7	mute all	X	X	1	1

Note

1. X = don’t care.

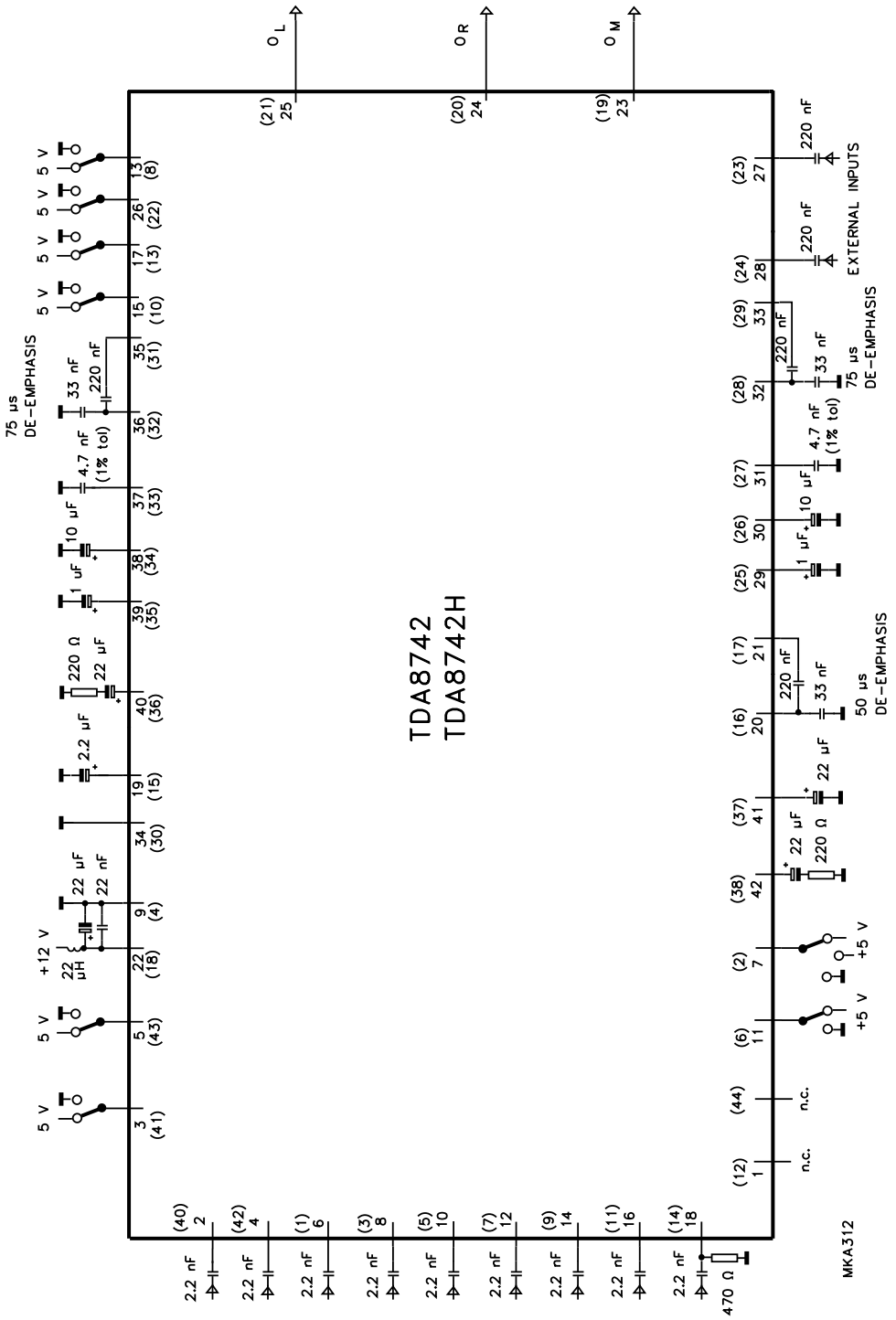


Fig.4 Test circuit.

The pin numbers in parenthesis refer to the QFP44 package.

APPLICATION INFORMATION

General

This application is mainly intended to have more than two inputs for secondary channel available. In this event a choice between the same frequency sets e.g. 10.7 and 10.52 MHz but with different bandwidths is possible. A narrow bandwidth can be chosen in the event of a weak signal, however this produces slightly more distortion. A normal signal will be processed using 150 kHz filters thus resulting in a signal with normal distortion. For the main channel either baseband or synthesized signal can be selected. The circuit is illustrated in Fig.5.

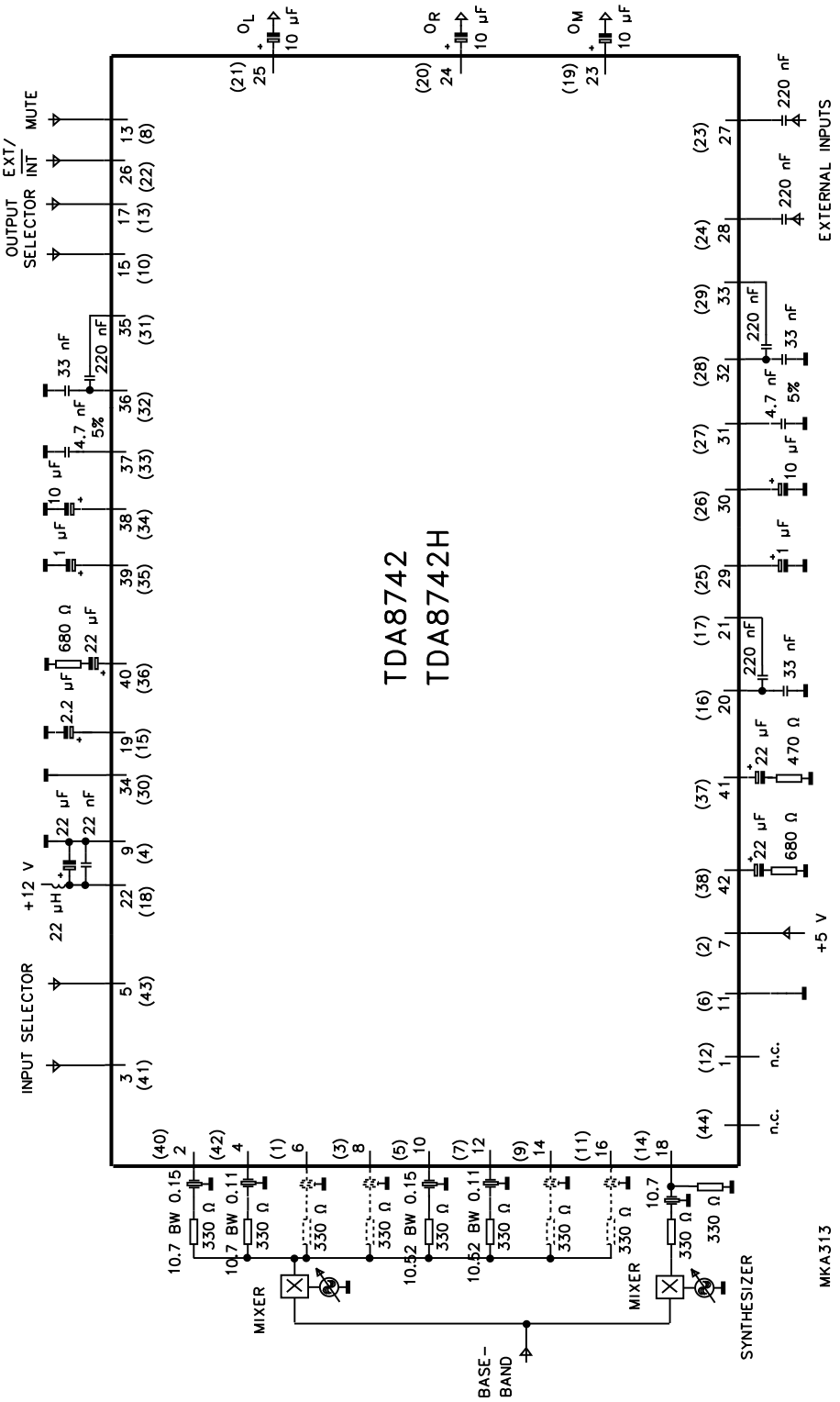
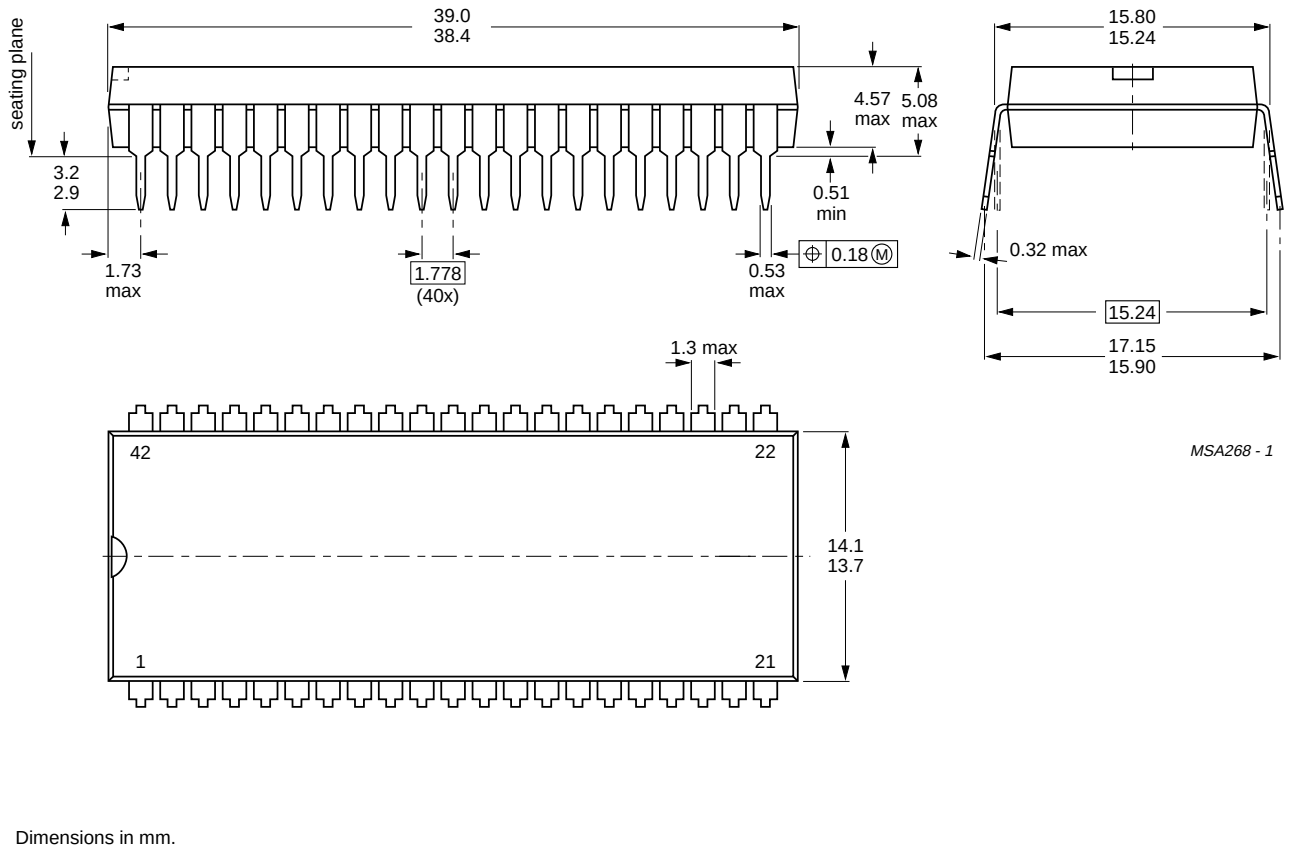


Fig.5 Application diagram.

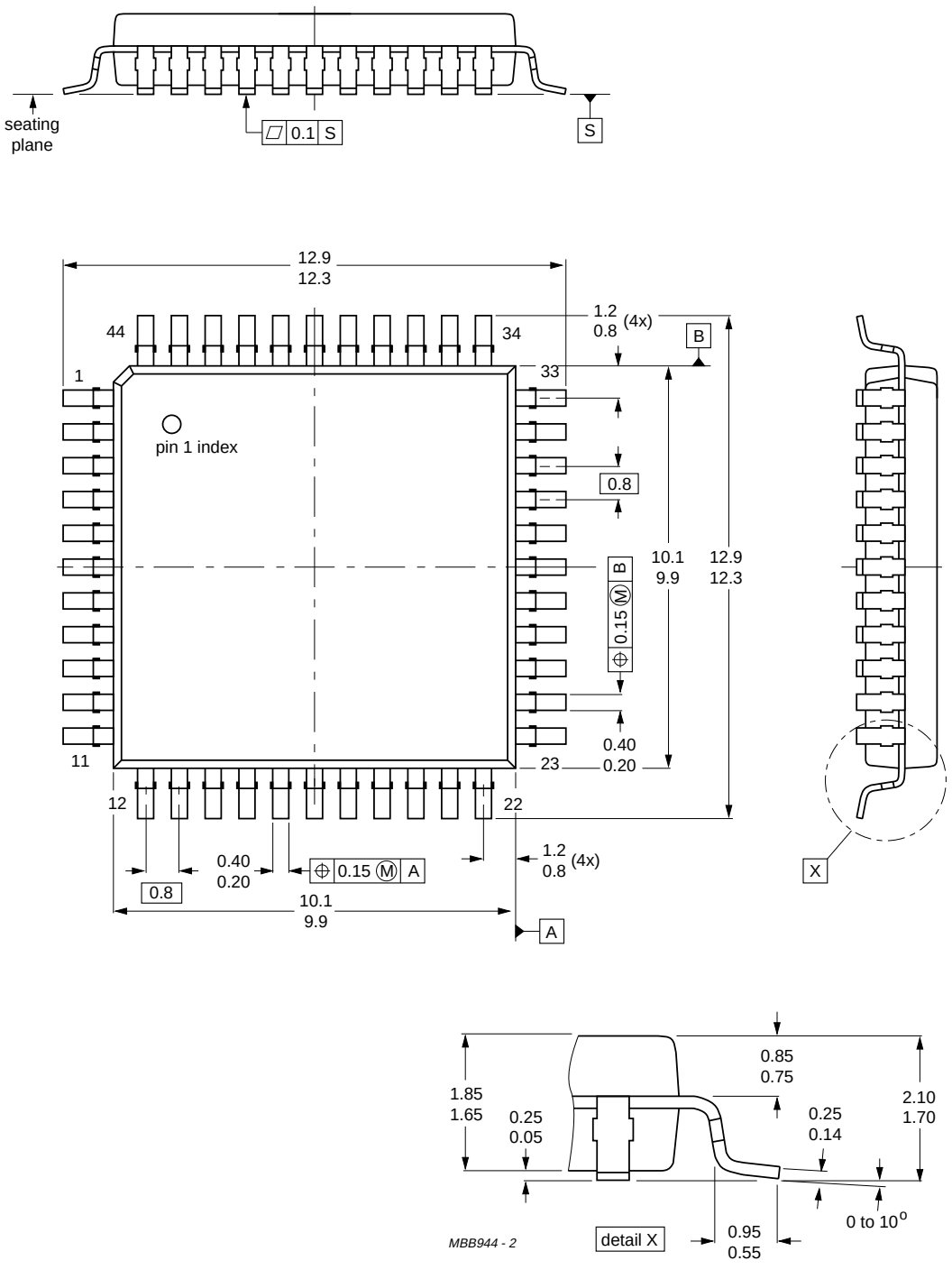
The pin numbers in parenthesis refer to the QFP44 package.

PACKAGE OUTLINES



Dimensions in mm.

Fig.6 Plastic shrink dual in-line package; 42 leads (600 mil); SDIP42; SOT270-1.



Dimensions in mm.

Fig.7 Plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm (QFP44; SOT307-2).

SOLDERING

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

Plastic quad flat packages

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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