DEVICE SPECIFICATION

TDA8359J

Full bridge vertical deflection output circuit in LVDMOS

Prelimenary specification

March 24, 1999

Philips
Semiconductors

PHILIPS

Full bridge vertical deflection output circuit in LVDMOS

TDA8359J

FEATURES

- Few external components
- Highly efficient fully DC-coupled vertical output bridge circuit
- Short rise and fall time of the vertical flyback switch
- Guard circuit built-in
- Temperature (thermal) protection
- Excellent EMC performance because of common mode inputs

GENERAL DESCRIPTION

The TDA8359J is a power circuit for use in 90° and 110° colour deflection systems for field frequencies of 25 to 200 Hz and 16 : 9 picture tubes. The IC contains a vertical deflection output circuit, operating as a highly efficient class G system. The full bridge output circuit enables DC coupling of the deflection coil with a single main supply.

The IC is constructed in a Low Voltage DMOS process that combines Bipolar, CMOS and DMOS devices. MOS transistors are used in the output stage due to the absence of second breakdown.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC supply						
V_p	supply voltage		7.5	12	18	V
$I_{pq(av.)}$	average quiescent supply current	during scan	–	10	15	mA
V_{flb}	flyback supply voltage		2 x V_p	45	68	V
$I_{flb(av.)}$	average flyback supply current	during scan	–	–	10	mA
P_{total}	total power dissipation				8	W
Vertical circuit						
$I_{o(p-p)}$	output current (peak to peak)		–	–	3.2	A
$V_{i(diff)(p-p)}$	input voltage (peak to peak) pin 1 or pin 2		–	1000	1500	mV
Flyback switch						
$I_{o(flb)}$	peak output current	$t \leq 1.5$ ms	–	–	±1.8	A
Thermal data (in accordance with IEC 747-1)						
T_{stg}	storage temperature		−55	–	+150	°C
T_{amb}	operating ambient temperature		−25	–	+75	°C
T_{vj}	virtual junction temperature		–	–	+150	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8359J	DBS9	plastic DIL-bent-SIL power package; 9 leads	SOT523-1

BLOCK DIAGRAM

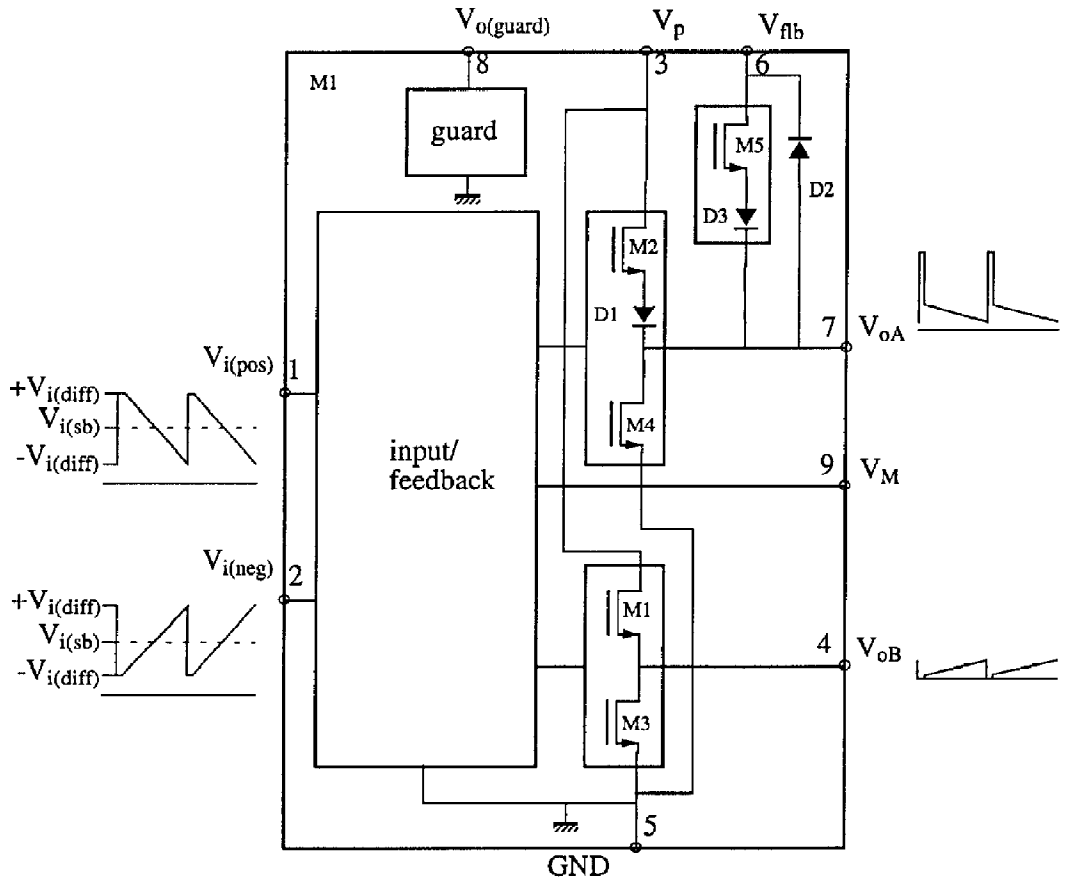
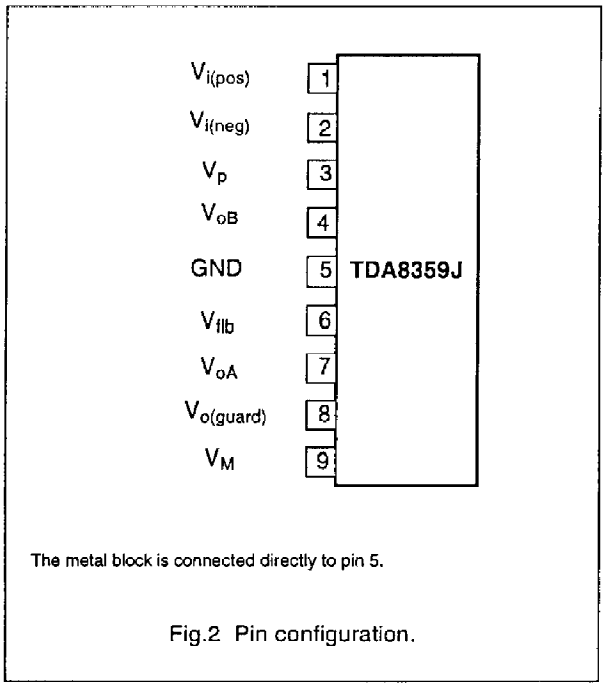


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{i(pos)}$	1	input voltage (positive);
$V_{i(neg)}$	2	input voltage (negative);
V_p	3	supply voltage
V_{oB}	4	output voltage B
GND	5	ground
V_{flb}	6	flyback supply voltage
V_{oA}	7	output voltage A
$V_{o(guard)}$	8	guard output voltage
V_M	9	input measuring resistor



The metal block is connected directly to pin 5.

Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

VERTICAL OUTPUT STAGE

The vertical driver circuit is a bridge configuration. The deflection coil is connected between the output amplifiers, which are driven in phase opposition. The differential input circuit is voltage driven. The input circuit is specially intended for direct connection to driver circuits which deliver symmetrical current signals, but is also suitable for asymmetrical currents. The output current of these devices is converted to voltages at the input pins via resistors R_{CV1} and R_{CV2}.The differential input voltage is compared with the voltage across R_M, which provides internal feedback information. The voltage across R_M is proportional to the output current. The relationship between the differential input current and the output current is defined by:

$$2 \times I_{i(diff)(p\text{-}p)} \times R_{CV1,2} = I_{coil(p\text{-}p)} \times R_M.$$

The output current is adjustable from 0.5 A (p-p) to 3.2 A (p-p) by varying $R_{CV1,2}$ or R_M. The maximum input voltage is 1.6V peak for each pin. The minimum input voltage is 100 mV. The formula given has no correction for the internal bondwire resistance (R_{bo}). Depending on the value of R_M and R_{bo} (typical 50 mΩ) the value of the actual current in the deflection coil will be about 5% lower than calculated.

FLYBACK SUPPLY

The flyback voltage is determined by an additional supply voltage V_{flb}. The principle of operating with two supply voltages (class G) makes it possible to fix the supply voltage V_p optimum for the scan voltage and the second supply voltage V_{flb} optimum for the flyback voltage. Using this method, very high efficiency is achieved. The supply voltage V_{flb} is almost totally available as flyback voltage across the coil, this being possible due to the absence of a coupling capacitor (not necessary, due to the bridge configuration). The very short rise and fall time of the flyback switch is determined by a slew-rate of more than 300V/µsec.

PROTECTION

The output circuit has protection circuits for:

- too high die temperature
- overvoltage of output stage A

GUARD CIRCUIT

A guard circuit with output signal $V_{o(guard)}$ is provided.

The guard circuit generates an active high level during the flyback period. The guard circuit is also activated for one or more of the following conditions:

- when the thermal protection is activated. (Tj = ~ 170°C)
- during open loop

The guard signal can be used for blanking the picture tube screen and signalling a fault condition.

The guard signal can also be used to supply vertical sync pulses to the microcontroller for On Screen Display.

DAMPING RESISTOR COMPENSATION

For HF loop stability a damping resistor is connected across the deflection coil. There is a big difference in current in the damping resistor R_p during scan and flyback. The resistor current is summed to the current in the deflection coil via the measuring resistor R_M, which results in a too low current in the deflection coil at the start of the scan.

The difference in the current value in the damping resistor during scan and flyback period can be compensated for by external means. This to achieve a short settling time. To do so a resistor (R_{comp}) in series with a zener diode can be connected between the output of the A-stage (pin 7) and pin 1($V_{i(pos)}$). The zener diode value should be equal to the supply voltage. The value of R_{comp} is calculated by:

$$R_{comp} = \frac{(V_{flb} - V_{loss} - V_p) \times R_p \times R_{CV1}}{(V_{flb} - V_{loss} - I_{coil\,(peak)} \times R_L) \times R_M}$$

Where V_{loss} is the voltage loss between pin 6 and 7 during flyback. R_L is the coil resistance.

INTERNAL CIRCUIT CONFIGURATION

The internal circuit configuration at each pin is given in fig.3.

HEATSINK CALCULATION

The value of the heatsink can be calculated in the standard way. This method bases on average temperatures. The value of the heatsink should be chosen such that the die temperature does not exceed the maximum specification value of 150°C. **In general we recommend to design for an average die temperature not exceeding 130°C**

EXAMPLE

Measured or given values:

$P_{VERT\,total}$ = 6W

$T_{ambient}$ max. = 40°C

T_{vj}= 130°C

$R_{THvj\text{-}case}$ = 5K/W

$R_{THcase\text{-}heatsink}$ =2K/W

The heatsink value is now given by:

$$R_{TH} = \frac{T_{vj} - T_{ambient}}{P_{VERT}} - (R_{THvj-case} + R_{THcase-heatsink})$$

When we use the values of the example we find:

$$R_{TH} = \frac{130 - 40}{6} - (5 + 2) = 8K/W$$

The heatsink temperature will be:

$T_{heatsink} = T_{ambient} + R_{TH} \times P_{total} = 40 + 6 \times 8 = 88°C$

SUPPLY VOLTAGE CALCULATION

To calculate the minimum required supply voltage, distinct values from the application have to be known. These values are the required coil peak current, the coil impedance and the measuring resistor. The coil peak current should include overscan.

For calculations the coil resistance is multiplied by 1.2 to correct for hot conditions.

The voltage loss given by the vertical output stage can be taken from the device characterics (see page 9). For the first part of the scan the voltage loss is given by V_{loss1} (3-7) plus (4-5). For the second part of the scan the voltage loss is given by V_{loss2} (3-4) plus (7-5).

The voltage drop across the coil during scan is given by the ohmic part and the inductance part. For the first part of the scan the inductance part subtracts from the ohmic part while for the second part of the scan the inductance part adds to the ohmic part. For calculations the highest vertical frequency should be taken.

First part of the scan

$V_{s1} = I_{defl\ peak} \times R_{total} - L_y \times 2 \times I_{defl\ peak} \times f_{Vmax} + V_{loss1}$

Second part of the scan

$V_{s2} = I_{defl\ peak} \times R_{total} + L_y \times 2\ I_{defl\ peak} \times f_{Vmax} + V_{loss2}$

The required supply voltage V_p is given by the highest values of V_{s1} or V_{s2}

FLYBACK SUPPLY VOLTAGE CALCULATION

In most cases the flyback supply voltage needed for a required flyback time can be calculated by a simplified formula:

$$V_{flb} = I_{coilpp} \times \frac{R_{total}}{1 - e^{-(t/x)}}$$

Where

$$x = \frac{L_Y}{R_{total}}$$

The flyback supply voltage value calculated in this way is about 5 to10% higher than required.

CALCULATION OF THE POWER DISSIPATION OF THE VERTICAL OUTPUT STAGE

The power dissipation in the IC is given by the formula:

$$P_{tot} = V_P \times \frac{I_{defl(peak)}}{2} + V_P \times 0.015A + 0.3W$$

In this formula 0.3W is taken as an average value for the losses in the flyback supply.

The average power dissipation in the external load (coil and measuring resistor) is given by the formula:

$$P_{load} = \frac{(I_{deflpeak})^2}{3} \times R_{total}$$

The power dissipation in the IC is given by the formula:

$$P_{IC} = P_{tot} - P_{load}$$

EXAMPLE

SYMBOL	VALUE	UNIT
Values given from the application		
$I_{deflpeak}$	1.2	A
I_{coilpp}	2.4	A
L_y	5	mH
R_L	6	Ω
R_M	0.6	Ω
f_{Vmax}	50	Hz
$t_{flyback}$	640	µs

SYMBOL	VALUE	UNIT
V_p	14	V
$R_{total\ (hot)}$	7.8	Ω
t	0.02	s
x	0.000641	
V_{flb}	30	V
P_{total}	8.91	W
P_{load}	3.74	W
P_{IC}	5.17	W

INTERNAL CIRCUIT CONFIGURATION.

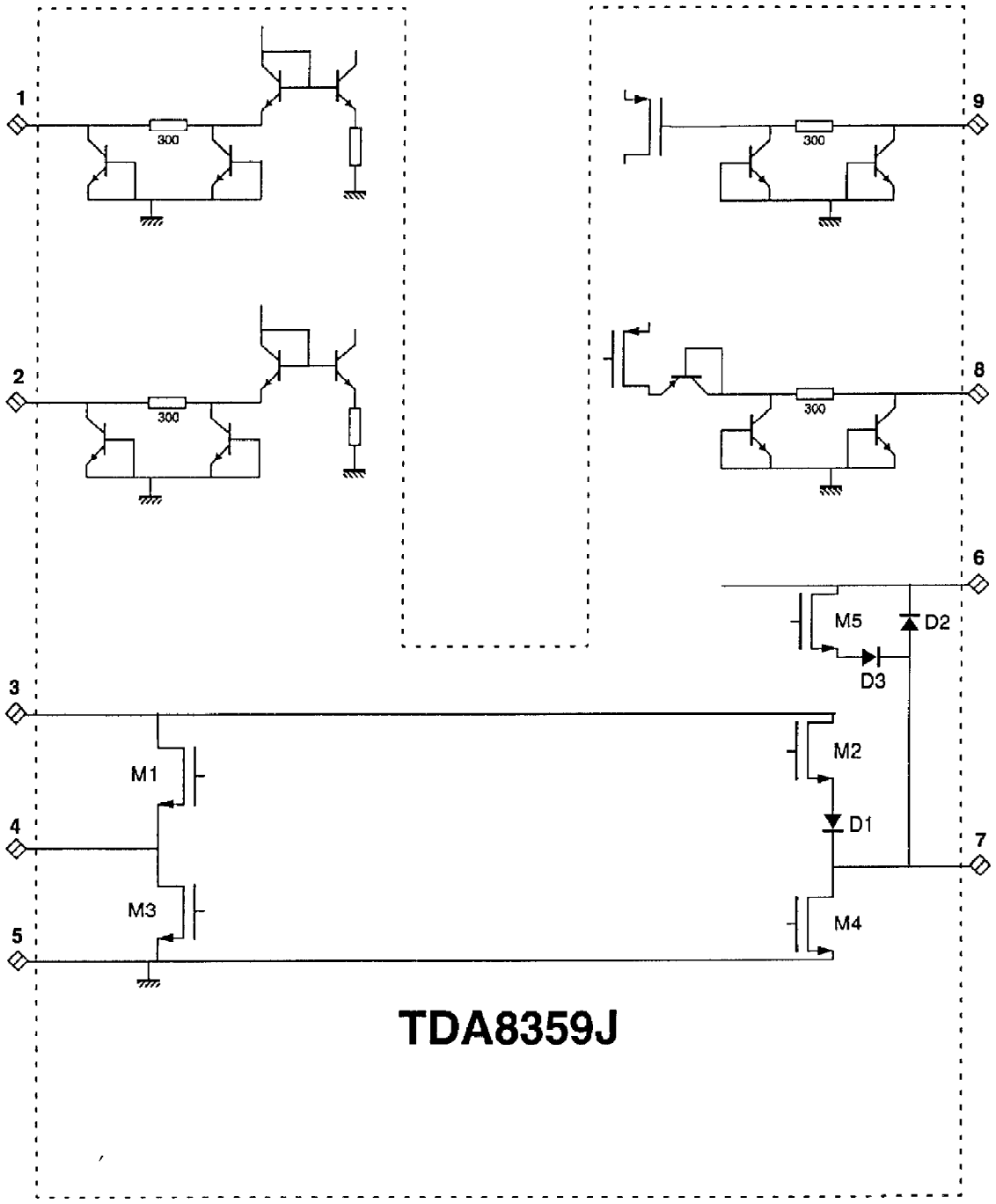


Fig.3 Internal circuit configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
DC supply					
V_p	supply voltage		–	18	V
V_{flb}	flyback supply voltage		–	68	V
P_{total}	total power dissipation			8	W
Vertical circuit					
$I_{o(p-p)}$	output current (peak-to-peak value)		–	3.2	A
V_{oA}	output voltage (pin 7)	note 1	–	68	V
V_{oB}	output voltage (pin 4)		–	V_p	V
$I_{1,2,3,8,9}$	current in or out		−20	+20	mA
$V_{1,2,3,8,9}$	peak voltage		−0.5	V_p	V
Flyback switch					
$I_{o(flb)}$	peak output current		–	±1.8	A
Thermal data (in accordance with IEC 747-1)					
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		−25	+75	°C
T_{vj}	virtual junction temperature	note 2	–	150	°C
$R_{th\ vj-c}$	resistance v_j-case		–	5	K/W
$R_{th\ vj-a}$	resistance v_j-ambient in free air		–	45	K/W
Miscellaneous					
I_{LAUP}	latch-up current into any pin	+1.5xV_p (ABSmax) note 3	–	+200	mA
I_{LAUP}	latch-up current out of any pin	−1.5xV_p (ABSmax) note 3	−200	–	mA
V_{ESD}	electrostatic handling (M.M.)	note 4	–	±300	V
V_{ESD}	electrostatic handling (H.B.M.)	note 5	–	±2000	V

Notes

1. When the pin voltage supersedes 70 V the device behaves like a power zenerdiode thus limiting the voltage.
2. Internally limited by thermal protection; switching point ~ 170 °C.
3. At Tjmax.
4. Equivalent to discharge a 200 pF capacitor through a 0 Ω series resistor.
5. Equivalent to discharge a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

V_p = 12 V; V_{flb} = 45 V; f_v = 50 Hz; $V_{i(sb)}$ = 660 mV; T_{amb} = 25 °C; measured in test circuit of Fig.4; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC supply						
V_p	operating supply voltage		7.5	–	18	V
V_{flb}	flyback supply voltage	note 1	2 x V_p	–	66	V
$I_{pq(av.)}$	average quiescent supply current	during scan	–	10	15	mA
I_{pq}	quiescent supply current	no signal; no load	–	55	75	mA
$I_{flb(av.)}$	average flyback supply current	during scan	–	–	10	mA
Output stage A and B						
V_{loss1}	Voltage loss (3-7) plus (4-5)	I_o = 1.6 A; note 2	–	–	6.6	V
V_{loss2}	Voltage loss (3-4) plus (7-5)	I_o = 1.6 A; note 2	–	–	4.8	V
V_{loss1}	Voltage loss (3-7) plus (4-5)	I_o = 1.1 A; note 2	–	–	4.5	V
V_{loss2}	Voltage loss (3-4) plus (7-5)	I_o = 1.1 A; note 2	–	–	3.3	V
LEAB	linearity error	I_o = 3.2 A (p-p); note 3	–	1	2	%
LENAB	linearity error	I_o = 3.2 A (p-p); note 3	–	1	3	%
V_o	output voltage swing (flyback) $V_{oA} - V_{oB}$	$V_{i(diff)}$ = 0.6 V; I_o = 1.6 A	–	46	–	V
$\|V_{off}\|$	offset voltage across R_M	$V_{i(diff)}$= 0;$V_{i(sb)}$= 1V	–	–	20	mV
		$V_{i(diff)}$= 0; $V_{i(sb)}$= 200 mV	–	–	15	mV
$\Delta V_{off}T$	offset voltage drift = f(T)	$V_{i(diff)}$ = 0	–	–	40	µV/K
$V_{oA\ and\ B}$	DC output voltage	$V_{i(diff)}$ = 0;	–	$V_p/2$	–	V
G_{vo}	open-loop voltage gain V_{7-4}/V_{9-4}	notes 4 and 5	–	60	–	dB
f_{-3dB}	-3dB frequency	open loop	–	1	–	kHz
G_v	voltage gain V_{9-4}/V_{1-2}	note 4	–	1	–	
$\Delta G_v T$	voltage gain drift = f(T)		–	–	10^{-4}	1/K
PSRR	power supply rejection ratio	note 6	80	90	–	dB
Input stage						
$V_{i(sb)}$	signal bias voltage (pin 1 or pin 2)	note 7	100	660	1600	mV
$V_{i(diff)(p-p)}$	differential mode input voltage (p-p) pin 1 or pin 2	note 7	–	1000	1500	mV
$I_{i(bias)}$	input bias current pin 1 or pin 2		–	10	–	µA
Flyback switch						
$I_{o(flb)}$	output peak current	t< 1.5 msec.	–	–	±1.8	A
V_{loss}	voltage loss (V_{flb}–V_{oA})	I_o = +1.6 A	–	8	9	V
$I_{i(bias)}$	input bias current pin 1 or pin 2		-	10	-	µA

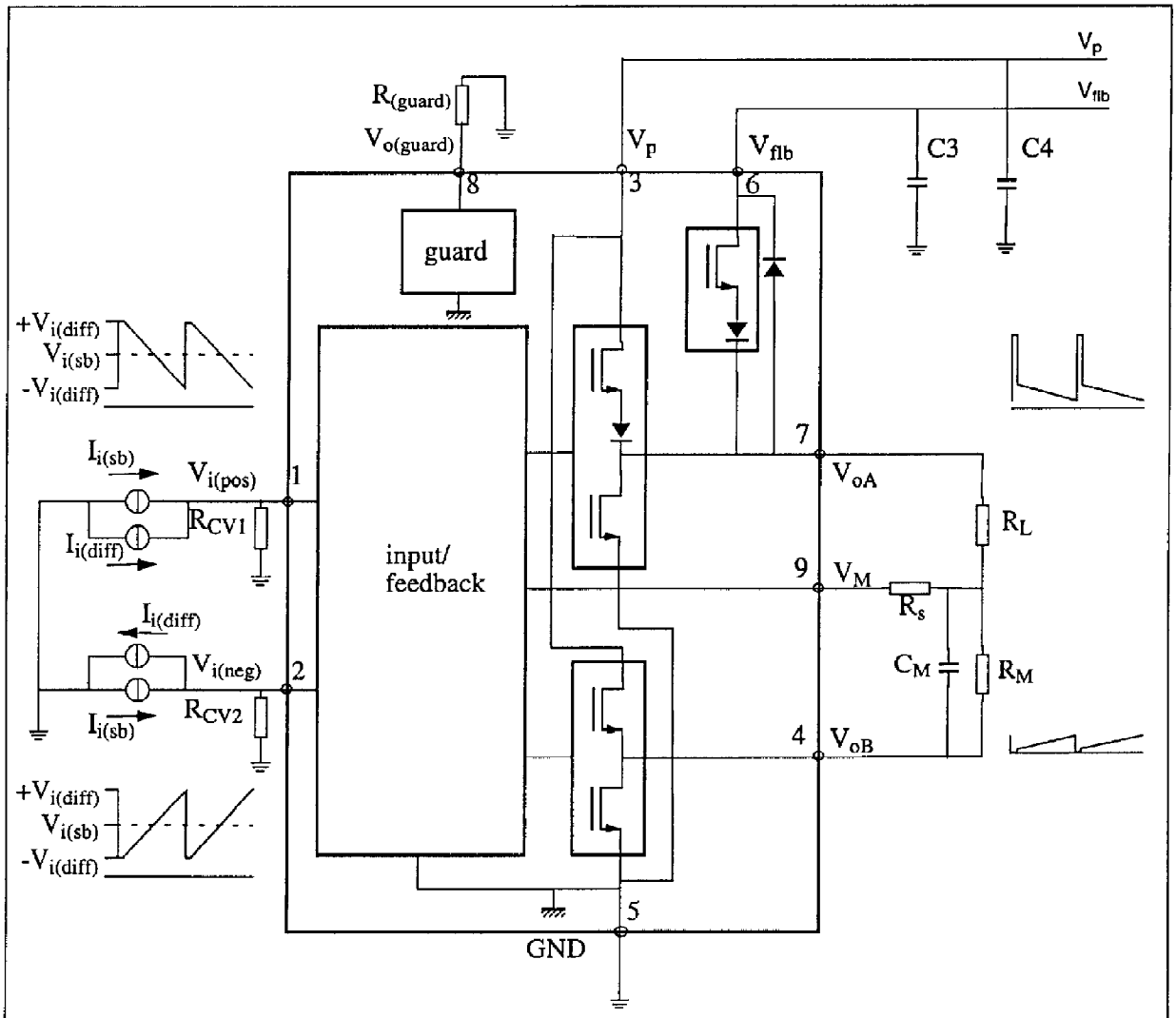
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Guard circuit						
$I_{o(guard)}$	output current	not active; $V_{o(guard)}$ = 0 V	–	–	10	µA
		active; $V_{o(guard)}$ = 4.5 V	1	–	2.5	mA
$V_{o(guard)}$	output voltage on pin 8	$I_{o(guard)}$ = 100 µA	5	6	7	V
	allowable voltage on pin 8	maximum leakage current = 10 µA;	–	–	18	V

Notes

1. To limit V_{oA} to 68V, the V_{flb} has to be 66V, due to the voltage drop of the internal flyback diode between pin 7 and pin 6 for the first part of the flyback.
2. At Tj = 125°C. The temperature coefficient of the V_{loss} has a positive sign.
3. The linearity error is measured for an linear input signal (without S-correction) and based on the same measurement principle as performed on the screen. The measuring method is as follows:
   Divide the output signal into 22 equal time parts ranging from 1 to 22 inclusive. Measure the value of the voltage across R_M of two succeeding parts called one block (a_k) starting with part 2 and 3 (block 1) and ending with part 20 and 21 (block 10). Thus part 1 and 22 are unused. The equations for linearity error for adjacent blocks (LEAB) and not adjacent blocks (LENAB) are given below

$$LEAB = \frac{a_k - a_{(k+1)}}{a_{avg}} \qquad LENAB = \frac{a_{max} - a_{min}}{a_{avg}}$$

4. The V value within formula, relates to voltages at or between relative pin numbers, i.e. V_{7-4}/V_{9-4} = voltage value across pins 7 and 4 divided by voltage value across pins 9 and 4.
5. Pin 9 disconnected from R_M.
6. At $V_{(ripple)}$ = 500 mV_{eff} at V_p; measured across R_M; $f_{(ripple)}$ = 50 Hz - 1 kHz.
7. $V_{i(sb)}+V_{i(diff)}$<1600 mV and $V_{i(sb)}-V_{i(diff)}$ >100 mV per pin.

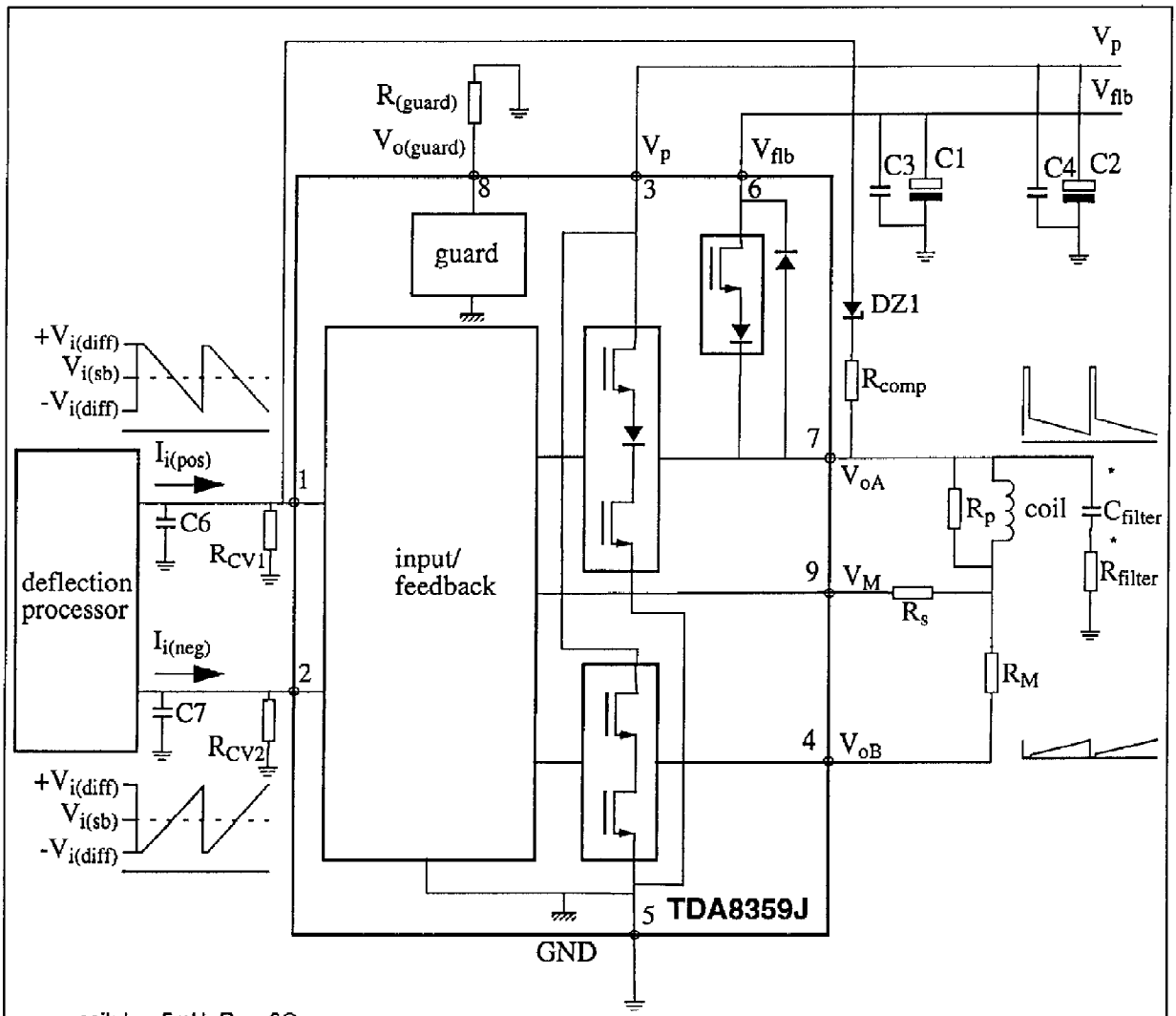


R_M = 0.5Ω;
R_{CV1} = 2.2kΩ;
R_{CV2} = R_{CV1} (1%);
R_L = 3.2Ω;
$R_{(guard)}$ = 4.7kΩ.
R_s = 2.7kΩ.

C3 = C4 = 100 nF;
C_M = 10 nF;

Fig.4 Test diagram.

APPLICATION INFORMATION



coil: L = 5mH; R_L = 6Ω

V_p = 14 V @ f_v = 50 Hz; *)

$I_{o(p-p)}$ = 2.4 A;

$I_{i(sb)}$ = 400 µA;

$I_{i(diff)(p-p)}$ = 480µA;

V_{flb} = 30 V;

t_{flb} = 640 µsec.

*) inclusive $spread_{(abs)}$ and temperature rise in the coil (W66ESF)

R_M = 0.6Ω;

R_{CV1} = 2.7kΩ;

R_{CV2} = R_{CV1} (1%);

R_p = 270Ω;

R_{comp} = 720kΩ;

$R_{(guard)}$ = 12kΩ.

R_s = 2.7kΩ.

DZ1 = 14V.

C1 = 47 µF 100V;

C2 = 220 µF 25V;

C3 = C4 = 100 nF;

C6 = C7 = 2.2 nF.

*) Optional:

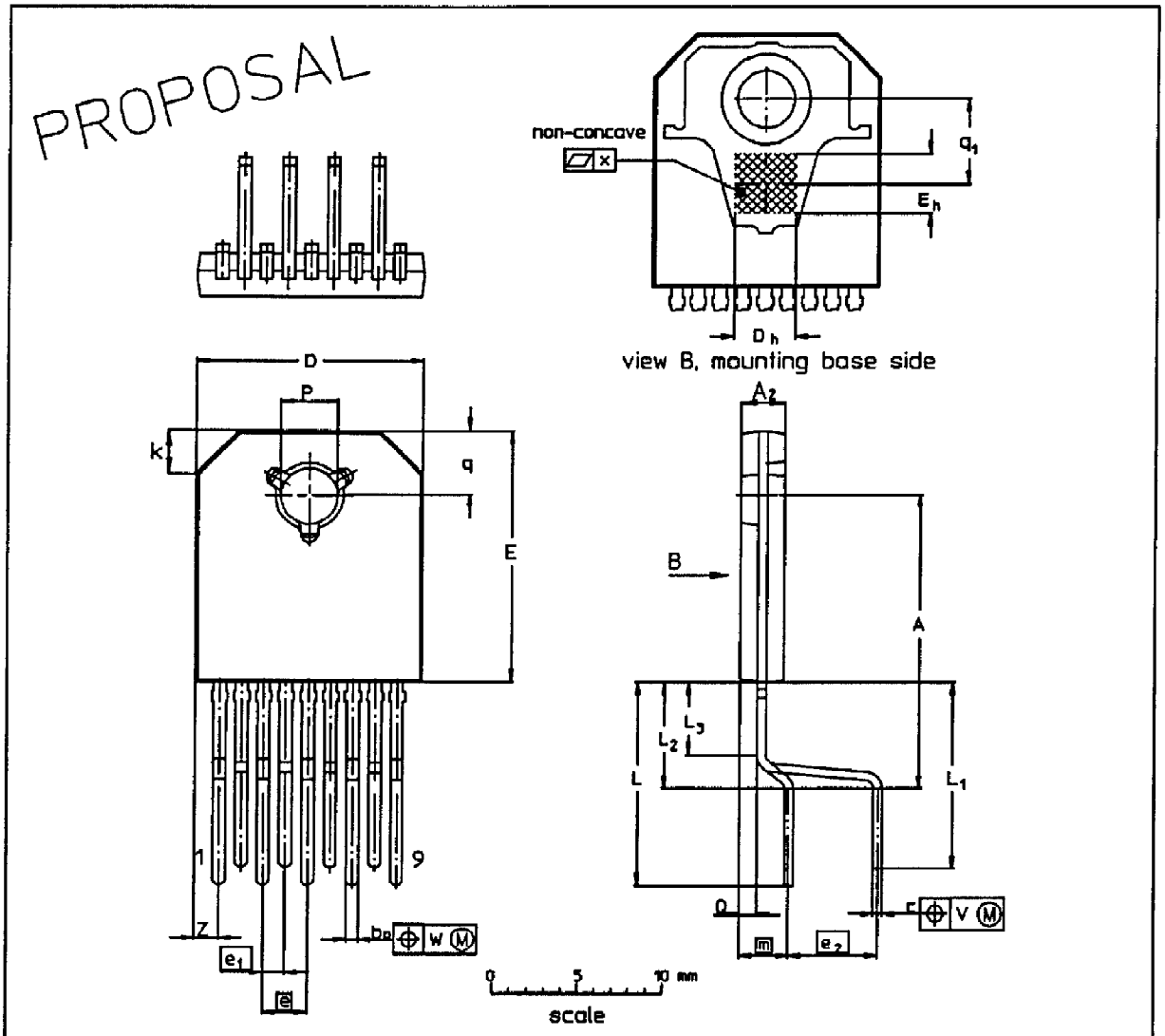
C_{filter} = 47nF;

R_{filter} = 22Ω.

Fig.5 Application diagram.

PACKAGE OUTLINE

DBS9P -plastic DIL-bent-SIL power package, 9 leads (lead length 12/11 mm), exposed die pad SOT523-1



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	b_p	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	k	L	L_1	L_2	L_3	m	P	Q	q	q_1	v	w	x	$Z^{(1)}$
mm	17.5 16.3	2.7 2.3	0.80 0.65	0.58 0.48	13.2 12.8	3.5	14.7 14.3	3.5	2.54	1.27	5.08	3.0 2.0	12.4 11.0	11.4 11.0	6.7 5.5	4.5 3.7	2.8	3.4 3.1	1.15 0.85	3.8 3.6	4.85	0.8	0.3	0.02	1.65 1.10

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT523-1						98-09-07

SOLDERING

Plastic SIL packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application Information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

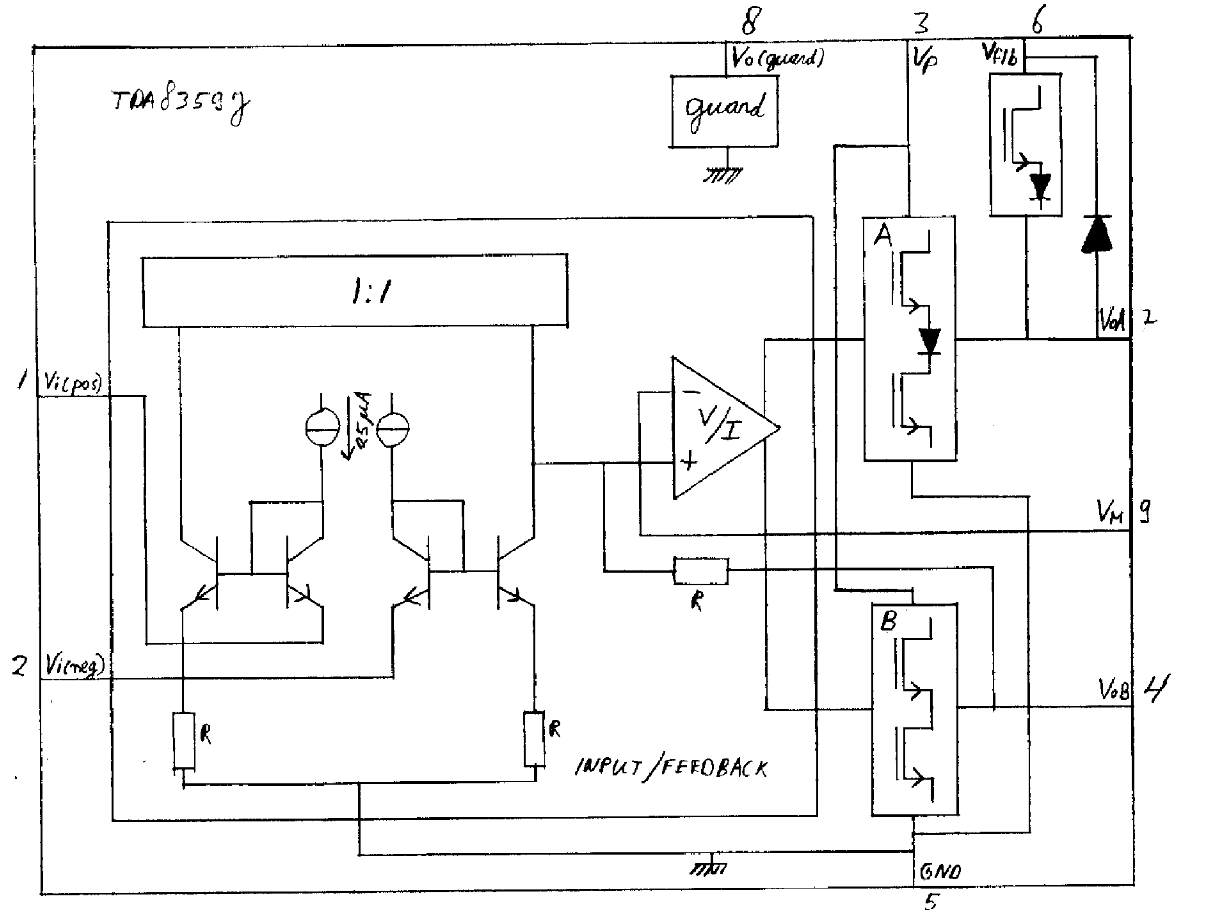
These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

NOTES

Datum 12 - 5 19 99

Onderwerp : Schema symbool voor Mentor Graphics; TDA 8357 J / TDA 8359 J

Door het schema van blz. 49 samen te voegen met het blok "input/feedback" op blz. 56, ontstaat het volgend schema-symbool. Zo zou het er uit moeten zien in Mentor Graphics



Use the schematic symbol of the TDA 8354 Q (9352 402 30112) as a reference for a.o. the dimension of the symbol. The height should be the same, the width proportional.

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Full bridge current driven vertical deflection output circuit in LVDMOS

TDA8354Q

BLOCK DIAGRAM

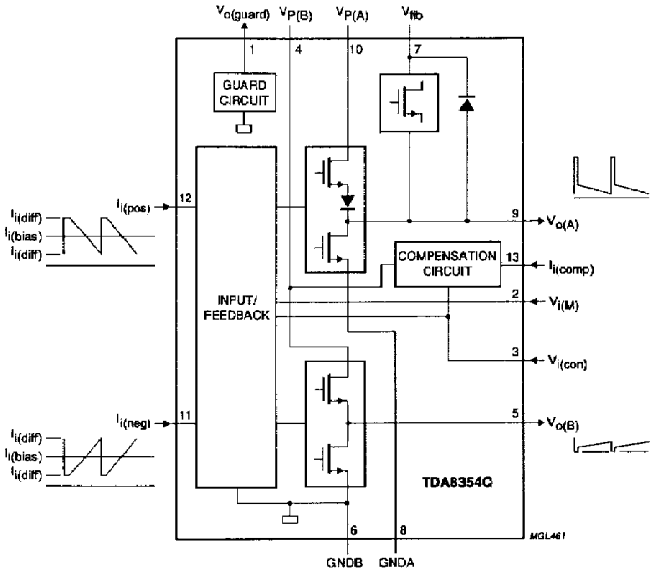

Fig.1 Block diagram.

Full bridge vertical deflection output circuit in LVDMOS

TDA8359J

BLOCK DIAGRAM

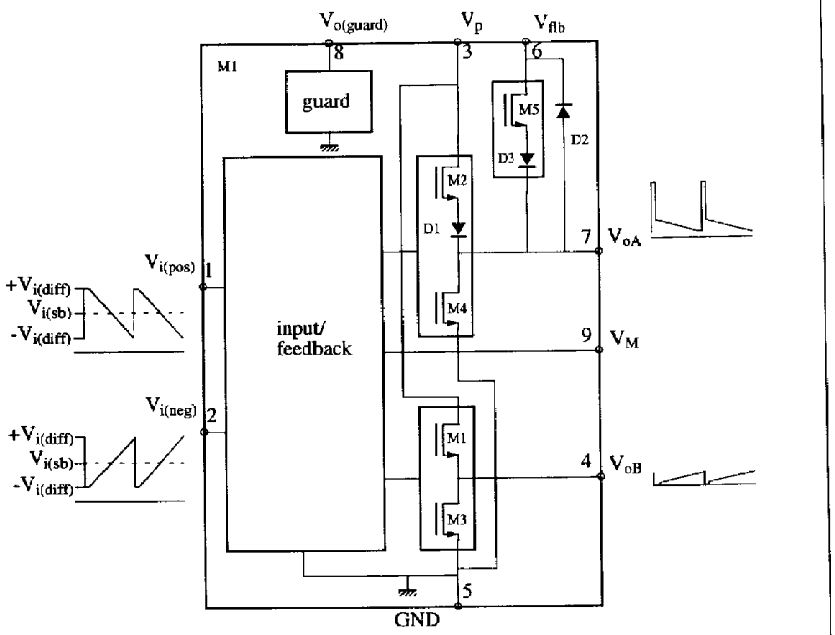

Fig.1 Block diagram.