

# DATA SHEET

## **TDA8357J**

Full bridge vertical deflection output  
circuit in LVDMOS

Preliminary specification  
File under Integrated Circuits, IC02

1999 Nov 10

## Full bridge vertical deflection output circuit in LVDMOS

## TDA8357J

### FEATURES

- Few external components required
- High efficiency fully DC coupled vertical bridge output circuit
- Vertical flyback switch with short rise and fall times
- Built-in guard circuit
- Thermal protection circuit
- Improved EMC performance due to differential inputs.

### GENERAL DESCRIPTION

The TDA8357J is a power circuit for use in 90° and 110° colour deflection systems for 25 to 200 Hz field frequencies, and for 4 : 3 and 16 : 9 picture tubes. The IC contains a vertical deflection output circuit, operating as a high efficiency class G system. The full bridge output circuit allows DC coupling of the deflection coil in combination with single positive supply voltages.

The IC is constructed in a Low Voltage DMOS (LVDMOS) process that combines bipolar, CMOS and DMOS devices. DMOS transistors are used in the output stage because of absence of second breakdown.

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supplies</b>						
$V_P$	supply voltage		7.5	12	18	V
$V_{FB}$	flyback supply voltage		$2V_P$	45	66	V
$I_{q(P)(av)}$	average quiescent supply current	during scan	–	10	15	mA
$I_{q(FB)(av)}$	average quiescent flyback supply current	during scan	–	–	10	mA
$P_{tot}$	total power dissipation		–	–	8	W
<b>Inputs and outputs</b>						
$V_{i(dif)(p-p)}$	differential input voltage (peak-to-peak value)		–	1000	1500	mV
$I_{o(p-p)}$	output current (peak-to-peak value)		–	–	2.0	A
<b>Flyback switch</b>						
$I_{o(peak)}$	maximum (peak) output current	$t \leq 1.5$ ms	–	–	$\pm 1.2$	A
<b>Thermal data; in accordance with IEC 747-1</b>						
$T_{stg}$	storage temperature		–55	–	+150	°C
$T_{amb}$	ambient temperature		–25	–	+75	°C
$T_j$	junction temperature		–	–	150	°C

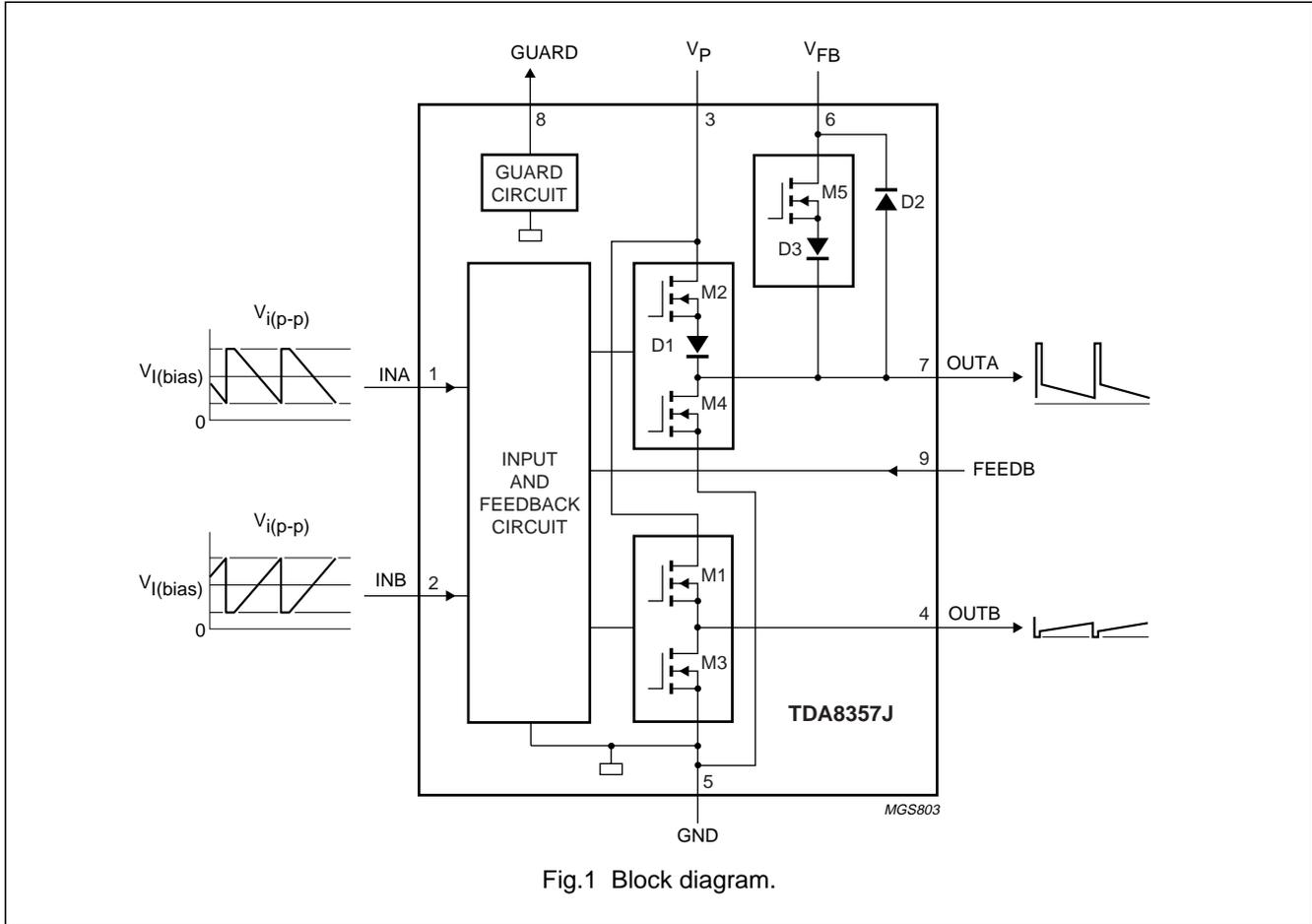
### ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8357J	DBS9P	plastic DIL-bent-SIL power package; 9 leads (lead length 12/11 mm); exposed die pad	SOT523-1

Full bridge vertical deflection output circuit  
in LVDMOS

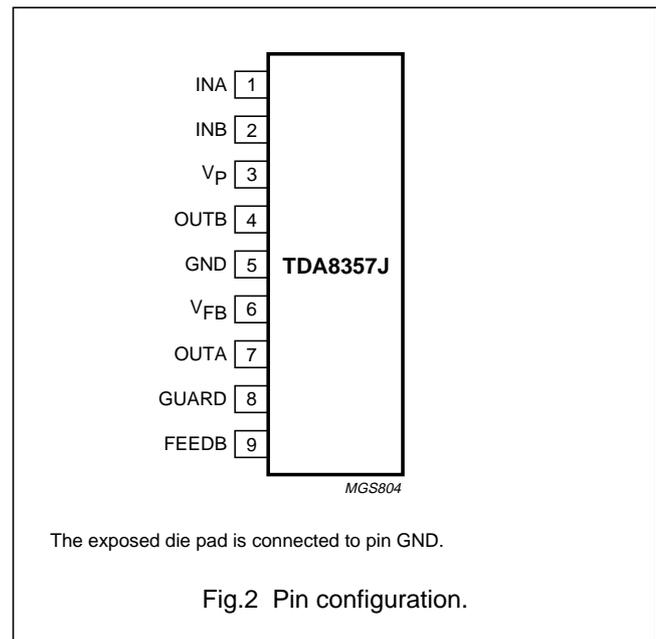
TDA8357J

BLOCK DIAGRAM



PINNING

SYMBOL	PIN	DESCRIPTION
INA	1	input A
INB	2	input B
VP	3	supply voltage
OUTB	4	output B
GND	5	ground
VFB	6	flyback supply voltage
OUTA	7	output A
GUARD	8	guard output
FEEDB	9	feedback input



## Full bridge vertical deflection output circuit in LVDMOS

TDA8357J

### FUNCTIONAL DESCRIPTION

#### Vertical output stage

The vertical driver circuit has a bridge configuration. The deflection coil is connected between the complimentary driven output amplifiers. The differential input circuit is voltage driven. The input circuit is specially designed for direct connection to driver circuits delivering a differential signal but it is also suitable for single-ended applications. The output currents of the driver device are converted to voltages by the conversion resistors  $R_{CV1}$  and  $R_{CV2}$  (see Fig.3) connected to pins INA and INB. The differential input voltage is compared with the voltage across the measuring resistor  $R_M$ , providing internal feedback information. The voltage across  $R_M$  is proportional with the output current. The relationship between the differential input current and the output current is defined by:

$$2 \times I_{i(dif)(p-p)} \times R_{CV} = I_{o(p-p)} \times R_M$$

The output current should measure 0.5 to 2.0 A (p-p) and is determined by the value of  $R_M$  and  $R_{CV}$ . The allowable input voltage range is 100 mV to 1.6 V for each input. The formula given does not include internal bondwire resistances. Depending on the values of  $R_M$  and the internal bondwire resistance (typical value of 50 m $\Omega$ ) the actual value of the current in the deflection coil will be about 5% lower than calculated.

#### Flyback supply

The flyback voltage is determined by the flyback supply voltage  $V_{FB}$ . The principle of two supply voltages (class G) allows to use an optimum supply voltage  $V_P$  for scan and an optimum flyback supply voltage  $V_{FB}$  for flyback, thus very high efficiency is achieved. The available flyback output voltage across the coil is almost equal to  $V_{FB}$ , due to the absence of a coupling capacitor which is not required in a bridge configuration. The very short rise and fall times of the flyback switch are determined mainly by the slew-rate value of more than 300 V/ $\mu$ s.

#### Protection

The output circuit contains protection circuits for:

- Too high die temperature
- Overvoltage of output A.

#### Guard circuit

A guard circuit with output pin GUARD is provided.

The guard circuit generates a HIGH-level during the flyback period. The guard circuit is also activated for one of the following conditions:

- During thermal protection ( $T_j \approx 170$  °C)
- During an open-loop condition.

The guard signal can be used for blanking the picture tube and signalling fault conditions. The vertical synchronization pulses of the guard signal can be used by an On Screen Display (OSD) microcontroller.

#### Damping resistor compensation

HF loop stability is achieved by connecting a damping resistor  $R_{D1}$  across the deflection coil. The current values in  $R_{D1}$  during scan and flyback are significantly different. Both the resistor current and the deflection coil current flow into measuring resistor  $R_M$ , resulting in a too low deflection coil current at the start of the scan.

The difference in the damping resistor current values during scan and flyback have to be externally compensated in order to achieve a short settling time. For that purpose a compensation resistor  $R_{CMP}$  in series with a zener diode is connected between pins OUTA and INA (see Fig.4). The zener diode voltage value should be equal to  $V_P$ . The value of  $R_{CMP}$  is calculated by:

$$R_{CMP} = \frac{(V_{FB} - V_{loss(FB)} - V_Z) \times R_{D1} \times R_{CV1}}{(V_{FB} - V_{loss(FB)} - I_{coil(peak)} \times R_{coil}) \times R_M}$$

where:

- $V_{loss(FB)}$  is the voltage loss between pins  $V_{FB}$  and OUTA at flyback
- $R_{coil}$  is the deflection coil resistance
- $V_Z$  is the voltage of zener diode D5.

## Full bridge vertical deflection output circuit in LVDMOS

TDA8357J

### LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_P$	supply voltage		–	18	V
$V_{FB}$	flyback supply voltage		–	68	V
$V_n$	DC voltage pin OUTA pin OUTB pins INA, INB, GUARD and FEEDB	note 1	– – –0.5	68 $V_P$ $V_P$	V V V
$I_n$	DC current pins OUTA and OUTB pins OUTA and OUTB pins INA, INB, GUARD and FEEDB	during scan (p-p) at flyback (peak); $t \leq 1.5$ ms	– – –20	2.0 $\pm 1.2$ +20	A A mA
$I_{lu}$	latch-up current	current into any pin; pin voltage is $1.5 \times V_P$ ; note 2	–	+200	mA
		current out of any pin; pin voltage is $-1.5 \times V_P$ ; note 2	–200	–	mA
$V_{es}$	electrostatic handling voltage	machine model; note 3	–300	+300	V
		human body model; note 4	–2000	+2000	V
$P_{tot}$	total power dissipation		–	8	W
$T_{stg}$	storage temperature		–55	+150	°C
$T_{amb}$	ambient temperature		–25	+75	°C
$T_j$	junction temperature	note 5	–	150	°C

### Notes

- When the voltage at pin OUTA supersedes 70 V the circuit will limit the voltage.
- At  $T_{j(max)}$ .
- Equivalent to 200 pF capacitance discharge through a 0  $\Omega$  resistor.
- Equivalent to 100 pF capacitance discharge through a 1.5 k $\Omega$  resistor.
- Internally limited by thermal protection at  $T_j \approx 170$  °C.

### THERMAL CHARACTERISTICS

In accordance with IEC 747-1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th(j-c)}$	thermal resistance from junction to case		–	–	6	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	–	–	65	K/W

## Full bridge vertical deflection output circuit in LVDMOS

TDA8357J

### CHARACTERISTICS

$V_P = 12\text{ V}$ ;  $V_{FB} = 45\text{ V}$ ;  $f_{\text{vert}} = 50\text{ Hz}$ ;  $V_{I(\text{bias})} = 880\text{ mV}$ ;  $T_{\text{amb}} = 25\text{ °C}$ ; measured in test circuit of Fig.3; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supplies</b>						
$V_P$	operating supply voltage		7.5	12	18	V
$V_{FB}$	flyback supply voltage	note 1	$2V_P$	45	66	V
$I_{q(P)(\text{av})}$	average quiescent supply current	during scan	–	10	15	mA
$I_{q(P)}$	quiescent supply current	no signal; no load	–	55	75	mA
$I_{q(FB)(\text{av})}$	average quiescent flyback supply current	during scan	–	–	10	mA
<b>Inputs A and B</b>						
$V_{i(\text{dif})(\text{p-p})}$	differential input voltage (peak-to-peak value)	note 2	–	1000	1500	mV
$V_{I(\text{bias})}$	input bias voltage	note 2	100	880	1600	mV
$I_{I(\text{bias})}$	input bias current		–	25	35	$\mu\text{A}$
<b>Outputs A and B</b>						
$V_{\text{loss}(1)}$	voltage loss first scan part	note 3 $I_o = 0.7\text{ A}$ $I_o = 1.0\text{ A}$	– –	– –	3.9 5.5	V V
$V_{\text{loss}(2)}$	voltage loss second scan part	note 4 $I_o = -0.7\text{ A}$ $I_o = -1.0\text{ A}$	– –	– –	2.8 4.0	V V
$I_{o(\text{p-p})}$	output current (peak-to-peak value)		–	–	2.0	A
LE	linearity error	$I_{o(\text{p-p})} = 2.0\text{ A}$ ; notes 5 and 6 adjacent blocks non adjacent blocks	– –	1 1	2 3	% %
$V_{\text{offset}}$	offset voltage	across $R_M$ ; $V_{i(\text{dif})} = 0\text{ V}$ $V_{I(\text{bias})} = 200\text{ mV}$ $V_{I(\text{bias})} = 1\text{ V}$	– –	– –	$\pm 15$ $\pm 25$	mV mV
$\Delta V_{\text{offset}(T)}$	offset voltage variation with temperature	across $R_M$ ; $V_{i(\text{dif})} = 0\text{ V}$	–	–	40	$\mu\text{V/K}$
$V_O$	DC output voltage	$V_{i(\text{dif})} = 0\text{ V}$	–	$0.5V_P$	–	V
$G_{V(\text{ol})}$	open-loop voltage gain	notes 7 and 8	–	60	–	dB
$f_{-3\text{dB}(h)}$	high –3 dB cut-off frequency	open-loop	–	1	–	kHz
$G_V$	voltage gain	note 9	–	1	–	
$\Delta G_{V(T)}$	voltage gain variation with the temperature		–	–	$10^{-4}$	$\text{K}^{-1}$
PSRR	power supply rejection ratio	note 10	80	90	–	dB

# Full bridge vertical deflection output circuit in LVDMOS

TDA8357J

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Flyback switch</b>						
$I_{O(\text{peak})}$	maximum (peak) output current	$t \leq 1.5 \text{ ms}$	–	–	$\pm 1.2$	A
$V_{\text{loss(FB)}}$	voltage loss at flyback	note 11 $I_o = 0.7 \text{ A}$ $I_o = 1.0 \text{ A}$	– –	7.5 8	8.5 9	V V
<b>Guard circuit</b>						
$V_{O(\text{grd})}$	guard output voltage	$I_{O(\text{grd})} = 100 \mu\text{A}$	5	6	7	V
$V_{O(\text{grd})(\text{max})}$	allowable guard voltage	maximum leakage current $I_{L(\text{max})} = 10 \mu\text{A}$	–	–	18	V
$I_{O(\text{grd})}$	output current	$V_{O(\text{grd})} = 0 \text{ V}$ ; not active	–	–	10	$\mu\text{A}$
		$V_{O(\text{grd})} = 4.5 \text{ V}$ ; active	1	–	2.5	mA

**Notes**

- To limit  $V_{\text{OUTA}}$  to 68 V,  $V_{\text{FB}}$  must be 66 V due to the voltage drop of the internal flyback diode between pins OUTA and  $V_{\text{FB}}$  at the first part of the flyback.
- Allowable input range:  $V_{I(\text{bias})} + V_{i(\text{dif})} < 1600 \text{ mV}$  and  $V_{I(\text{bias})} - V_{i(\text{dif})} > 100 \text{ mV}$  for each input.
- This value specifies the sum of the voltage losses of the internal current paths between pins  $V_P$  and OUTA, and between pins OUTB and GND. Specified for  $T_j = 125 \text{ }^\circ\text{C}$ . The temperature coefficient for  $V_{\text{loss}(1)}$  is a positive value.
- This value specifies the sum of the voltage losses of the internal current paths between pins  $V_P$  and OUTB, and between pins OUTA and GND. Specified for  $T_j = 125 \text{ }^\circ\text{C}$ . The temperature coefficient for  $V_{\text{loss}(2)}$  is a positive value.
- The linearity error is measured for a linear input signal without S-correction and is based on the 'on screen' measurement principle. This method is defined as follows. The output signal is divided in 22 successive equal time blocks  $k$ . The 1st and 22nd blocks are ignored, while the voltage amplitudes are measured across  $R_M$ , starting at  $k = 2$  and ending at  $k = 21$ , where  $V_k$  and  $V_{k+1}$  are the measured voltages of two successive blocks.  $V_{\text{min}}$ ,  $V_{\text{max}}$  and  $V_{\text{avg}}$  are the minimum, maximum and average voltages respectively. The linearity errors are defined as:

$$\text{a) } LE = \frac{V_k - V_{k+1}}{V_{\text{avg}}} \text{ (adjacent blocks)}$$

$$\text{b) } LE = \frac{V_{\text{max}} - V_{\text{min}}}{V_{\text{avg}}} \text{ (non adjacent blocks)}$$

- The linearity errors are specified for a minimum input voltage of 300 mV (p-p). Lower input voltages lead to voltage dependent S-distortion in the input stage.

$$7. \quad G_{V(\text{ol})} = \frac{V_{\text{OUTA}} - V_{\text{OUTB}}}{V_{\text{FEEDB}} - V_{\text{OUTB}}}$$

- Pin FEEDB not connected.

$$9. \quad G_V = \frac{V_{\text{FEEDB}} - V_{\text{OUTB}}}{V_{\text{INA}} - V_{\text{INB}}}$$

- $V_{P(\text{ripple})} = 500 \text{ mV}$  (RMS value);  $50 \text{ Hz} < f_{P(\text{ripple})} < 1 \text{ kHz}$ ; measured across  $R_M$ .

- This value specifies the internal voltage loss of the current path between pins  $V_{\text{FB}}$  and OUTA.

Full bridge vertical deflection output circuit  
in LVDMOS

TDA8357J

APPLICATION INFORMATION

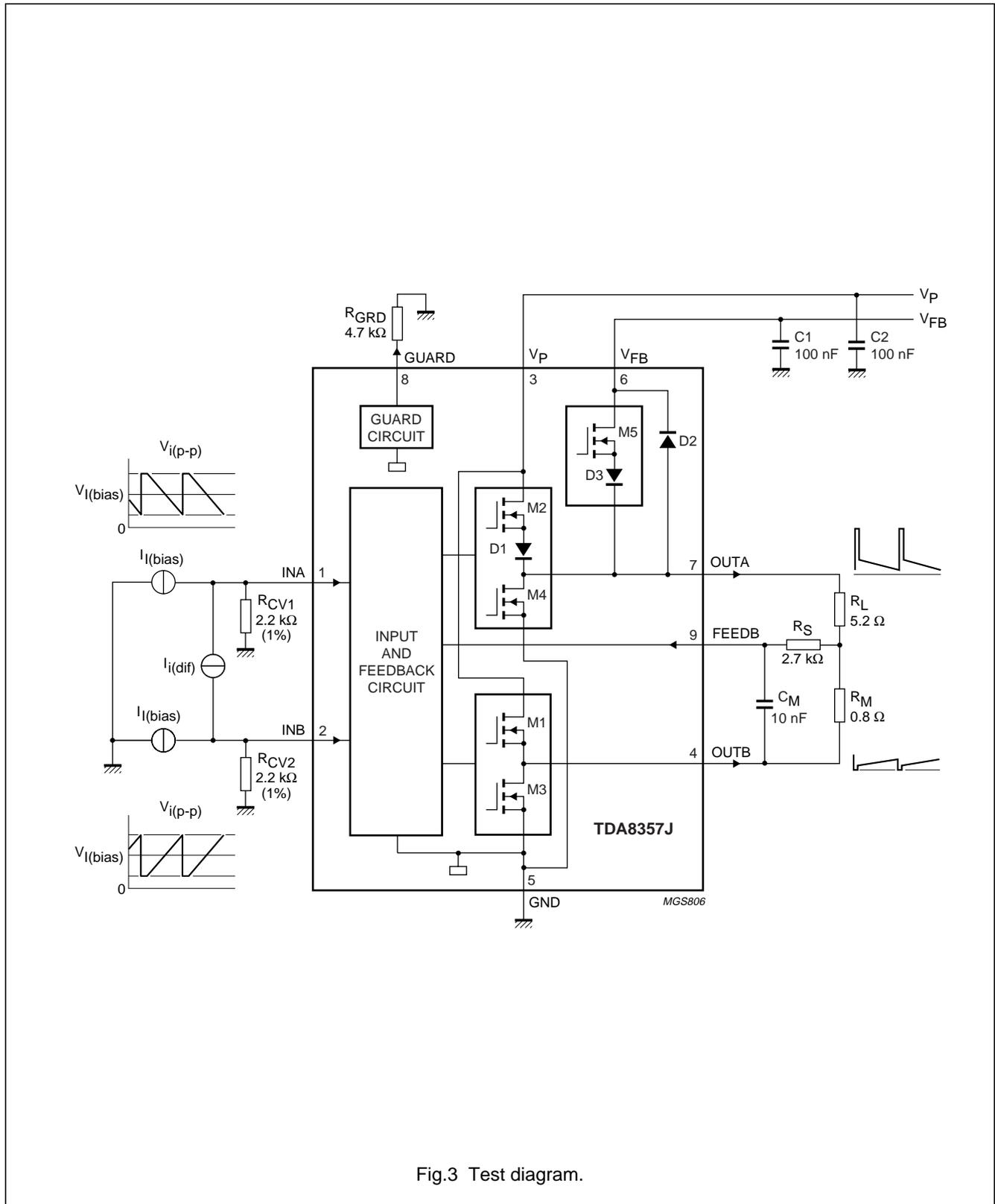
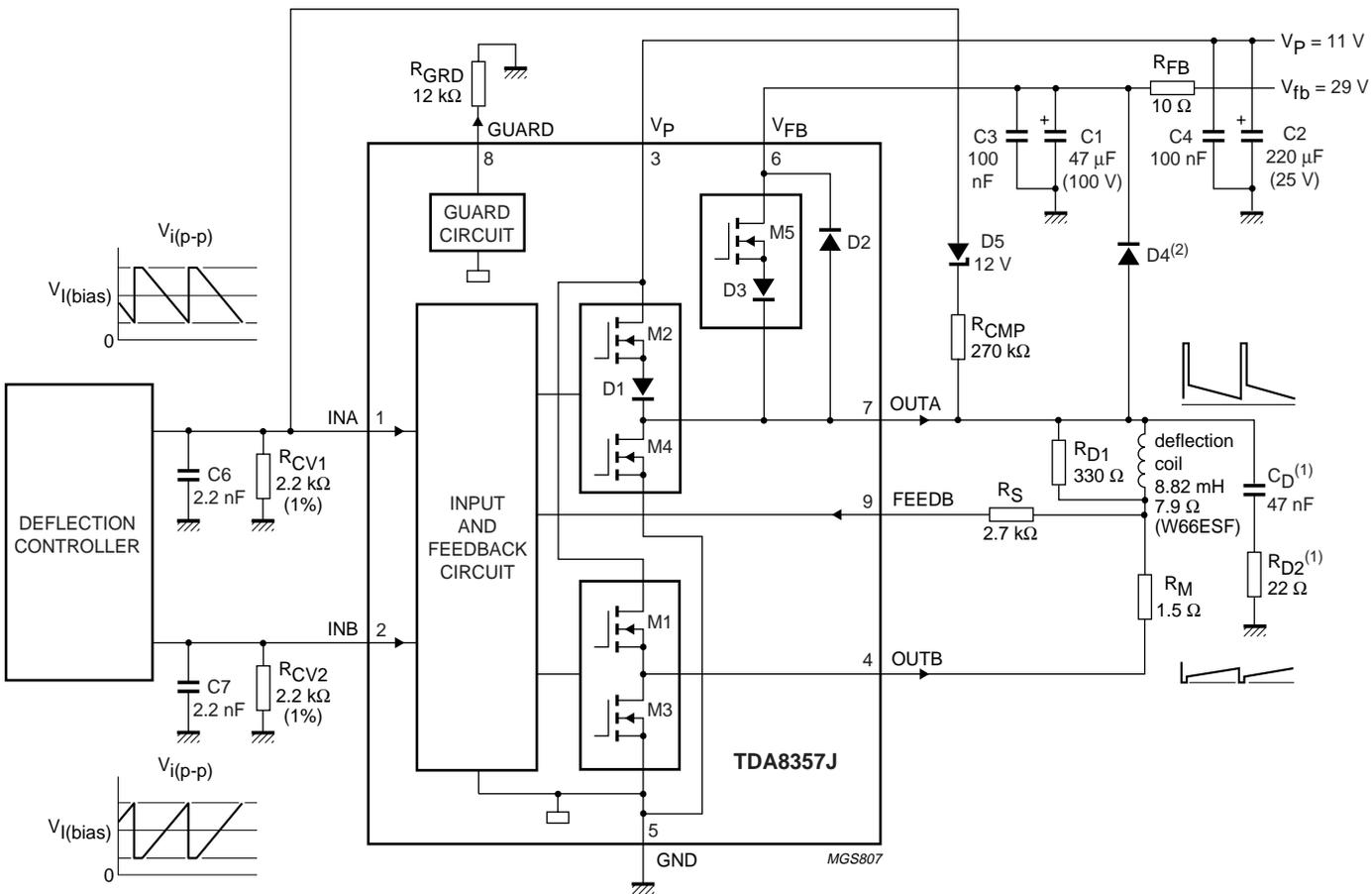


Fig.3 Test diagram.

Full bridge vertical deflection output circuit in LVDMOS

TDA8357J



$f_{\text{vert}} = 50 \text{ Hz}$ ;  $t_{\text{FB}} = 640 \mu\text{s}$ ;  $I_{\text{I(bias)}} = 400 \mu\text{A}$ ;  $I_{\text{I(dif)(peak)}} = 494 \mu\text{A}$ ;  $I_{\text{O(p-p)}} = 1.45 \text{ A}$ .

(1) Optional, depending on the deflection coil impedance.

(2) Optional extended flash over protection; BYD33D or equivalent.

Fig.4 Application diagram.

# Full bridge vertical deflection output circuit in LVDMOS

TDA8357J

## Supply voltage calculation

For calculating the minimum required supply voltage, several specific application parameter values have to be known. These parameters are the required maximum (peak) deflection coil current  $I_{coil(peak)}$ , the coil parameters  $R_{coil}$  and  $L_{coil}$ , and the measuring resistance of  $R_M$ . The required maximum (peak) deflection coil current should also include the overscan.

The deflection coil resistance has to be multiplied with 1.2 in order to take account of hot conditions.

Chapter "Characteristics" supplies values for the voltage losses of the vertical output stage. For the first part of the scan the voltage loss is given by  $V_{loss(1)}$ . For the second part of the scan the voltage loss is given by  $V_{loss(2)}$ .

The voltage drop across the deflection coil during scan is determined by the coil impedance. For the first part of the scan the inductive contribution and the ohmic contribution to the total coil voltage drop are of opposite sign, while for the second part of the scan the inductive part and the ohmic part have the same sign.

For the vertical frequency the maximum frequency occurring must be applied to the calculations.

The required power supply voltage  $V_P$  for the first part of the scan is given by:

$$V_{P(1)} = I_{coil(peak)} \times (R_{coil} + R_M) - L_{coil} \times 2I_{coil(peak)} \times f_{vert(max)} + V_{loss(1)}$$

The required power supply voltage  $V_P$  for the second part of the scan is given by:

$$V_{P(2)} = I_{coil(peak)} \times (R_{coil} + R_M) + L_{coil} \times 2I_{coil(peak)} \times f_{vert(max)} + V_{loss(2)}$$

The minimum required supply voltage  $V_P$  shall be the highest of the two values  $V_{P(1)}$  and  $V_{P(2)}$ . Spread in supply voltage and component values also has to be taken into account.

## Flyback supply voltage calculation

If the flyback time is known, the required flyback supply voltage can be calculated by the simplified formula:

$$V_{FB} = I_{coil(p-p)} \times \frac{R_{coil} + R_M}{1 - e^{-t_{FB}/x}}$$

where:

$$x = \frac{L_{coil}}{R_{coil} + R_M}$$

The flyback supply voltage calculated this way is about 5% to 10% higher than required.

## Calculation of the power dissipation of the vertical output stage

The IC total power dissipation is given by the formula:

$$P_{tot} = P_{sup} - P_L$$

The power to be supplied is given by the formula:

$$P_{sup} = V_P \times \frac{I_{coil(peak)}}{2} + V_P \times 0.015 [A] + 0.3 [W]$$

In this formula 0.3 [W] represents the average value of the losses in the flyback supply.

The average external load power dissipation in the deflection coil and the measuring resistor is given by the formula:

$$P_L = \frac{(I_{coil(peak)})^2}{3} \times (R_{coil} + R_M)$$

## Example

Table 1 Application values

SYMBOL	VALUE	UNIT
$I_{coil(peak)}$	0.725	A
$I_{coil(p-p)}$	1.45	A
$L_{coil}$	8.82	mH
$R_{coil}$	7.9	$\Omega$
$R_M$	1.5	$\Omega$
$f_{vert}$	50	Hz
$t_{FB}$	640	$\mu$ s

Table 2 Calculated values

SYMBOL	VALUE	UNIT
$V_P$	11	V
$R_M + R_{coil} (hot)$	11	$\Omega$
$t_{vert}$	0.02	s
x	0.000802	
$V_{FB}$	29	V
$P_{sup}$	4.45	W
$P_L$	1.93	W
$P_{tot}$	2.52	W

## Full bridge vertical deflection output circuit in LVDMOS

TDA8357J

### Heatsink calculation

The value of the heatsink can be calculated in a standard way with a method based on average temperatures.

The required thermal resistance of the heatsink is determined by the maximum die temperature of 150 °C.

**In general we recommend to design for an average die temperature not exceeding 130 °C.**

#### EXAMPLE

Measured or given values:  $P_{\text{tot}} = 3 \text{ W}$ ;  $T_{\text{amb}} = 40 \text{ °C}$ ;  
 $T_j = 110 \text{ °C}$ ;  $R_{\text{th}(j-c)} = 5 \text{ K/W}$ ;  $R_{\text{th}(c-h)} = 2 \text{ K/W}$ .

The required heatsink thermal resistance is given by:

$$R_{\text{th}(h-a)} = \frac{T_j - T_{\text{amb}}}{P_{\text{tot}}} - (R_{\text{th}(j-c)} + R_{\text{th}(c-h)})$$

When we use the values given we find:

$$R_{\text{th}(h-a)} = \frac{110 - 40}{3.0} - (5 + 2) = 16 \text{ K/W}$$

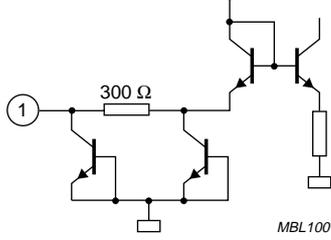
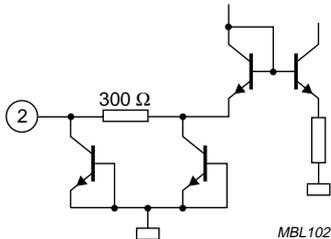
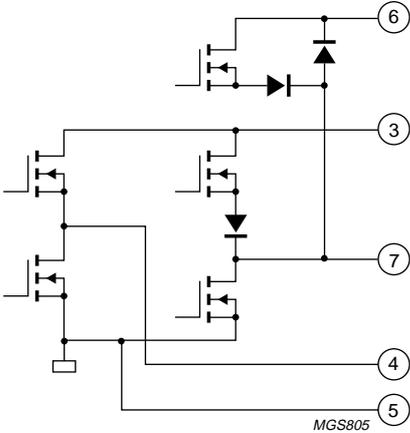
The heatsink temperature will be:

$$T_h = T_{\text{amb}} + (R_{\text{th}(h-a)} \times P_{\text{tot}}) = 40 + (3 \times 16) = 90 \text{ °C}$$

Full bridge vertical deflection output circuit  
in LVDMOS

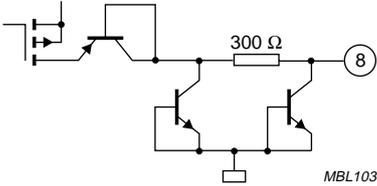
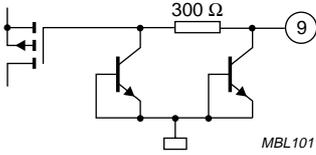
TDA8357J

INTERNAL PIN CONFIGURATION

PIN	SYMBOL	EQUIVALENT CIRCUIT
1	INA	
2	INB	
3	$V_P$	
4	OUTB	
5	GND	
6	$V_{FB}$	
7	OUTA	

Full bridge vertical deflection output circuit  
in LVDMOS

TDA8357J

PIN	SYMBOL	EQUIVALENT CIRCUIT
8	GUARD	
9	FEEDB	

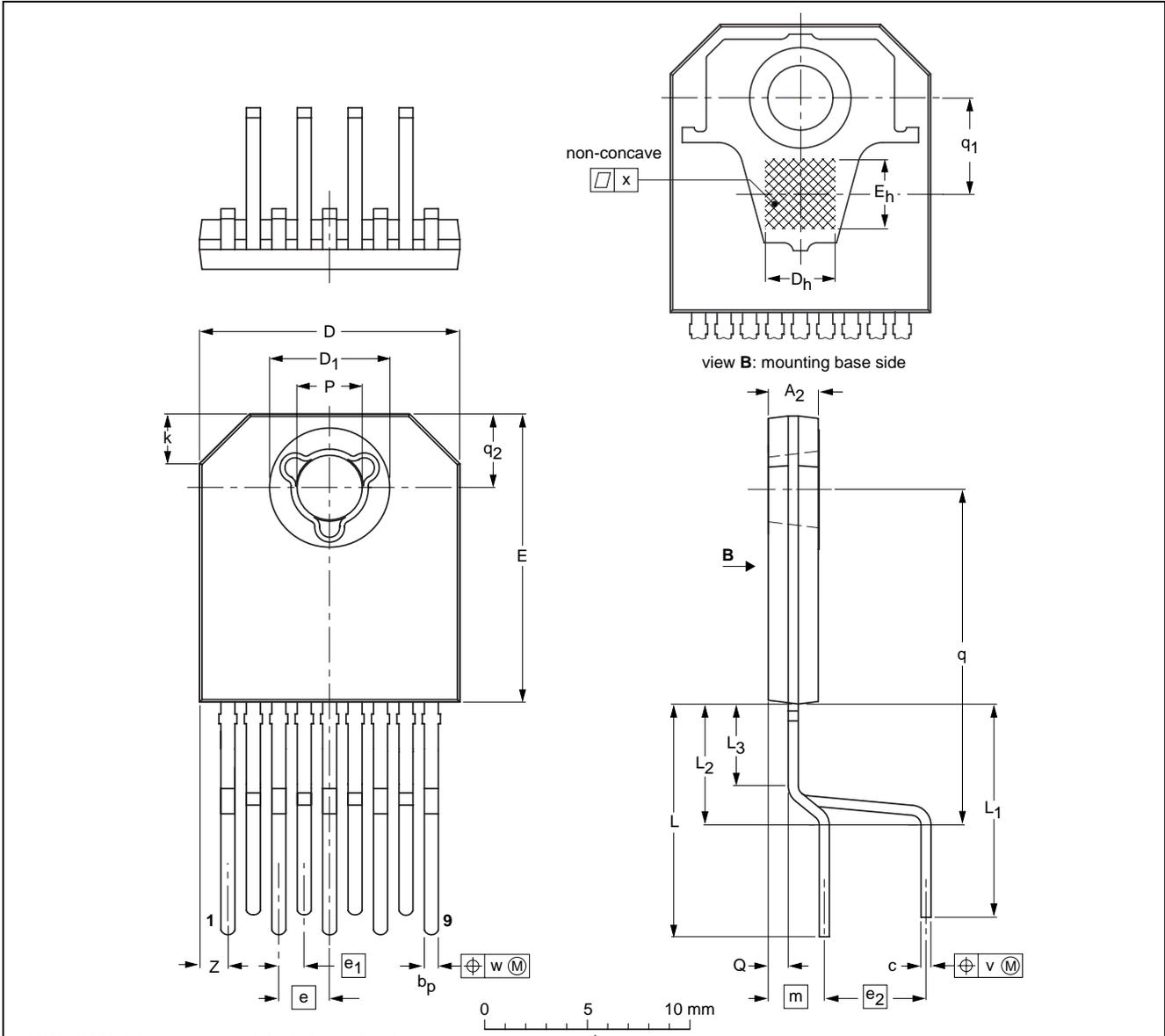
Full bridge vertical deflection output circuit  
in LVDMOS

TDA8357J

PACKAGE OUTLINE

DBS9P: plastic DIL-bent-SIL power package; 9 leads (lead length 12/11 mm); exposed die pad

SOT523-1



DIMENSIONS (mm are the original dimensions)

UNIT	A <sub>2</sub> <sup>(2)</sup>	b <sub>p</sub>	c	D <sup>(1)</sup>	D <sub>1</sub> <sup>(2)</sup>	D <sub>h</sub>	E <sup>(1)</sup>	E <sub>h</sub>	e	e <sub>1</sub>	e <sub>2</sub>	k	L	L <sub>1</sub>	L <sub>2</sub>	L <sub>3</sub>	m	P	Q	q	q <sub>1</sub>	q <sub>2</sub>	v	w	x	z <sup>(1)</sup>
mm	2.7 2.3	0.80 0.65	0.58 0.48	13.2 12.8	6.2 5.8	3.5	14.7 14.3	3.5	2.54	1.27	5.08	3.0 2.0	12.4 11.0	11.4 10.0	6.7 5.5	4.5 3.7	2.8	3.4 3.1	1.15 0.85	17.5 16.3	4.85	3.8 3.6	0.8	0.3	0.02	1.65 1.10

Notes

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.
2. Plastic surface within circle area D<sub>1</sub> may protrude 0.04 mm maximum.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT523-1						98-11-12

## Full bridge vertical deflection output circuit in LVDMOS

TDA8357J

### SOLDERING

#### Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our "Data Handbook IC26; Integrated Circuit Packages" (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

#### Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg(max)}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

#### Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

#### Suitability of through-hole mount IC packages for dipping and wave soldering methods

PACKAGE	SOLDERING METHOD	
	DIPPING	WAVE
DBS, DIP, HDIP, SDIP, SIL	suitable	suitable <sup>(1)</sup>

#### Note

- For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

### DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

### LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

# Philips Semiconductors – a worldwide company

**Argentina:** see South America

**Australia:** 3 Figtree Drive, HOMEBUSH, NSW 2140,  
Tel. +61 2 9704 8141, Fax. +61 2 9704 8139

**Austria:** Computerstr. 6, A-1101 WIEN, P.O. Box 213,  
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

**Belarus:** Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,  
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

**Belgium:** see The Netherlands

**Brazil:** see South America

**Bulgaria:** Philips Bulgaria Ltd., Energoproject, 15th floor,  
51 James Bourchier Blvd., 1407 SOFIA,  
Tel. +359 2 68 9211, Fax. +359 2 68 9102

**Canada:** PHILIPS SEMICONDUCTORS/COMPONENTS,  
Tel. +1 800 234 7381, Fax. +1 800 943 0087

**China/Hong Kong:** 501 Hong Kong Industrial Technology Centre,  
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,  
Tel. +852 2319 7888, Fax. +852 2319 7700

**Colombia:** see South America

**Czech Republic:** see Austria

**Denmark:** Sydhavnsgade 23, 1780 COPENHAGEN V,  
Tel. +45 33 29 3333, Fax. +45 33 29 3905

**Finland:** Sinikalliontie 3, FIN-02630 ESPOO,  
Tel. +358 9 615 800, Fax. +358 9 6158 0920

**France:** 51 Rue Carnot, BP317, 92156 SURESNES Cedex,  
Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

**Germany:** Hammerbrookstraße 69, D-20097 HAMBURG,  
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

**Hungary:** see Austria

**India:** Philips INDIA Ltd, Band Box Building, 2nd floor,  
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,  
Tel. +91 22 493 8541, Fax. +91 22 493 0966

**Indonesia:** PT Philips Development Corporation, Semiconductors Division,  
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,  
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

**Ireland:** Newstead, Clonskeagh, DUBLIN 14,  
Tel. +353 1 7640 000, Fax. +353 1 7640 200

**Israel:** RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,  
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

**Italy:** PHILIPS SEMICONDUCTORS, Via Casati, 23 - 20052 MONZA (MI),  
Tel. +39 039 203 6838, Fax +39 039 203 6800

**Japan:** Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,  
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5057

**Korea:** Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,  
Tel. +82 2 709 1412, Fax. +82 2 709 1415

**Malaysia:** No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,  
Tel. +60 3 750 5214, Fax. +60 3 757 4880

**Mexico:** 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,  
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

**Middle East:** see Italy

**Netherlands:** Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,  
Tel. +31 40 27 82785, Fax. +31 40 27 88399

**New Zealand:** 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,  
Tel. +64 9 849 4160, Fax. +64 9 849 7811

**Norway:** Box 1, Manglerud 0612, OSLO,  
Tel. +47 22 74 8000, Fax. +47 22 74 8341

**Pakistan:** see Singapore

**Philippines:** Philips Semiconductors Philippines Inc.,  
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,  
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

**Poland:** Al.Jerozolimskie 195 B, 02-222 WARSAW,  
Tel. +48 22 5710 000, Fax. +48 22 5710 001

**Portugal:** see Spain

**Romania:** see Italy

**Russia:** Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,  
Tel. +7 095 755 6918, Fax. +7 095 755 6919

**Singapore:** Lorong 1, Toa Payoh, SINGAPORE 319762,  
Tel. +65 350 2538, Fax. +65 251 6500

**Slovakia:** see Austria

**Slovenia:** see Italy

**South Africa:** S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,  
2092 JOHANNESBURG, P.O. Box 58088 Newville 2114,  
Tel. +27 11 471 5401, Fax. +27 11 471 5398

**South America:** Al. Vicente Pinzon, 173, 6th floor,  
04547-130 SÃO PAULO, SP, Brazil,  
Tel. +55 11 821 2333, Fax. +55 11 821 2382

**Spain:** Balmes 22, 08007 BARCELONA,  
Tel. +34 93 301 6312, Fax. +34 93 301 4107

**Sweden:** Kottbygatan 7, Akalla, S-16485 STOCKHOLM,  
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

**Switzerland:** Allmendstrasse 140, CH-8027 ZÜRICH,  
Tel. +41 1 488 2741 Fax. +41 1 488 3263

**Taiwan:** Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,  
TAIPEI, Taiwan Tel. +886 2 2134 2886, Fax. +886 2 2134 2874

**Thailand:** PHILIPS ELECTRONICS (THAILAND) Ltd.,  
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,  
Tel. +66 2 745 4090, Fax. +66 2 398 0793

**Turkey:** Yukari Dudullu, Org. San. Blg., 2.Cad. Nr. 28 81260 Umraniye,  
ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

**Ukraine:** PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,  
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

**United Kingdom:** Philips Semiconductors Ltd., 276 Bath Road, Hayes,  
MIDDLESEX UB3 5BX, Tel. +44 208 730 5000, Fax. +44 208 754 8421

**United States:** 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,  
Tel. +1 800 234 7381, Fax. +1 800 943 0087

**Uruguay:** see South America

**Vietnam:** see Singapore

**Yugoslavia:** PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,  
Tel. +381 11 62 5344, Fax.+381 11 63 5777

**For all other countries apply to:** Philips Semiconductors,  
International Marketing & Sales Communications, Building BE-p, P.O. Box 218,  
5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

**Internet:** <http://www.semiconductors.philips.com>

© Philips Electronics N.V. 1999

SCA 68

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Printed in The Netherlands

545004/200/01/pp16

Date of release: 1999 Nov 10

Document order number: 9397 750 06196

*Let's make things better.*

**Philips**  
Semiconductors



**PHILIPS**