

DATA SHEET

TDA8012AM

Low power PLL FM demodulator for
satellite TV receivers

Product specification
File under Integrated Circuits, IC02

1997 May 26

Low power PLL FM demodulator for satellite TV receivers

TDA8012AM

FEATURES

- High input sensitivity
- Fully balanced two-pin Voltage Controlled Oscillator (VCO)
- Low input impedance (50 Ω)
- Low impedance video baseband output
- Internal voltage stabilizer
- Keyed Automatic Frequency Control (AFC) or peak AFC
- Carrier detector
- Automatic Gain Control (AGC) output.

GENERAL DESCRIPTION

The TDA8012AM is a sensitive Phase Locked Loop (PLL) Frequency Modulation (FM) demodulator for the second Intermediate Frequency (IF) in satellite receivers. It provides Automatic Gain Control (AGC) and Automatic Frequency Control (AFC) outputs that can be used to optimize the level and the frequency of the signal applied at the input. During the search procedure, the AFC output provides a signal used for carrier detection.

APPLICATIONS

- Digital Broadcast System (DBS) satellite receivers.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		4.75	5.0	5.25	V
I_{CC}	supply current	$V_{CC} = 5\text{ V}; T_{amb} = 25\text{ }^\circ\text{C}$	40	50	60	mA
V_i	input level		53	57	61	dB μ V
f_c	operating carrier frequency		–	480	–	MHz
$V_{o(p-p)}$	video output signal amplitude (peak-to-peak value)	frequency deviation = 25 MHz	–	1	–	V

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8012AM	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

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BLOCK DIAGRAM

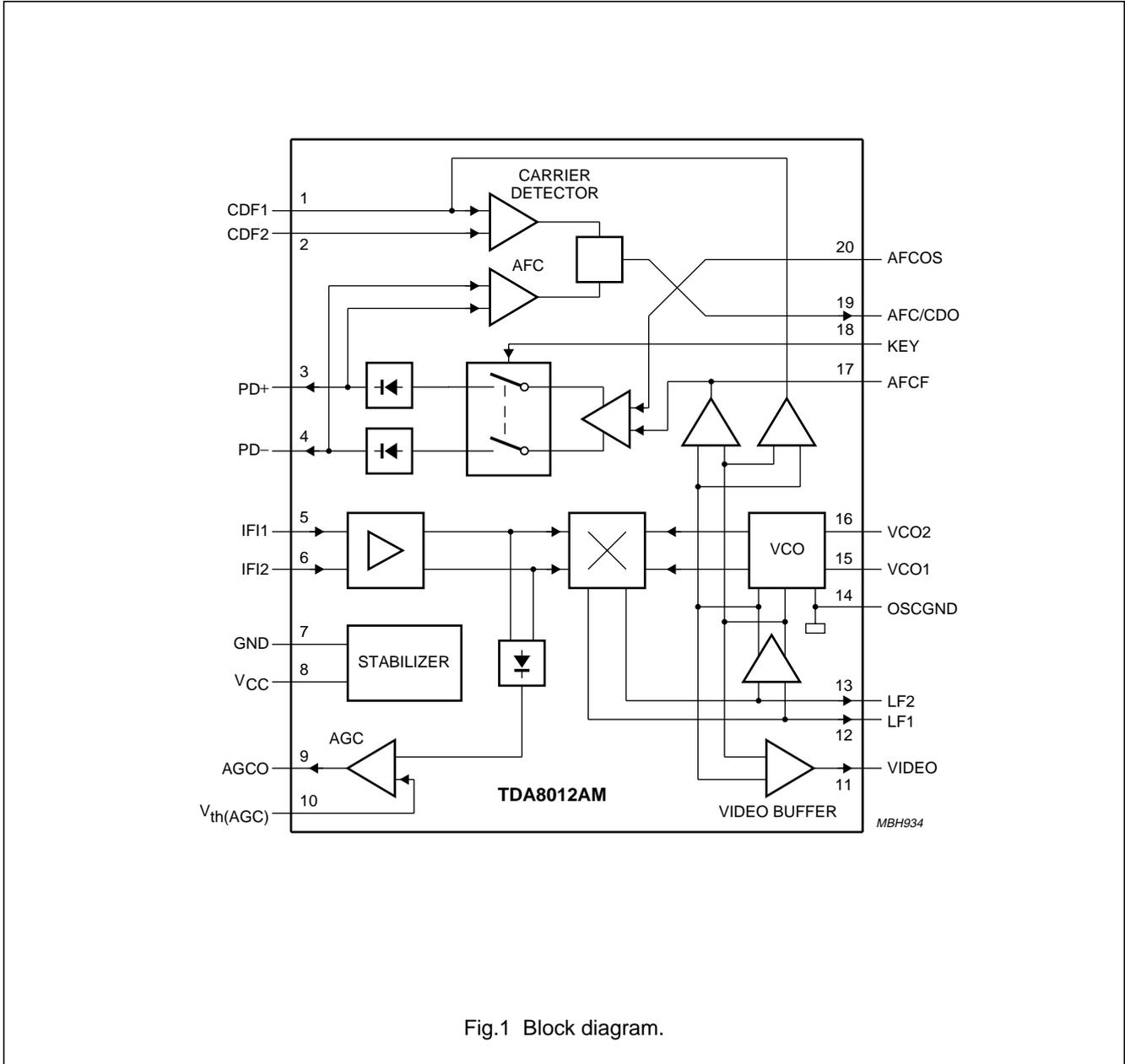


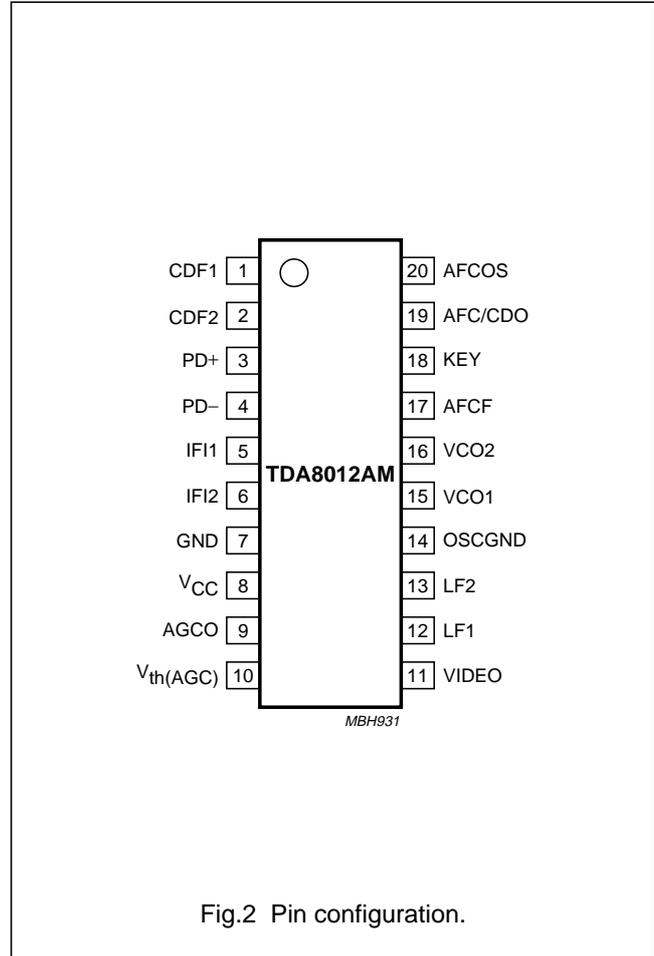
Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
CDF1	1	carrier detector filter 1 input
CDF2	2	carrier detector filter 2 input
PD+	3	positive peak detector output
PD-	4	negative peak detector output
IF1	5	intermediate frequency input 1
IF2	6	intermediate frequency input 2
GND	7	general ground
V _{CC}	8	supply voltage
AGCO	9	automatic gain control output
V _{th(AGC)}	10	automatic gain control threshold voltage input
VIDEO	11	baseband signal output
LF1	12	loop filter 1 input
LF2	13	loop filter 2 input
OSCGND	14	oscillator ground
VCO1	15	oscillator tank circuit 1 input
VCO2	16	oscillator tank circuit 2 input
AFCF	17	automatic frequency control filter input
KEY	18	key pulse input
AFC/CDO	19	automatic frequency control /carrier detector output
AFCOS	20	automatic frequency control offset input



FUNCTIONAL DESCRIPTION

The TDA8012AM is a low power PLL FM demodulator designed for use in satellite TV reception systems.

The demodulator is based on a PLL structure including a fully balanced two-pin VCO. A high gain IF amplifier ensures a high input sensitivity. The video output voltage is supplied through a highly-linear video buffer with a low output impedance. The centre frequency of the VCO and the loop characteristics can be set by external components (see Fig.4).

The circuit provides an AGC signal which is used to drive a gain-controlled IF amplifier (TDA8011T or TDA8010AM) for a stable PLL demodulation characteristic.

An analog AFC voltage is available. This signal fits in with the input of the A/D converter port of the PLL frequency synthesizer (TSA5055). The AFC function may be keyed to address D2MAC systems.

The TDA8012AM includes a Carrier Detector (CD) used for channel detection during search procedures.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	-0.3	+6.0	V
$V_{I(max)}$	voltage on all pins	-0.3	V_{CC}	V
$I_{O(max)}$	output source current	-	10	mA
$t_{sc(max)}$	maximum short-circuit time on outputs	-	10	s
Z_L	AC load impedance at video output	600	-	Ω
T_{stg}	IC storage temperature	-55	+150	$^{\circ}C$
T_j	junction temperature	-	150	$^{\circ}C$
T_{amb}	operating ambient temperature	-10	+80	$^{\circ}C$

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	in free air	120	K/W

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CHARACTERISTICS

Measured in the application circuit (see Fig.4) with the following conditions: $V_{CC} = 5\text{ V}$, $T_{amb} = 25\text{ }^{\circ}\text{C}$, $f_c = 480\text{ MHz}$, input level: 57 dB μV ; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CC}	supply voltage		4.75	5.0	5.25	V
I_{CC}	supply current	note 1	40	50	60	mA
Voltage controlled oscillator						
K_{VCO}	VCO constant	$4.75 < V_{CC} < 5.25\text{ V}$; $-10 < T_{amb} < 80\text{ }^{\circ}\text{C}$	20	25	30	MHz/V
$\Delta f_{VCO(\text{drift})}$	VCO frequency temperature dependence	note 2	–	1	2.5	MHz
$\Delta f_{VCO(\text{shift})}$	VCO frequency voltage dependence	$4.75 < V_{CC} < 5.25\text{ V}$	–	± 300	± 750	kHz
Frequency demodulator						
V_i	operating input level	note 3	53	57	61	dB μV
f_c	optimal operating carrier frequency		–	480	–	MHz
Z_i	input impedance	note 4				
	resistive part		–	50	–	Ω
	inductive part		–	100	–	nH
K_D	phase detector constant	$V_i = 57\text{ dB}\mu\text{V}$	–	0.42	–	V/rad
L_G	PLL loop gain	note 5				
	drift		–	2	–	dB
	shift		–	2	–	dB
Z_o	differential output impedance of the phase detector		1.8	2.3	2.8	k Ω
$f_{cr(\text{PLL})}$	PLL capture range	note 6	± 20	± 26	–	MHz
D_G	differential gain	note 7	–	± 2	–	%
D_P	differential phase	note 7	–	± 2	–	deg
IM3	third-order intermodulation distortion	note 8	47	–	–	dB
IM2	second-order intermodulation distortion	note 9	45	–	–	dB
Video output						
$V_{o(p-p)}$	baseband signal amplitude (peak-to-peak value)	frequency deviation = 25 MHz	0.8	1.0	1.2	V
V_O	DC voltage level of video output		2.1	2.35	2.6	V
Z_o	output impedance		–	75	–	Ω
S/N	weighted baseband signal-to-noise ratio	note 10	58	61	–	dB
S_{AM}	Amplitude Modulation (AM) sensitivity	note 11	–	30	–	dB

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Automatic gain control (note 12)						
TH _{AGC}	automatic gain control threshold as a function of the voltage applied to pin 10	I _{AGCO} = 0.5 mA; V ₁₀ = 0.1V _{CC}	–	–	53	dB μ V
		I _{AGCO} = 0.5 mA; V ₁₀ = 0.9V _{CC}	61	–	–	dB μ V
	note 13	V _{th(AGC)} (pin 10) not connected	–	57	–	dB μ V
LD	level detector					
	shift drift	V _{CC} = 4.75 to 5.25 V T _{amb} = –10 to +80 °C	– –	1 1	– –	dB dB
S _{AGC}	automatic gain control steepness	I _{AGCO} = 0.5 mA; note 14	–	8	–	mA/dB
V _{sat(AGC)}	low level automatic gain control output saturation voltage	I _{AGCO} = 1 mA	–	200	500	mV
Keying pulse						
t _{key}	input keyed pulse time period		–	64	–	μ s
t _{W(key)}	keyed pulse width		8	–	–	μ s
V _{IL}	LOW level input keyed pulse voltage	key on	–	–	0.8	V
V _{IH}	HIGH level input keyed pulse voltage	key off	3.0	–	–	V
Z _i	input impedance		1	10	–	k Ω
AFC and carrier detector output (note 15)						
I _{L(pd)}	peak detector leakage current	note 16	50	150	250	nA
$\frac{\Delta V_{AFC}}{\Delta f}$	automatic frequency control steepness with unmodulated input signal		4.5	5.5	6.5	V/MHz
$\Delta f_{AFC(\text{shift})}$	shift of automatic frequency control voltage with respect to f _{VCO} with unmodulated 480 MHz input signal	$\Delta V_{CC} = \pm 5\%$	–	± 180	± 500	kHz
$\Delta f_{AFC(\text{drift})}$	drift of automatic frequency control voltage with respect to f _{VCO}	T _{amb} = 80 °C; note 17	–	–1.1	–	MHz

Notes

- The DC supply current is measured with V_{CC} = 5 V.
- The VCO frequency drift is defined as the change in oscillator frequency for a variation of ambient temperature, on the one hand from T_{amb} = 25 °C to T_{amb} = 0 °C and on the other hand from T_{amb} = 25 °C to T_{amb} = 50 °C. It is measured in the application of Fig.4 with the following component values for the tank circuit:
Coil: 2.5 turns; diameter 2 mm; adjustable.
Capacitor: miniature ceramic plate capacitor NP0, 3.3 pF.
- The circuit is designed for an input level of 57 dB μ V. The maximum allowable input level for the PLL design is 61 dB μ V. However, for levels different from 57 dB μ V, the optimum loop filter values will be different from those given for the 57 dB μ V input level in the reference measuring set-up.
- The input impedance is reduced to a resistor with a parallel reactance. The values are given at 480 MHz. In order to reduce the radiation from the oscillator to the RF input, it is recommended to use a symmetrical drive.
- The PLL loop gain shift and drift are given without loop filter shift and drift (non-temperature compensated external components).

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6. The capture range or lock-in range is defined as the range where the PLL gets in lock. This value depends strongly on the loop filter characteristics.
7. Measurements with test signals in accordance with CCIR recommendation 473-3; FM modulated signal with DBS parameters:
 - a) 625 lines PAL TV system
 - b) 16 MHz/V modulator sensitivity
 - c) 1 V (p-p) video signal
 - d) No SAW filter is used.
8. No SAW filter is used at the input:
 - a) 16 MHz/V modulator sensitivity
 - b) 4.43 MHz sine wave colour signal (660 mV (p-p))
 - c) 3.25 MHz sine wave luminance signal (700 mV (p-p))
 - d) CCIR pre-emphasis
 - e) Intermodulation distance is defined as the distance between the luminance signal and the intermodulation products. The video output spectrum is measured on pin 11 (point A of Fig.4) with a high resistance probe. The de-emphasis figure is obtained from the measured data by calculation.
9. No SAW filter is used at the input:
 - a) 16 MHz/V modulator sensitivity
 - b) Two sound carriers at 7.02 MHz and 7.20 MHz; 4 MHz deviation
 - c) Intermodulation measurement without pre-emphasis
 - d) Intermodulation distance is defined as the distance between one of the sound carriers and the intermodulation products
 - e) The video output spectrum is measured on pin 11 (point A of Fig.4) with a high resistance probe and a spectrum analyser.
10. Measurements are made under the following conditions
 - a) FM modulator video signal
 - b) Amplitude level: 57 dB μ V
 - c) Frequency: 479.5 MHz
 - d) Frequency deviation: 16 MHz
 - e) CCIR pre-emphasis + unified weighting filter
 - f) C/N > 50 dB
S/N is measured after de-emphasis with a baseband spectrum from 200 kHz to 5 MHz.
11. The AM sensitivity is defined as the ratio of the baseband output signals obtained from either an AM or FM modulated RF input signal.

$$S_{AM} = 20 \log \frac{V_{o(FM)}}{V_{o(AM)}}$$

FM modulated signal: $f_c = 480$ MHz, frequency deviation = 25 kHz, modulation frequency = 20 kHz, input level = 57 dB μ V
 AM modulated signal: $f_c = 480$ MHz, modulation depth = 50%, modulation frequency = 20 kHz, input level = 57 dB μ V.
12. The characteristics of the AGC function are measured in the application circuit of Fig.4. The circuit illustrated in Fig.4 has been designed to set the maximum AGC current to 1 mA. The output of the AGC function is capable of handling up to 5 mA. The maximum AGC current can be increased to 5 mA by decreasing the value of the resistor connected between pins 8 and 9.

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13. For applications in which a fixed AGC threshold is used, it is recommended to use the internal resistor voltage divider for lower AGC threshold spread. In this case, the threshold is set to 57 dB μ V.
14. In the application circuit (see Fig.4) the voltage at the AGC output decreases when the IF input level increases above the adjusted AGC threshold.
15. The outputs from the AFC and carrier detector are combined at pin 19 (see Fig.3). During search tuning, when the input frequency is outside the capture range, the combined output (carrier detector function) is at a LOW level (any voltage below 0.6V_{CC}). When the PLL becomes locked, the voltage at pin 19 rises to a HIGH level (V₁₉ = 0.8V_{CC} to V_{CC}). When the input channel is close to the centre frequency, V₁₉ falls to the LOW level. As shown in Fig.3, the voltage at pin 19 is now a function of the centre frequency (AFC function). This information may be read by a microcontroller via the ADC of the satellite frequency synthesizer (TSA5055) and the I²C-bus.
16. This current discharges the external capacitors between two energy dispersal peak values and avoid the use of external resistors in parallel with capacitors.
17. The drift of the automatic frequency control voltage is measured in accordance with the following method:
 - a) At room temperature (T_{amb} = 25 °C) the TDA8012AM is driven by a 480 MHz unmodulated signal. The voltage at pin 20 must be adjusted to obtain a 1.5 V output at the AFC output (pin 19).
 - b) At T_{amb} = 80 °C, due to its temperature drift, the AFC output voltage differs from 1.5 V. The input frequency must be adjusted to obtain 1.5 V at the AFC output. Then the VCO frequency f_{VCO} is measured in free running mode (without input signal). The drift of the automatic frequency control voltage will then be equal to the difference between the input frequency and f_{VCO}.

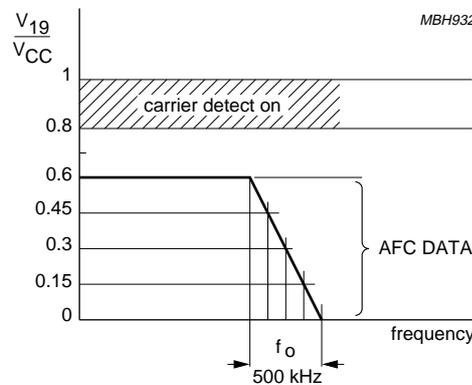
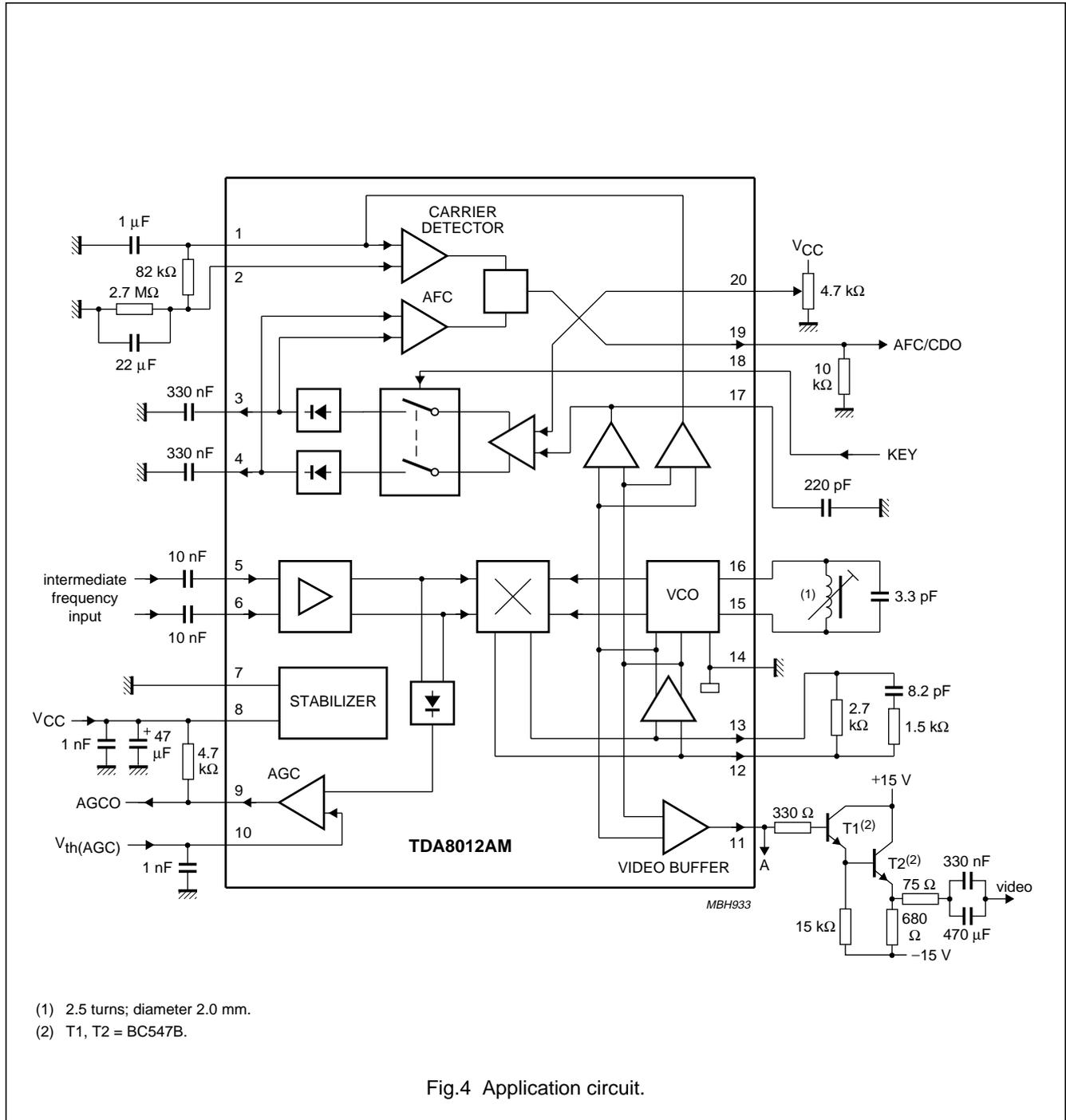


Fig.3 AFC and carrier detector output.

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APPLICATION INFORMATION



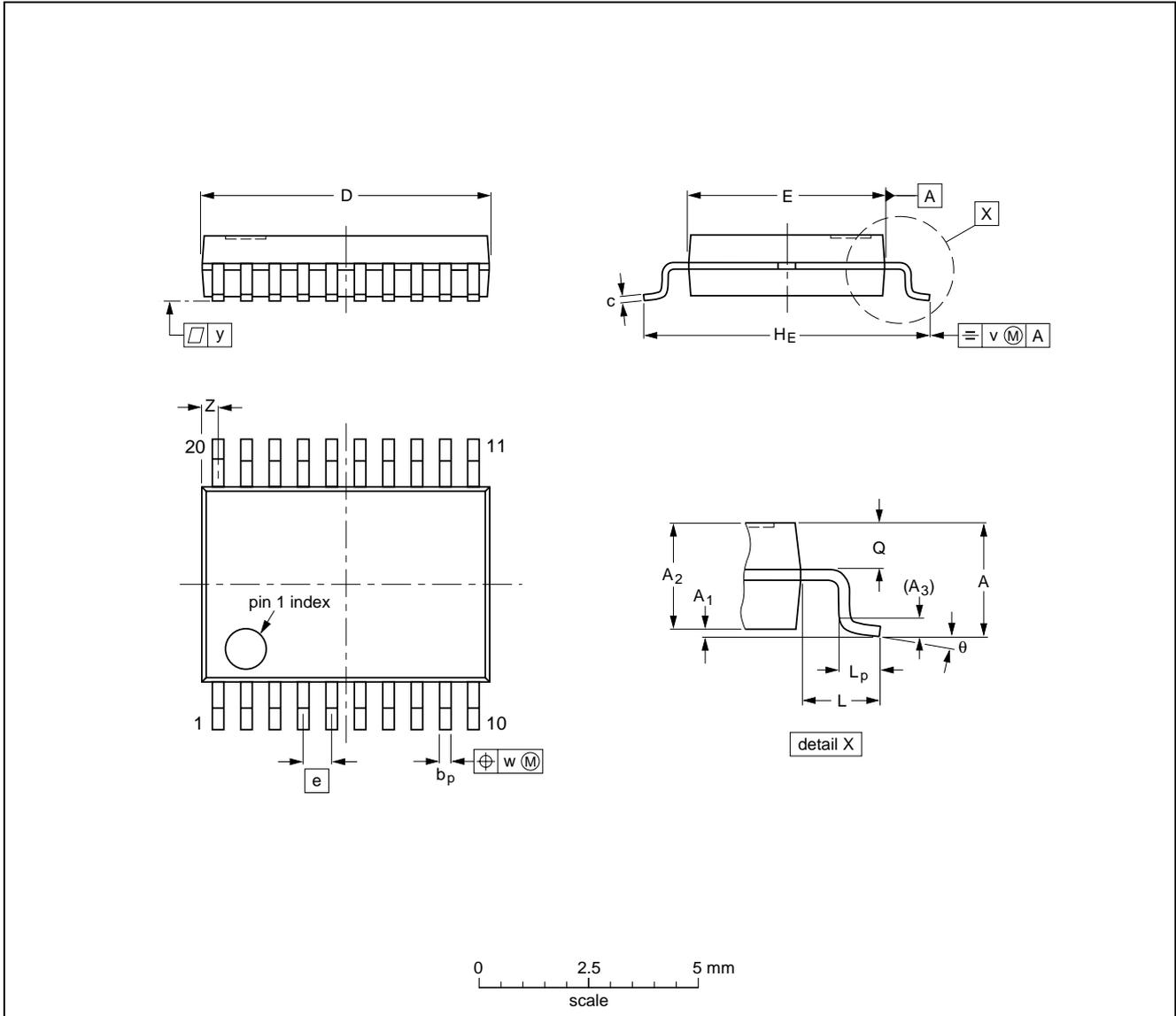
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PACKAGE OUTLINE

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm

SOT266-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.5	0.15 0	1.4 1.2	0.25	0.32 0.20	0.20 0.13	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT266-1						90-04-05 95-02-25

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SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "*IC Package Databook*" (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for SSOP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.**

Even with these conditions, only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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NOTES

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NOTES

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