

CAR RADIO SIGNAL PROCESSOR

PRODUCT PREVIEW

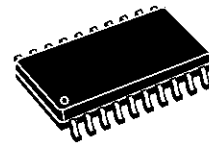
- DEVICE INCLUDES AUDIO PROCESSOR, STEREO DECODER, NOISEBLANKER AND HIGHCUT FUNCTIONS.
- HIGH PERFORMANCE SIGNAL PROCESSOR
- NO EXTERNAL COMPONENTS REQUIRED
- FULLY PROGRAMMABLE VIA I²C BUS
- LOW DISTORTION
- LOW NOISE

DESCRIPTION

The TDA7460 is a high performance signal processor specifically designed for car radio applications.

The device includes a complete audioprocessor and a stereo decoder with noiseblanker, stereoblend and all signal processing functions necessary for state-of-the-art as well as future car radio systems.

Switching-capacitors design technique allows to obtain all these features without external compo-

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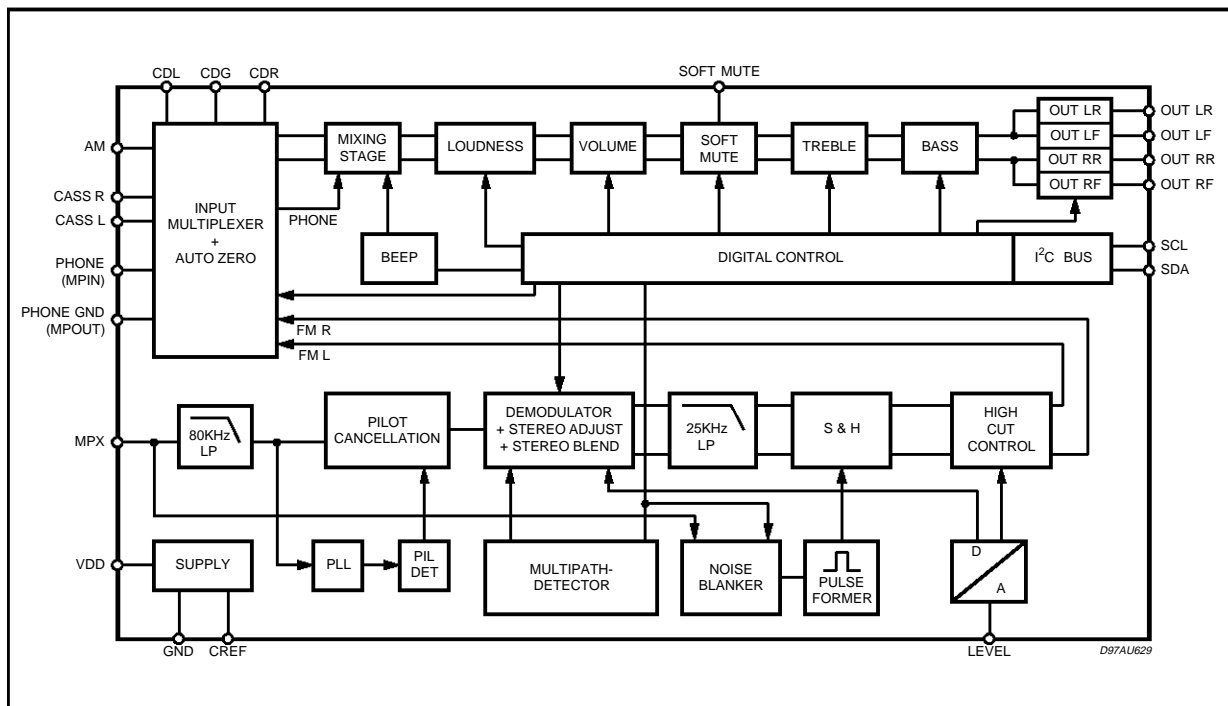
ORDERING NUMBER: TDA7460D

nents or adjustments. This means that higher quality and reliability walks alongside an overall cost saving.

The CSP is fully programmable by I2C bus interface allowing to customize key device parameters and especially filter characteristics.

The BICMOS process combined with the optimized signal processing assure low noise and low distortion performances.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _S	Operating Supply Voltage	10.5	V
T _{amb}	Operating Ambient Temperature Range	-40 to 80	°C
T _{stg}	Operating Storage Temperature Range	-55 to 150	°C

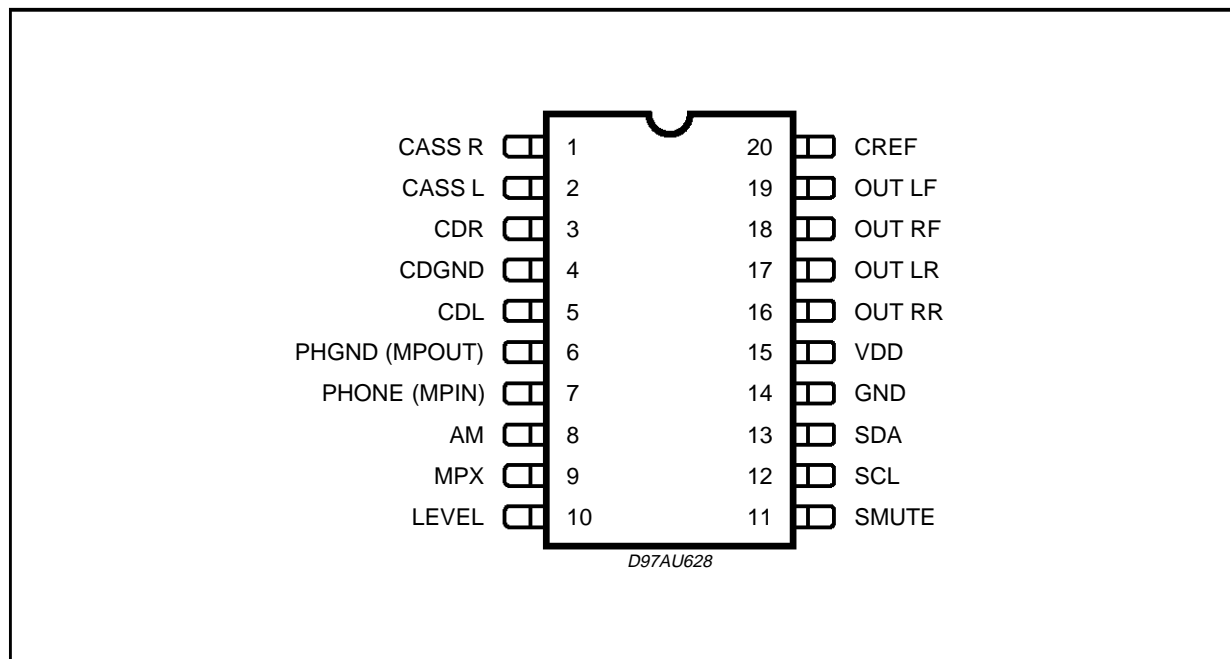
Supply

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V _S	Supply Voltage		7.5	9	10	V
I _S	Supply Current	V _S = 9V		30		mA
SVRR	Ripple Rejection @ 1KHz	Audioprocessor (all filters flat)		60		dB
		Stereodecoder + Audioprocessor		55		dB

ESD

All pins are protected against ESD according to the MIL883 standard.

PIN CONNECTION



THERMAL DATA

Symbol	Parameter	Value	Unit
R _{th j-pins}	Thermal Resistance Junction-pins Max	85	°C/W

AUDIO PROCESSOR PART**Input Multiplexer**

- Fully differential or quasi-differential CD Stereo input
- Cassette stereo input
- AM mono or stereo input
- Phone differential or single ended input
- Internal beep with 2 frequencies (selectable)
- Mixable phone and beep signals

Loudness

- Second order frequency response
- Programmable center frequency and quality factor
- Selectable flat-mode (constant attenuation)

Volume control

- 1dB attenuator
- Max. gain 20dB
- Max. attenuation 79dB
- Soft-step gain control

Bass Control

- 2nd order frequency response
- Center frequency programmable in 4(5) steps
- DC gain programmable
- 7 x 2dB steps

Treble Control

- 2nd order frequency response
- Center frequency programmable in 4 steps
- 7 x 2dB steps

Speaker Control

- 4 independent speaker controls (1dB steps with 50dB control range)

Mute Functions

- Direct mute
- Digitally controlled softmute with 4 programmable time constants

ELECTRICAL CHARACTERISTICS ($V_S = 9V$; $T_{amb} = 25^\circ C$; $R_L = 10K\Omega$; all gains = 0dB; $f = 1KHz$; unless otherwise specified).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
INPUT SELECTOR						
R _{in}	Input Resistance	All inputs except Phone		100		KΩ
V _{CL}	Clipping Level			2.6		V _{RMS}
S _{IN}	Input Separation		80	100		dB
G _{IN MIN}	Min. Input Gain		-1	0	1	dB
G _{IN MAX}	Max. Input Gain			14		dB
G _{STEP}	Step Resolution			2		dB
V _{DC}	DC Steps	Adjacent Gain Step		2		mV
		G _{MIN} to G _{MAX}		6		mV
DIFFERENTIAL CD STEREO INPUT						
R _{in}	Input Resistance	Differential mode	70	100	130	KΩ
		Common Mode	20	30	40	KΩ
CMRR	Common Mode Rejection Ratio	V _{CM} = 1V _{RMS} @ 1KHz	45	70		dB
		V _{CM} = 1V _{RMS} @ 10KHz	45	60		dB
G _{IN MAX}	Max. Input Gain	20Hz to 20KHz flat; all stages 0dB		9		μV
DIFFERENTIAL PHONE INPUT						
R _{in}	Input Resistance	Differential	10	15	20	KΩ
		Common Mode	20	30	40	KΩ
CMRR	Common Mode Rejection Ratio	V _{CM} = 1V _{RMS} @ 1KHz	45	70		dB
		V _{CM} = 1V _{RMS} @ 10KHz	45	60		dB

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
BEEP CONTROL						
V _{RMS}	Beep Level			350		mV
f _{BMIN}	Lower Beep Frequency			600		Hz
f _{BMAN}	Higher Beep Frequency			1.2		KHz
MIXING CONTROL						
M _{LEVEL}	Mixing Level	Source		0		dB
		Source		-6		dB
		Source		-12		dB
		Beep/Phone		0		dB
VOLUME CONTROL						
G _{MAX}	Max Gain			20		dB
A _{MAX}	Max Attenuation			79		dB
A _{STEP}	Step Resolution			1		dB
E _A	Attenuation Set Error	G = -20 to 20dB	-1.25	0	1.25	dB
		G = -60 to 20dB	-4	0	3	dB
E _T	Tracking Error				2	dB
V _{DC}	DC Steps	Adjacent Attenuation Steps		0.1	3	mV
		From 0dB to G _{MIN}		0.5	5	mV
LOUDNESS CONTROL						
A _{STEP}	Step Resolution			1		dB
A _{MAX}	Max. Attenuation			15		dB
f _{CMIN}	Lower Center Frequency			200		Hz
f _{CMAX}	Higher Center Frequency			400		Hz
SOFT MUTE						
A _{MUTE}	Mute Attenuation		80	100		dB
T _D	Delay Time	T ₁		0.48		ms
		T ₂		0.96		ms
		T ₃		40.4		ms
		T ₄		324		ms
V _{THlow}	Low Threshold for SM-Pin ¹				1	V
V _{THhigh}	High Threshold for SM - Pin		2.5			V
R _{PD}	Internal Pull-up Resistor			100		KΩ
SOFT STEP						
T _{SW}	Switch Time			10		ms

1) The SM pin is active low (Mute = 0)

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
BASS CONTROL						
CRANGE	Control Range			±14		dB
ASTEP	Step Resolution			2		dB
fc	Center Frequency	fc1		60		ms
		fc2		70		ms
		fc3		80		ms
		fc4		100		Hz
QBASS	Quality Factor	Q1		1		
		Q2		1.25		
		Q3		1.5		
		Q4		2		
DCGAIN	Bass-Dc-Gain	DC = off		0		dB
		DC = on		4.4		dB
TREBLE CONTROL						
CRANGE	Control Range			±14		dB
ASTEP	Step Resolution			1		dB
fc	Center Frequency	fc1		10		KHz
		fc2		12.5		KHz
		fc3		15		KHz
		fc4		17.5		KHz
SPEAKER ATTENUATORS						
CRANGE	Control Range			50		dB
ASTEP	Step Resolution			1		dB
AMUTE	Output Mute Attenuation		80	90		dB
EE	Attenuation Set Error				2	dB
VDC	DC Steps	Adjacent Attenuation Steps		0.1	5	mV
AUDIO OUTPUTS						
VCLIP	Clipping Level	d = 0.3%	2.2	2.6		V _{RMS}
RL	Output Load Resistance		2			KΩ
CL	Output Load Capacitance				10	nF
ROUT	Output Impedance			30	120	Ω
VDC	DC Voltage Level			3.8		V
GENERAL						
eno	Output Noise	BW = 20 Hz to 20 KHz output muted		3		μV
		BW = 20 Hz to 20 KHz all gain = 0dB		6.5		μV
S/N	Signal to Noise Ratio	all gain = 0dB flat; V _O = 2V _{RMS}		110		dB
		Bass & Treble at 12dB; a-weighted; V _O = 2.6V _{RMS}		100		dB
d	Distortion	V _{IN} = 1V _{RMS} ; all stages 0dB		0.002	0.05	%
		V _{IN} = 1V _{RMS} ; Bass & Treble = 12dB		0.05		%
Sc	Channel separation Left/Right		80	100		dB
ET	Total Tracking Error	A _V = 0 to -20dB		0	1	dB
		A _V = -20 to -60dB		0	2	dB

2) See description of Audioprocessor Part

DESCRIPTION OF THE AUDIOPROCESSOR PART

Programmable Input-matrix

The programmable input matrix of the TDA7460 offers several possibilities to adapt the Audioprocessor to the desired application. In addition to the standard application we have:

- CD quasi differential
- Cassette stereo
- Phone differential
- AM mono
- Stereodecoder input.

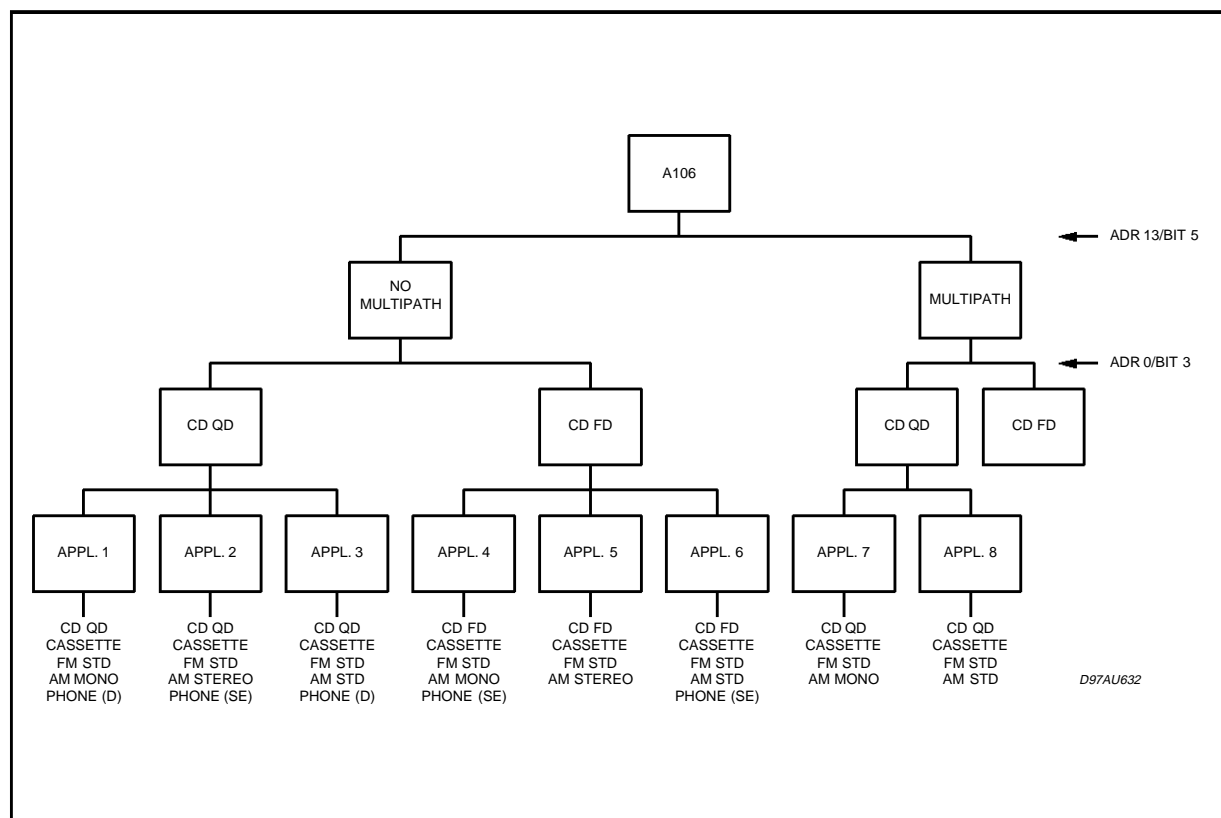
The input matrix can be configured by only 3 bits:

bits 3+4 of subaddress 0 and Bit 5 of subaddress 13. Basically the bit of subaddress 13 is fixed by the application and has to be programmed only once at the startup of the IC.

For many configurations the two other bits are also fixed during one application (e.g. the standard application) and a change of the input source can be done by loading the first three bits of subaddress 0 (0/xxxxxxx??).

In the other configurations for some sources a programming of bit 3+4 of subaddress 0 is necessary in addition to the three source selection bits. In every case only the subaddress 0 has to be changed to switch from one source to another. The following table shows the input and source programming for all applications:

Figure 1. Input Configuration Tree



Appl. No	PIN NUMBER				Programming	
	4 (CD _{GND})	6 (Phone _{GND})	7 (Phone)	8 (AM)		
1	CD _{GND}	Phone _{GND}	Phone	AM _{mono}	Startup:	0/xxx11xxx ¹ 13/xx1xxxxx
2	CD _{GND}	Phone	AMR	AML	Startup:	13/xx1xxxxx
					FM	0/xxx11100
					AM	0/xxx01011
3	CD _{GND}	Phone _{GND}	Phone	AMSTD	Phone	0/xxx11010
					Startup:	13/xx1xxxxx
					FM	0/xxx11100
4	CD _{GND}	Phone _{GND}	AMR	AML	AM	0/xxx01100
					Phone	0/xxx11010
					Startup:	13/xx1xxxxx
5	CD _{GND}	Phone _{GND}	AMR	AML	Startup:	0/xxx10xxx 13/xx1xxxxx
					FM	0/xxx0xxx 13/xx1xxxxx
					AM	0/xxx10100
6	CD _{GND}	Phone _{GND}	AMR	AML	Phone	0/xxx00011
					Startup:	0/xxx0xxx 13/xx1xxxxx
					FM	0/xxx10100
7	CD _{GND}	Phone _{GND}	AMR	AML	AM	0/xxx00100
					Phone	0/xxx10010
					Startup:	0/xxx0xxx 13/xx1xxxxx
8	CD _{GND}	Phone _{GND}	AMR	AML	Startup:	0/xxx11xxx 13/xx0xxxxx
					FM	0/xxx11xxx 13/xx0xxxxx
					AM	0/xxx11100
					Phone	0/xxx01100

¹ Syntax 0/xxx11100 means: SUBADDRESS = 0 - DATA BYTE = xxx11100 (x - don't care)

How to find the right application

The best way to come to the desired application may be to go through the application tree from the top to the bottom while making the specific decisions.

This way will lead to one of the eight possible applications. Then take the number of the application and go into the pinning table. Here you will find the special pinout as well as the special programming codes for selecting sources.

For example in Appl. 6 the TDA7460 has to be configured while startup with the DATA-BYTE 13/xx11xxxx.

To select the FM, AM or Phone source the last five significant bits of subaddress 0 have to be changed, for any other source the last three bits will sufficient (see data byte specification).

Input stages

Most of the input stages have remained the same as in preceding ST Audioprocessors with exception of the CD inputs (see Figure 2).

In the meantime there are some CD players in

the market which have a significant high source-impedance which affects strongly the common-mode rejection of the normal differential input stage. The additional buffer of the A106 CD input avoids this drawback and offers the full common-mode-rejection even with those CD players.

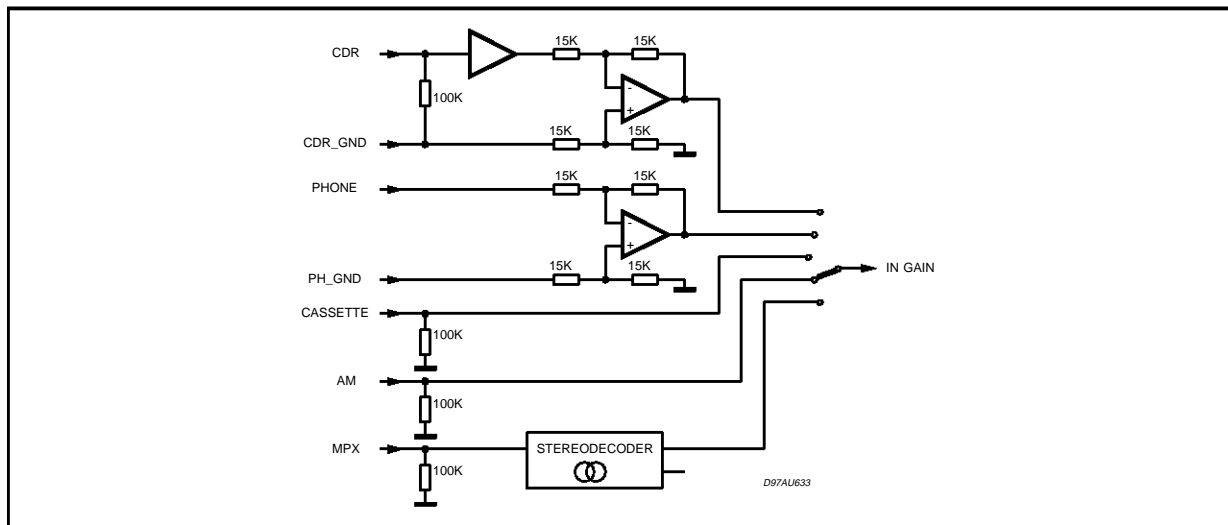
AutoZero

In order to reduce the number of pins there is no AC coupling between the In-Gain and the following stage, so that any offset generated by or before the In-Gain stage would be transferred or even amplified to the output.

To avoid that effect a special offset cancellation stage called AutoZero is implemented. This stage is located before the mixing block to eliminate all offsets generated by the Stereodecoder, the Input stages and the In Gain

To avoid audible clicks the audioprocessor is muted before the loudness stage during this time. In some cases, for example if the μP is executing a refresh cycle of the I2C bus programming, it is not useful to start a new AutoZero action because no new source is selected and an undesired mute would appear at the outputs. For such applica-

Figure 2. Input stages



tions the TDA7460 could be switched in the "AutoZeroRemain" mode (Bit 6 of the subaddress byte). If this bit is set to high, the DATABYTE 0 could be loaded without invoking the AutoZero and the old adjustment value remains.

Mixing Stage

This stage offers the possibility to mix the internal beep or the phone signal to any other source. Due to the fact that the mixing stage is also located behind the In-Gain stage fine adjustments of the main source level can be done in this way.

Loudness

There are four parameters programmable in the loudness stage (see fig. 3, 4, 5):

- Attenuation
- Center Frequency
- Loudness Q
- Flat Mode: in flat mode (1/xxx1xxxx) the loudness stage works as a 0dB - 15dB attenuator.

Softmute

The digitally controlled softmute stage allows muting/demuting the signal with a I2C bus programmable slope. The mute process can either be activated by the softmute pin or by the I2C bus. The slope is realized in a special S shaped curve to mute slow in the critical regions (see Figure 5).

For timing purposes the Bit 3 of the I2C bus output register is set to 1 from the start of muting until the end of demuting.

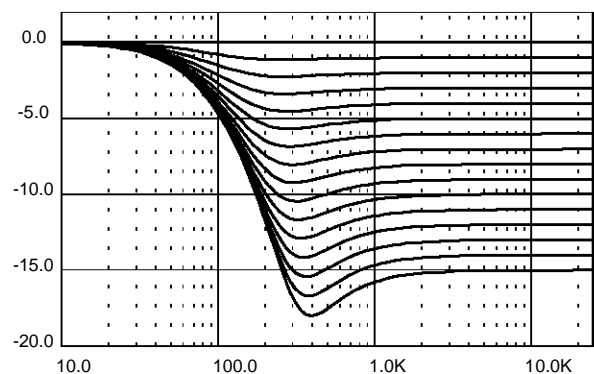
Figure 3. Loudness Attenuation @ $f_c = 400\text{Hz}$ 

Figure 4. Loudness Center frequency @ Attn. = 15dB

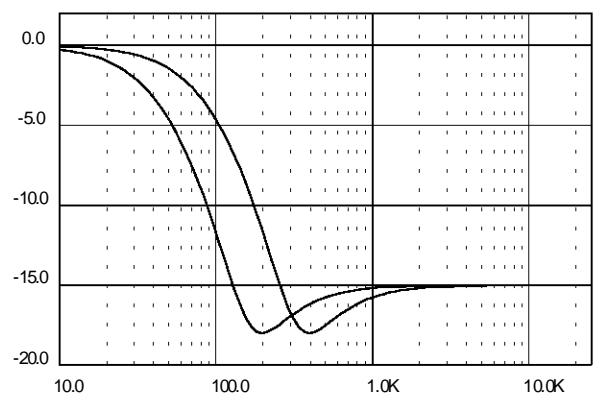
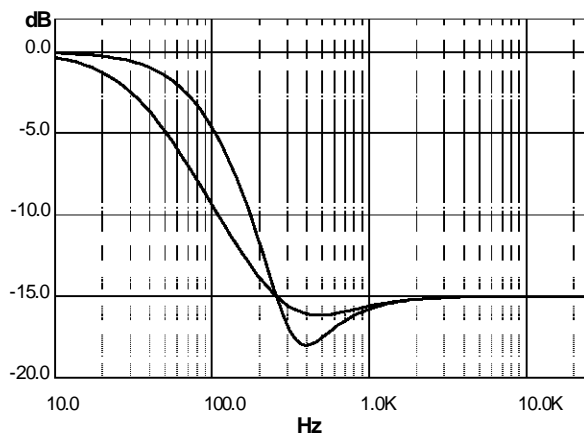


Figure 5. Loudness Q @ Attn. = 15dB, fc = 400Hz



Softstep Volume

When volume level is changed often an audible click appears at the output. The root cause of those clicks could be either a DC offset before the volume stage or the sudden change of the envelope of the audiosignal. With the SoftStep feature both kinds of clicks could be reduced to a minimum and are no more audible.

Bass

There are three parameters programmable in the bass stage (see figs 8, 9, 10, 11):

- Attenuation
- Center Frequency (60, 70, 80 and 100Hz)
- Quality Factors (1, 1.25, 1.5 and 2)

DC Mode

In this mode the DC gain is increased by 5.1dB. In addition the programmed center frequency and quality factor is decreased by 25% which can be used to reach alternative center frequencies or quality factors.

Treble

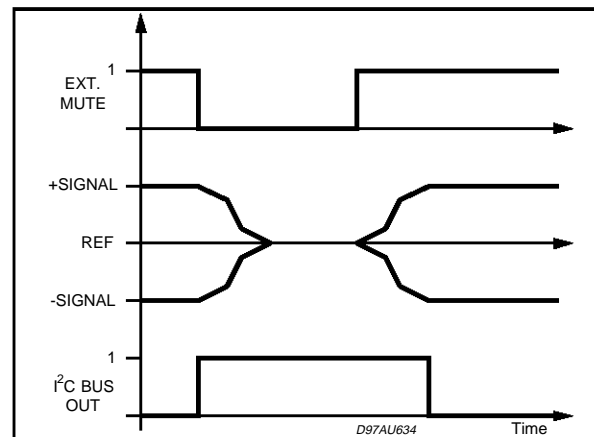
There are two parameters programmable in the treble stage (see figs 12, 13):

- Attenuation
- Center Frequency (10, 12.5, 15 and 17.5kHz).

Speaker Attenuator

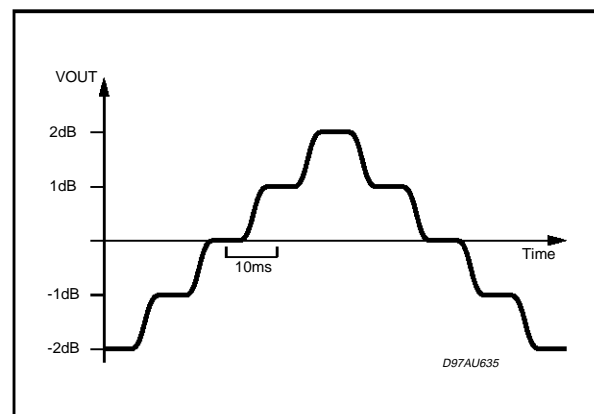
Due to practical aspects the steps in the speaker attenuators are not linear over the full range. At attenuations more than 24dB the steps increase from 1.5dB to 10dB (please see data byte specification).

Figure 6. Softmute Timing

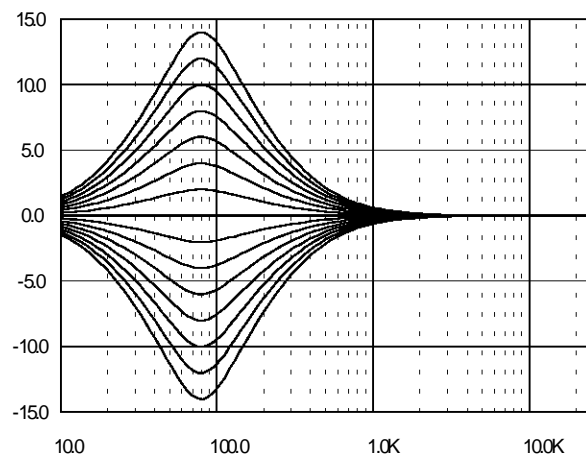
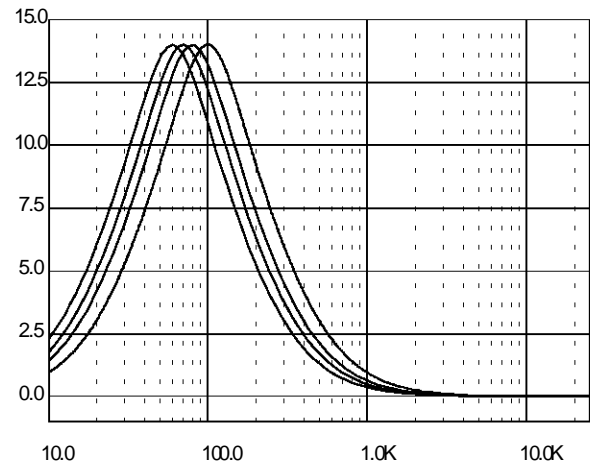
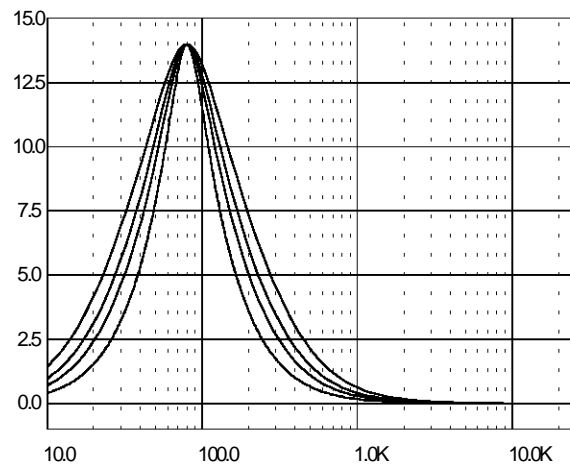
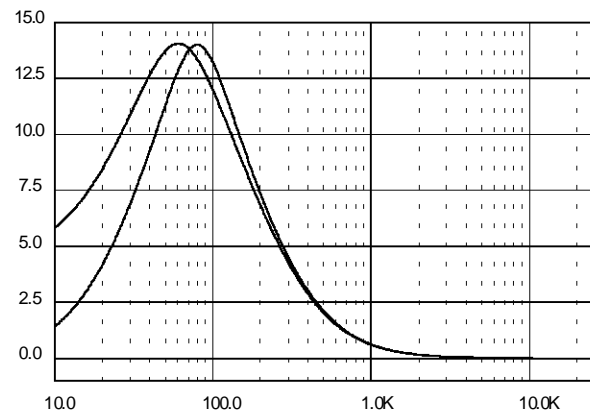


Note: Please notice that a Mute action is always terminated and could not be interrupted by a change of the mute signal.

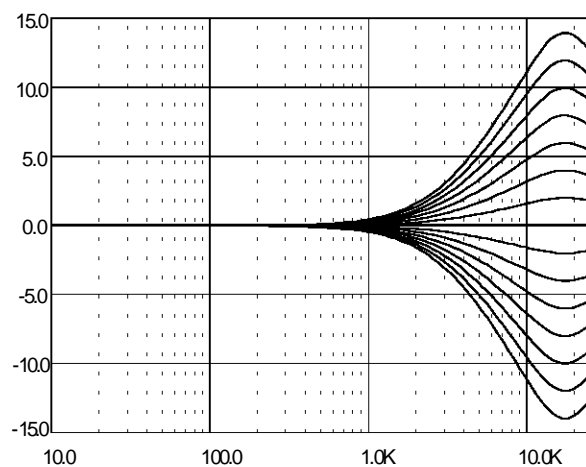
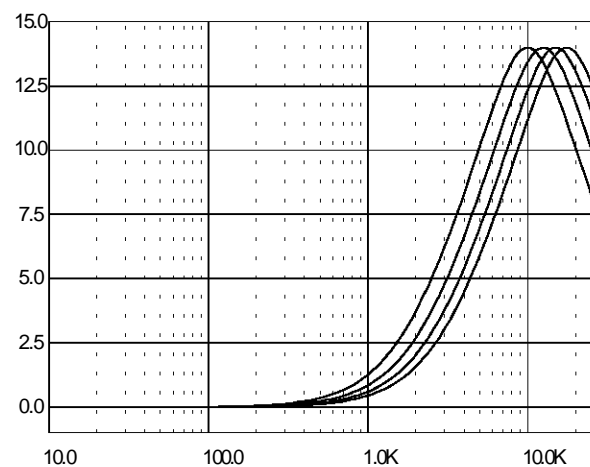
Figure 7. Soft Step Timing



Note: For steps more than 1dB the softstep mode should be deactivated because it could generate a 1dB error during the blend time

Figure 8. Bass Control @ $f_c = 80\text{Hz}$, $Q = 1$ **Figure 9. Bass Center @ Gain = 14dB, $Q = 1$** **Figure 10. Bass Quality factors @ Gain = 14dB, $f_c = 80\text{Hz}$** **Figure 11. Bass normal and DC Mode @ Gain = 14dB, $f_c = 80\text{Hz}$** 

Note: In general the center frequency, Q and DC-mode can be set independently. The exception from this rule is the mode (5/xx1111xx) where the center frequency is set to 150Hz instead of 100Hz.

Figure 12. Treble Control @ $f_c = 17.5\text{KHz}$ **Figure 13. Treble Center Frequencies @ Gain = 14dB**

STEREODECODER PART

- No external components necessary
- PLL with adjustment free fully integrated VCO
- Automatic pilot dependent MONO/STEREO switching
- Very high suppression of intermodulation and interference
- Programmable Roll-Off compensation
- dedicated RDS Softmute
- Highcut and Stereoblend characteristics programmable in a wide range
- Internal Noiseblanker with threshold controls
- Multipath detector with programmable internal/external influence
- I²C bus control of all necessary functions

ELECTRICAL CHARACTERISTICS ($V_s = 9V$; deemphasis time constant = $50\mu s$, $V_{MPX} = 500mV$ (75KHz deviation), $f = 1KHz$. $G_I = 6dB$, $T_{amb} = 25^\circ C$; unless otherwise specified).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IN}	MPX Input Level	Input Gain = 3.5dB		0.5	1.25	V_{RMS}
R_{in}	Input Resistance			100		$K\Omega$
G_{min}	Minimum Input Gain			3.5		dB
G_{max}	Max Input Gain			11		dB
G_{STEP}	Step Resolution			2.5		dB
SVRR	Supply Voltage Ripple Rejection	$V_{ripple} = 100mV$, $f = 1kHz$		60		dB
α	Max Channel Separation			50		dB
THD	total Harmonic Distortion			0.02	0.3	%
$\frac{S+N}{N}$	Signal plus Noise to Noise Ratio	A-weighted, $S = 2V_{rms}$		91		dB

MONO/STEREO SWITCH

V_{PTHST1}	Pilot Threshold Voltage	for Stereo, PTH = 1		15		mV
V_{PTHST0}	Pilot Threshold Voltage	for Stereo, PTH = 0		25		mV
V_{PTHMO1}	Pilot Threshold Voltage	for Mono, PTH = 1		12		mV
V_{PTHMO0}	Pilot Threshold Voltage	for Stereo, PTH = 0		19		mV

PLL

$\Delta f/f$	Capture Range		0.5			%
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DEEMPHASIS and HIGHCUT

τ_{HC50}	Deemphasis Time Constant	Bit = 7, Subadr. 10 = 0 $V_{LEVEL} \gg V_{HCH}$		50		μs
τ_{HC75}	Deemphasis Time Constant	Bit = 7, Subadr. 10 = 1 $V_{LEVEL} \gg V_{HCH}$		75		μs
τ_{HC50}	Highcut Time Constant	Bit = 7, Subadr. 10 = 0 $V_{LEVEL} \gg V_{HCL}$		150		μs
τ_{HC75}	Highcut Time Constant	Bit = 7, Subadr. 10 = 1 $V_{LEVEL} \gg V_{HCL}$		225		μs

STEREOBLEND and HIGHCUT-CONTROL

REF5V	Internal Reference Voltage			5		V
T_{CREF5V}	Temperature Coefficient			3300		ppm
L_{Gmin}	Min. LEVEL Gain			0		dB
L_{Gmax}	Max. LEVEL Gain			10		dB
L_{Gstep}	LEVEL Gain Step Resolution			0.67		dB
V_{SBLmin}	Min. Voltage for Mono			33		%REF5V
V_{SBLmax}	Max. Voltage for Mono			58		%REF5V
$V_{SBLstep}$	Step Resolution			8.4		%REF5V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
STEREOBLEND and HIGHCUT CONTROL						
VHCH _{min}	Min. Voltage for NO Highcut			25		%REF5V
VHCH _{max}	Max. Voltage for NO Highcut			50		%REF5V
VHCH _{step}	Step Resolution			8.4		%REF5V
VHCL _{min}	Min. Voltage for FULL High cut			17		%VHCH
VHCL _{max}	Max. Voltage for FULL High cut			33		%VHCH
Carrier and harmonic suppression at the output						
α_{19}	Pilot Signal	f = 19KHz		50		dB
α_{38}	Subcarrier	f = 38KHz		75		dB
α_{57}	Subcarrier	f = 57KHz		62		dB
α_{76}	Subcarrier	f = 76KHz		90		dB
Intermodulation (Note1)						
α_2	Pilot Signal	f _{mod} = 10KHz; f _{spur} = 1KHz;		65		dB
α_3		f _{mod} = 13KHz; f _{spur} = 1KHz;		75		dB
Traffic Radio (Note 2)						
α_{57}	Signal	f = 57KHz		70		dB
SCA - Subsidiary Communications Authorization (Note 3)						
α_{67}	Signal	f = 67KHz		75		dB
ACI - Adjacent Channel Interference (Note 4)						
α_{114}	Signal	f = 114KHz		95		dB
α_{190}	Signal	f = 190KHz		84		dB

Notes to the Characteristics:

1. Intermodulation Suppression: measured with: 91% pilot signal; fm = 10kHz or 13kHz.
2. Traffic Radio (V.F.) Suppression: measured with: 91% stereo signal; 9% pilot signal; fm=1kHz; 5% subcarrier (f = 57kHz, fm = 23Hz AM, m = 60%)
3. SCA (Subsidiary Communications Authorization) measured with: 81% mono signal; 9% pilot signal; fm = 1kHz; 10%SCA - subcarrier (fs = 67kHz, unmodulated).
4. ACI (Adjacent Channel Interference) measured with: 90% mono signal; 9% pilot signal; fm =1kHz; 1% spurious signal (fs = 110kHz or 186kHz, unmodulated).

NOISE BLANKER PART

- Internal 2nd order 140kHz high-pass filter
- Programmable trigger threshold
- Programmable noise rectifier discharge current
- Additional circuits for trigger adjustment (deviation, field-strength)
- Very low offset current during hold time
- Four selectable pulse suppression times

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
V _{TR}	Trigger Threshold ^{0) 1)}	meas. with V _{PEAK} = 0.9V	NBT = 111		30		mV _{OP}
			NBT = 110		35		mV _{OP}
			NBT = 101		40		mV _{OP}
			NBT = 100		45		mV _{OP}
			NBT = 011		50		mV _{OP}
			NBT = 010		55		mV _{OP}
			NBT = 001		60		mV _{OP}
			NBT = 000		65		mV _{OP}
V _{TRNOISE}	Noise Controlled Trigger Threshold ²⁾	meas. with V _{PEAK} = 1.5V	NCT = 00		260		mV _{OP}
			NCT = 01		220		mV _{OP}
			NCT = 10		180		mV _{OP}
			NCT = 11		140		mV _{OP}
V _{RECT}	Rectifier Voltage	NDR ⁶⁾ = 00, V _{MPX} = 0mV			0.9		V
		V _{MPX} = 50mV; f = 150KHz			1.7		V
		V _{MPX} = 200mV; f = 150KHz			3.5		V
V _{RECT DEV}	deviation dependent rectifier Voltage ³⁾	means. with V _{MPX} = 500mV (75KHz dev.)	OVD = 11		0.9(off)		V _{OP}
			OVD = 10		1.2		V _{OP}
			OVD = 01		2.0		V _{OP}
			OVD = 00		2.8		V _{OP}
V _{RECT FS}	Fieldstrength Controlled Rectifier Voltage ⁴⁾	means. with V _{MPX} = 0mV V _{LEVEL} << V _{SBL} (fully mono)	FSC = 11		0.9(off)		V
			FSC = 10		1.4		V
			FSC = 01		1.9		V
			FSC = 00		2.4		V

0) All thresholds are measured using a pulse with $T_R = 2 \mu s$, $T_{HIGH} = 2 \mu s$ and $T_F = 10 \mu s$.

1) NBT represents the Noiseblanker-Byte bits D2 -D0 for the noise blanker trigger threshold

2) NAT represents the Noiseblanker-Byte bit pair D4,D3 for the noise controlled trigger adjustment

3) OVD represents the Noiseblanker-Byte bit pair D7,D6 for the over deviation detector

4) FSC represents the Fieldstrength-Byte bit pair D1,D0 for the fieldstrength control

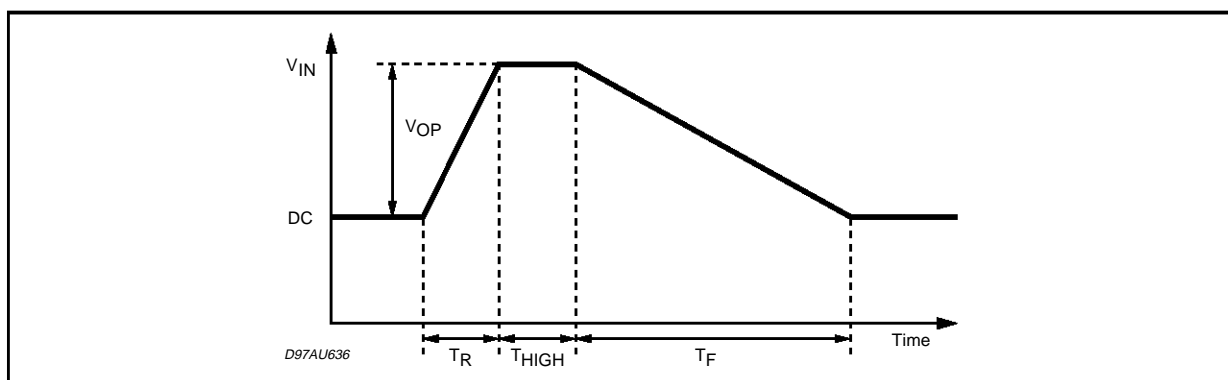


Figure 14. Trigger Threshold vs. VPEAK

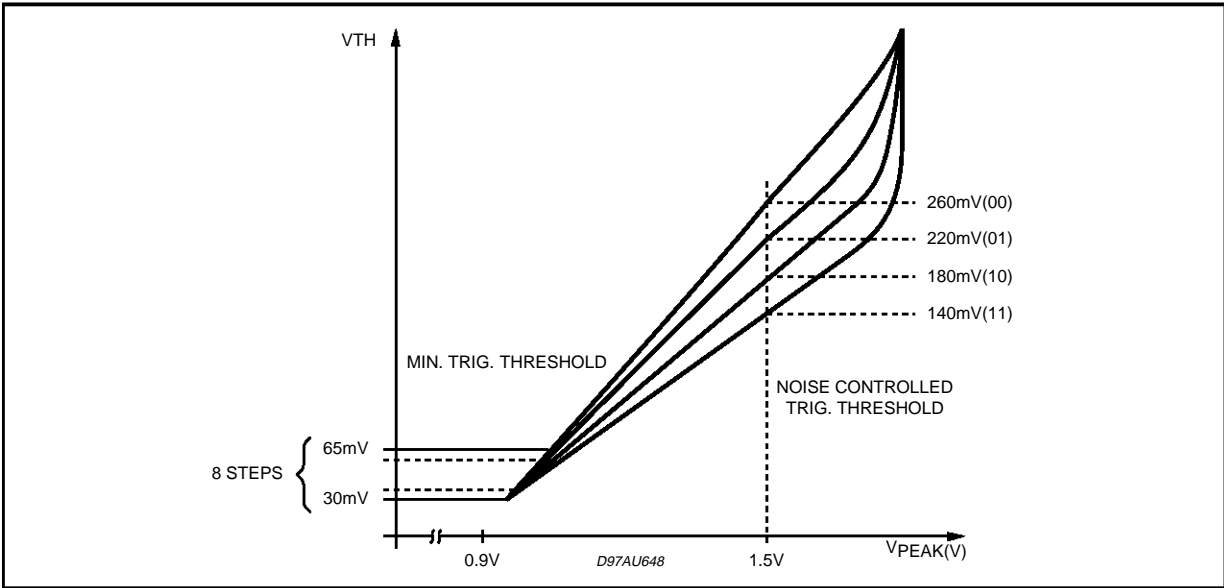


Figure 15. Deviation Controlled Trigger Adjustment

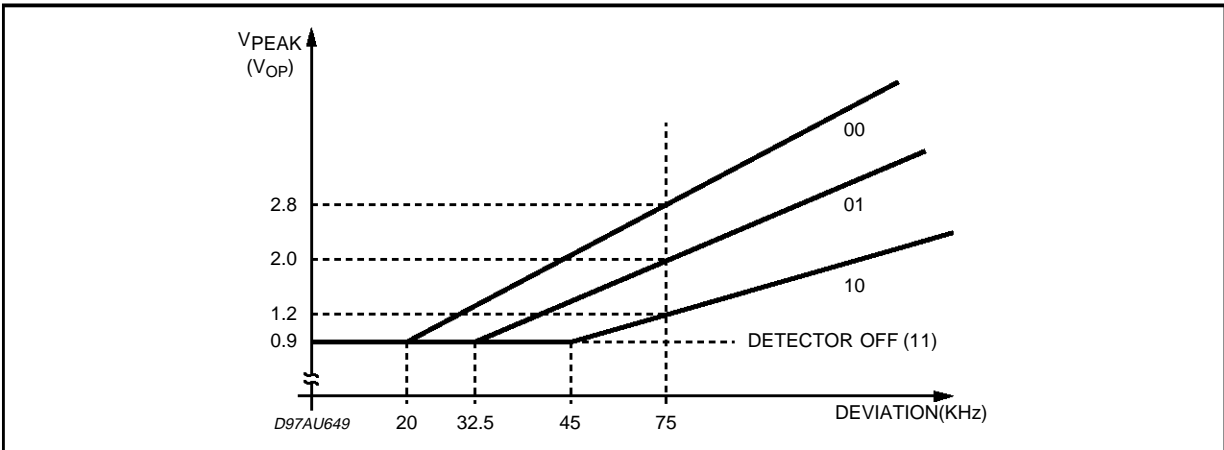
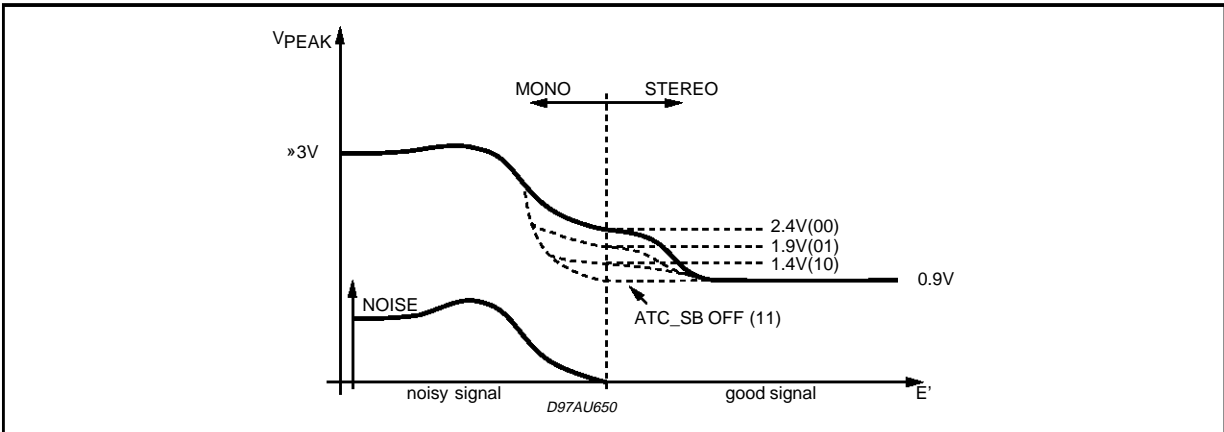


Figure 16. Fieldstrength Controlled Trigger Adjustment



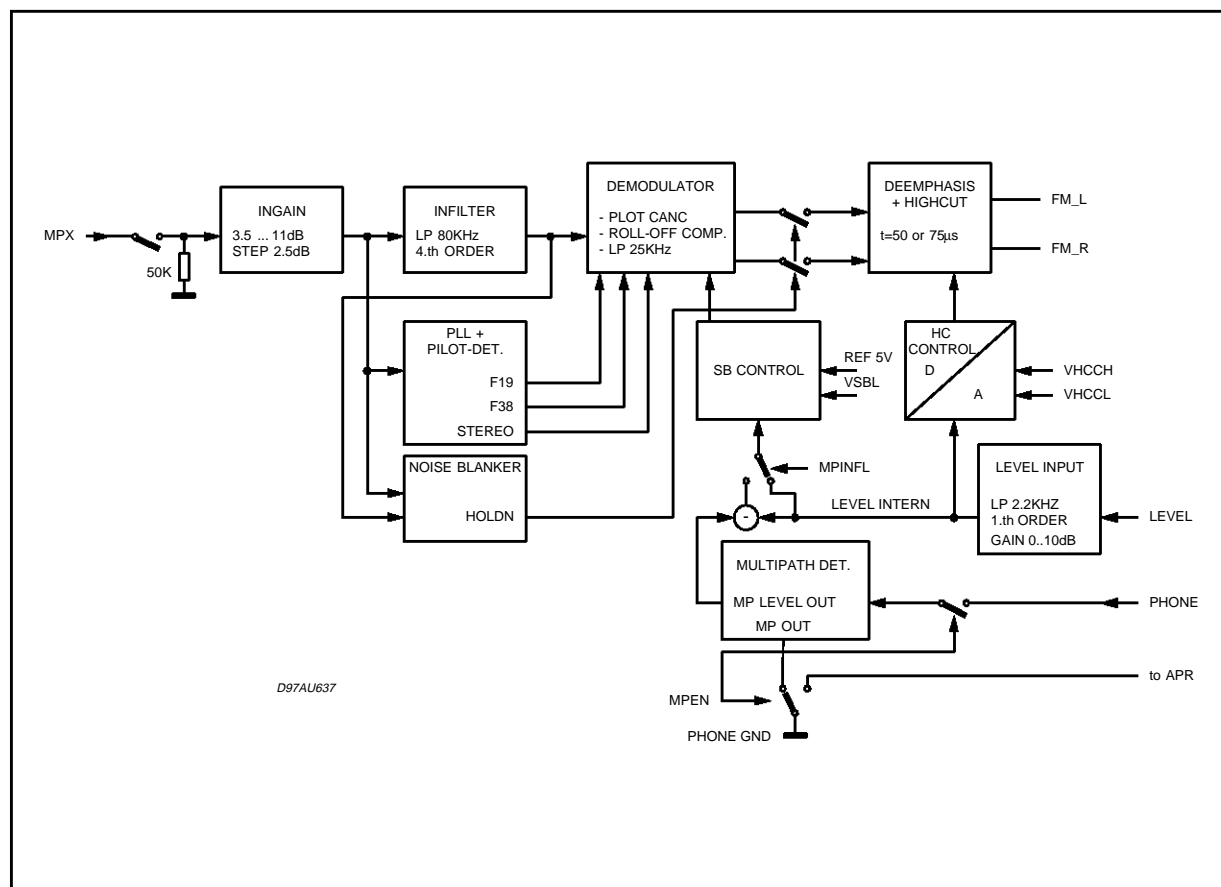
MULTIPATH DETECTOR

- Internal 19kHz band pass filter
- Programmable band-pass and rectifier gain
- Selectable internal influence on Stereoblend

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
f _{CMP}	Center frequency of Multipath-Bandpass	stereodecoder locked on Pilotone		19		KHz
G _{BPMP}	Bandpass Gain	bits D ₂ , D ₁ configuration byte = 00		6		dB
		bits D ₂ , D ₁ configuration byte = 01		12		dB
		bits D ₂ , D ₁ configuration byte = 10		16		dB
		bits D ₂ , D ₁ configuration byte = 11		18		dB
G _{RECTMP}	Reflection Gain	bits D ₇ , D ₆ configuration byte = 00		7.6		dB
		bits D ₇ , D ₆ configuration byte = 01		4.6		dB
		bits D ₇ , D ₆ configuration byte = 10		0		dB
		bits D ₇ , D ₆ configuration byte = 11		-10		dB
I _{CHMP}	Rectifier Charge Current			0.5		μA
I _{DISMP}	Rectifier Discharge Current			1.5		mA

Figure 17. Blockdiagram of the Stereodecoder



FUNCTIONAL DESCRIPTION OF STEREODECODER

The stereodecoder part of the TDA7460 (see Fig. 17) contains all functions necessary to demodulate the MPX signal: pilot tone-dependent MONO/STEREO switching as well as "stereoblend" and "highcut" advanced features.

Adaptations like programmable input gain, roll-off compensation, selectable deemphasis time constant and a programmable fieldstrength input allow to use different IF devices.

Stereodecoder Mute

The TDA7460 has a fast and easy to control RDS-Mute function which is a combination of the audioprocessor softmute and the high-ohmic mute of the stereodecoder. If the stereodecoder is selected and a Softmute command is sent (or activated through the SM pin) the stereodecoder will be set automatically to the high-ohmic mute condition after the audio signal has been softmuted.

Hence a checking of alternate frequencies could be performed. To release the system from the mute condition simply the unmute command must be sent: the stereodecoder is unmuted immediately and the audioprocessor is softly unmuted. Fig. 18 shows the output signal V_O as well as the internal stereodecoder mute signal. This influence of Softmute on the stereodecoder mute can be switched off by setting bit 3 of the Softmute byte to "0". A stereodecoder mute command (bit 0, stereodecoder byte set to "1") will set the stereodecoder in any case independently to the high-ohmic mute state.

If any other source than the stereodecoder is selected the decoder remains muted and the MPX pin is connected to V_{ref} to avoid any discharge of the coupling capacitor through leakage currents.

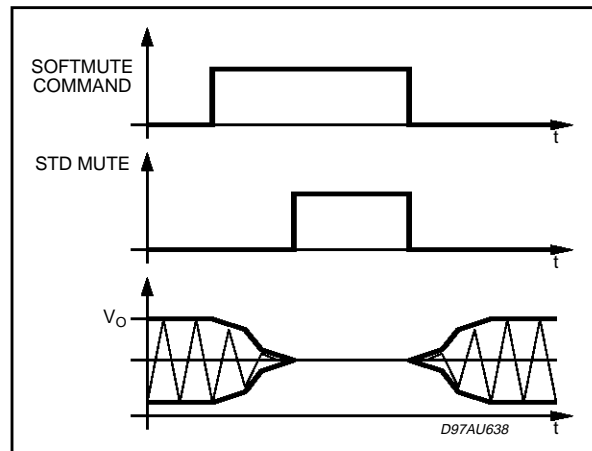
Ingain + Infilter

The Ingain stage allows to adjust the MPX signal to a magnitude of about 1Vrms internally which is the recommended value. The 4th order input filter has a corner frequency of 80kHz and is used to attenuate spikes and noise and acts as an anti-aliasing filter for the following switch capacitor filters.

Demodulator

In the demodulator block the left and the right channel are separated from the MPX signal. In this stage also the 19 kHz pilot tone is cancelled. For reaching a high channel separation the TDA7460 offers an I2C bus programmable roll-off

Figure 18. Signals during stereodecoder's softmute



adjustment which is able to compensate the low-pass behaviour of the tuner section. If the tuner attenuation at 38kHz is in a range from 13.8% to 24.6% the TDA7460 needs no external network in front of the MPX pin. Within this range an adjustment to obtain at least 40dB channel separation is possible.

The bits for this adjustment are located together with the fieldstrength adjustment in one byte. This gives the possibility to perform an optimization step during the production of the carradio where the channel separation and the fieldstrength control are trimmed.

Deemphasis and Highcut.

The deemphasis lowpass filter allows to choose between a time constant of 50μs and 75μs (bit D7, Stereodecoderbyte).

The highcut control range will be in both cases $t_{HC} = 2 \times t_D$. Inside the highcut control range (between VHCH and VHCL) the LEVEL signal is converted into a 5 bit word which controls the lowpass time constant between $t_D \dots 3 \times t_D$. Thereby the resolution will remain always 5 bits independently of the absolute voltage range between the VHCH and VHCL values.

The highcut function can be switched off by I2C-bus (bit D7, Fieldstrength byte set to "0").

PLL and Pilot Tone Detector

The PLL has the task to lock on the 19kHz pilot tone during a stereo transmission to allow a correct demodulation. The included detector enables the demodulation if the pilot tone reaches the selected threshold VPTHST. Two different thresholds are available. The detector output (signal STEREO, see blockdiagram) can be checked by reading the status byte of the TDA7460 via I2C bus.

Fieldstrength Control

The fieldstrength input is used to control the highcut and the stereoblend function. In addition the signal can be also used to control the noise-blanker thresholds and as input for the multipath detector. These additional functions are described in further sections.

LEVEL Input and Gain

To suppress undesired high frequency modulation on the highcut and stereoblend function the LEVEL signal is lowpass filtered firstly. The filter is a combination of a 1st order RC lowpass at 53kHz (working as anti aliasing filter) and a 1st order switched-capacitor lowpass at 2.2kHz. The second stage is a programmable gain stage to adapt the LEVEL signal internally to different IF-devices (see Testmode section: LEVELINTERN).

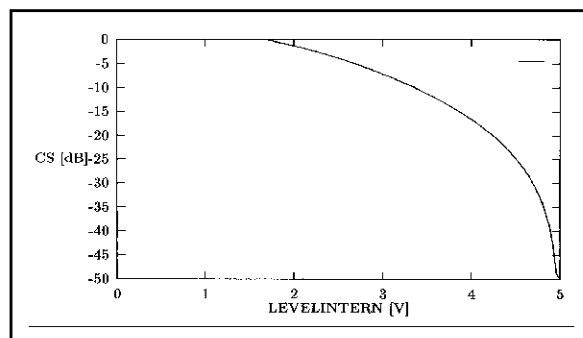
The gain is widely programmable in 16 steps from 0dB to 10dB (step=0.67dB). The 4 bits are located together with the Roll-Off bits in the "Stereodecoder Adjustment" byte to simplify a possible adaptation during the production of the carradio.

Stereoblend Control

The stereoblend control block converts the internal LEVEL voltage (LEVELINTERN) into an demodulator compatible analog signal which is used to control the channel separation between 0dB and the maximum separation. Internally this control range has a fixed upper limit which is the internal reference voltage REF5V. The lower limit can be programmed to be 33%, 42%, 50% or 58% of REF5V (see figs.16, 17).

To adjust the external LEVEL voltage to the internal range two values must be defined: the LEVEL gain LG and VSBL (see fig. 17). To adjust the voltage where the full channel separation is reached (VST) the LEVEL gain LG has to be defined.

Figure 19. Internal Stereoblend characteristics



The gain can be programmed through 4 bits in the "Stereodecoder-Adjustment" byte.

The MONO voltage VMO (0dB channel separation) can be chosen selecting 33, 42, 50 or 58% of REF5V.

All necessary internal reference voltages like REF5V are derived from a bandgap circuit. Therefore they have a temperature coefficient near zero. This is useful if the fieldstrength signal is also temperature compensated.

But most IF devices applying a LEVEL voltage with a TC of 3300ppm. The TDA7460 offers this TC for the reference voltages, too. The TC is selectable with bit D7 of the "stereodecoder adjustment"-byte.

Highcut Control

The highcut control set up is similar to the stereoblend control set up: the starting point VHCH can be set with 2 bits to be 25, 33, 42 or 50% of REF5V whereas the range can be set to be 17 or 33% of VHCH (see fig. 21).

FUNCTIONAL DESCRIPTION OF THE NOISE-BLANKER

In a first stage the spikes must be detected but to

Figure 20. Relation between internal and external LEVEL voltage and Setup of Stereoblend

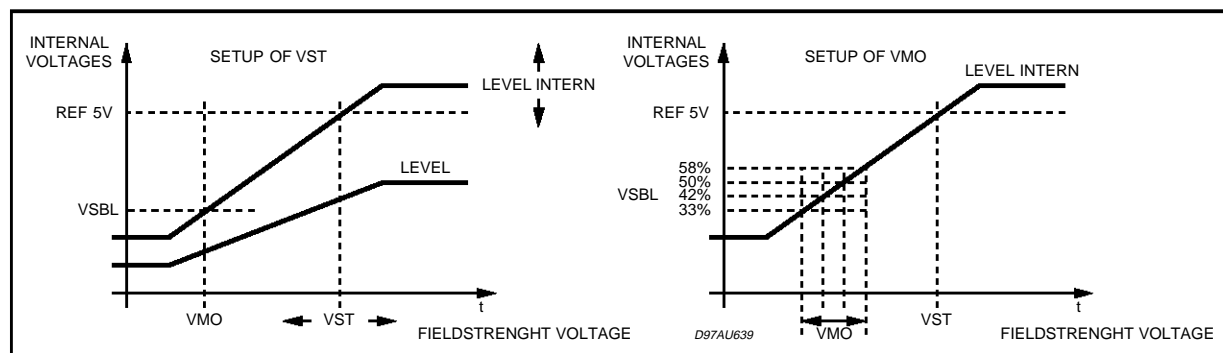
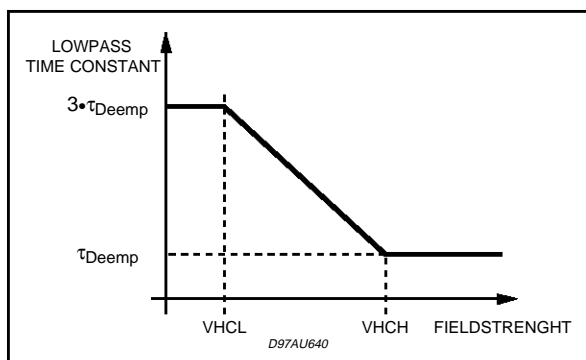


Figure 21. Highcut characteristics



avoid a wrong triggering on high frequency (white) noise a complex trigger control is implemented. Behind the triggerstage a pulse former generates the blanking pulse. To avoid any crosstalk to the signalpath the noiseblanker is supplied by his own biasing circuit.

Trigger Path

The incoming MPX signal is highpass filtered, amplified and rectified. This second order high-pass filter has a corner frequency of 140kHz. The rectified signal, RECT, is lowpass filtered to generate a signal called PEAK. Also noise with a frequency 140kHz increases the PEAK voltage. The PEAK voltage is fed to a threshold generator, which adds to the PEAK voltage a DC dependent threshold VTH. Both signals, RECT and PEAK+VTH are fed to a comparator which triggers a monoflop. The monoflop's output activates the sample-and-hold circuits for 40μs.

In the automotive environment the MPX signal is

disturbed by spikes produced for example by the ignition and the wiper-motor. The aim of the noiseblanker part is to cancel the audible influence of the spikes. Therefore the output of the stereodecoder is held at the actual voltage for 40μs.

The block diagram of the noiseblanker is given in fig.22.

In a first stage the spikes must be detected but to avoid a wrong triggering on high frequency (white) noise a complex trigger control is implemented. Behind the trigger stage a pulse former generates the blanking pulse. To avoid any crosstalk the noiseblanker is supplied by his own biasing circuit.

Automatic Noise Controlled Threshold Adjustment (ATC)

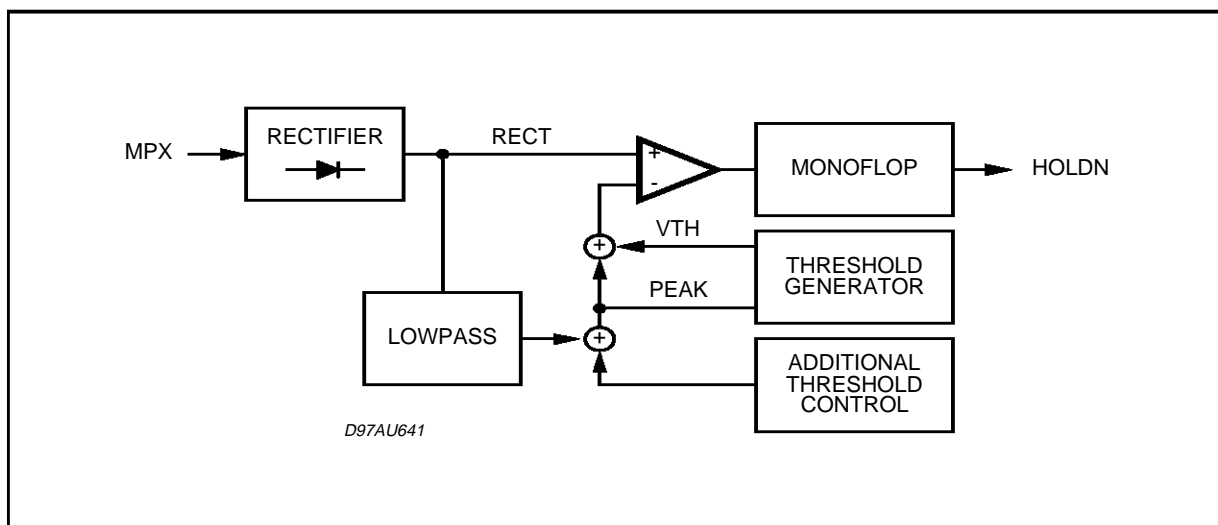
There are mainly two independent possibilities for programming the trigger threshold:

- the low threshold in 8 steps (bits D0 to D2 of the noiseblanker byte)
- the noise adjusted threshold in 4 steps (bits D3 and D4 of the noiseblanker byte, see fig. 14).

The low threshold is active in combination with a good MPX signal without any noise; the PEAK voltage is less than 1V. The sensitivity in this operation is high.

If the MPX signal is noisy the PEAK voltage increases due to the higher noise, which is also rectified. With increasing of the PEAK voltage the trigger threshold increases, too. This particular gain is programmable in 4 steps (see fig. 14).

Figure 22. Block diagram of the Noiseblanker



Automatic Threshold Control by the Stereoblend voltage

Besides the noise controlled threshold adjustment there is an additional possibility for influencing the trigger threshold. It is depending on the stereoblend control.

The point where the MPX signal starts to become noisy is fixed by the RF part. Therefore also the starting point of the normal noise-controlled trigger adjustment is fixed (fig. 16). In some cases the behaviour of the noiseblanker can be improved by increasing the threshold even in a region of higher fieldstrength. Sometimes a wrong triggering occurs for the MPX signal often shows distortion in this range which can be avoided even if using a low threshold.

Because of the overlap of this range and the range of the stereo/mono transition it can be controlled by stereo blend. This threshold increase is programmable in 3 steps or switched off with bits D0 and D1 of the field strength control byte.

Over Deviation Detector

If the system is tuned to stations with a high deviation the noiseblanker can trigger on the higher frequencies of the modulation. To avoid this wrong behaviour, which causes noise in the output signal, the noiseblanker offers a deviation-dependent threshold adjustment.

By rectifying the MPX signal a further signal representing the actual deviation is obtained. It is used to increase the PEAK voltage. Offset and gain of this circuit are programmable in 3 steps with the bits D6 and D7 of the stereodecoder-byte (the first step turns off the detector, see fig. 15).

FUNCTIONAL DESCRIPTION OF THE MULTIPATH DETECTOR

Using the internal Multipath Detector the audible effects of a multipath condition can be minimized. A multipath condition is detected by rectifying the 19kHz spectrum in the fieldstrength signal.

An external capacitor is used to define the attack and decay times (see fig. 23). The PHONE_GND pin is used as detector-output (MPOUT) connected to a capacitor of about 47nF and additionally the PHONE pin is selected to be the field-strength input (MPIN). Using this configuration an external adaptation to the user's requirement is possible without effecting the standard field-strength input (LEVEL) for the stereodecoder. One possible application is showed in fig. 25.

Selecting the "internal influence" in the configuration byte the channel separation is automatically reduced during a multipath condition according to the voltage appearing at the MPOUT pin.

To obtain a good multipath performance an adaptation is necessary. Therefore the gain of the 19kHz bandpass is programmable in four steps as well as the rectifier gain. The attack and decay times can be set by the external capacitor value.

TESTMODE

During the Testmode which can be activated by setting bit D0 of the the testing byte and bit D5 of the subaddress byte to "1" several internal signals are available at the CASS_R pin. During this mode the input resistance of 100kOhm is disconnected from the pin. The internal signals available are shown in the Data byte specification.

Figure 23. Block diagram of the Multipath Detector

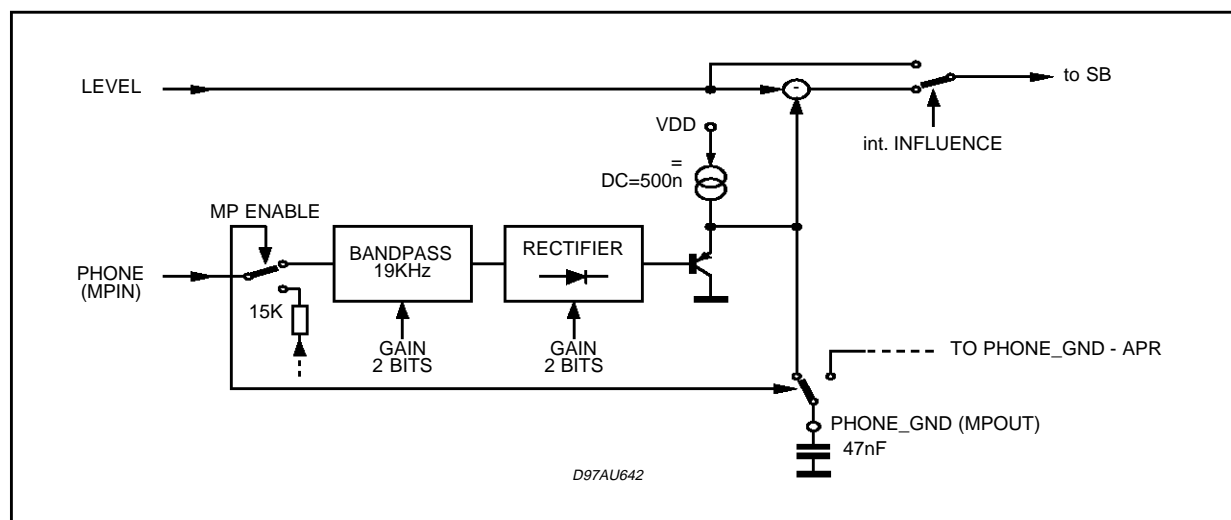


Figure 24. Application 1

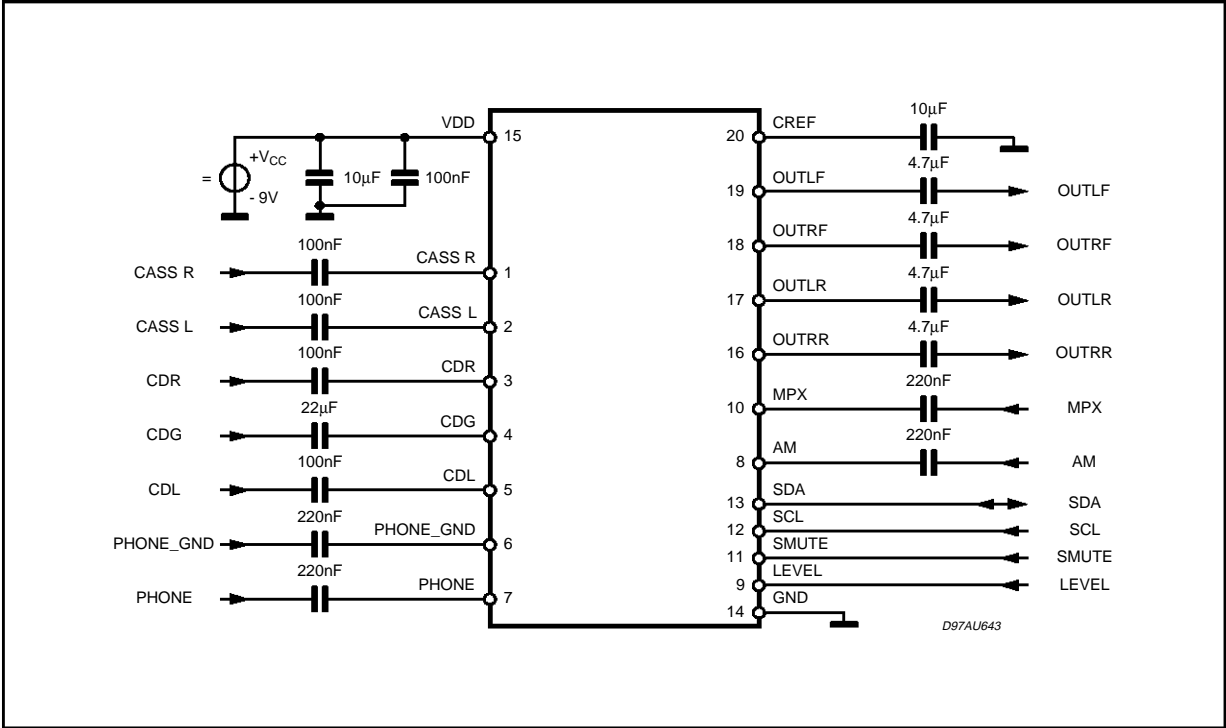
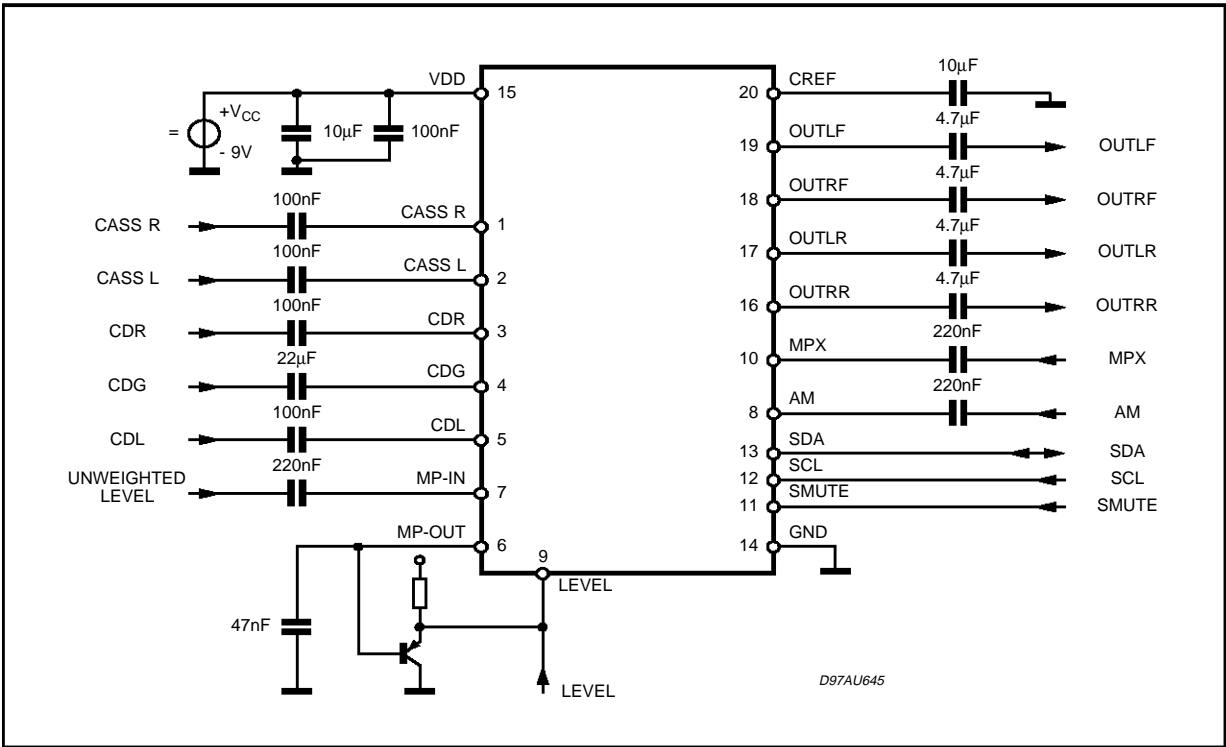


Figure 25. Application 2

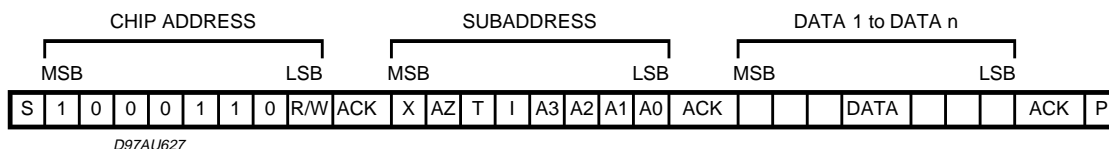


I²C BUS INTERFACE DESCRIPTION

Interface Protocol

The interface protocol comprises:

- a start condition (S)
- a chip address byte (the LSB bit determines read / write transmission)
- a subaddress byte
- a sequence of data (N-bytes + acknowledge)
- a stop condition (P)



S = Start

ACK = Acknowledge

AZ = AutoZero Remain

T = Testing

P = Stop

MAX CLOCK SPEED 500kbits/s

The transmitted data is automatically updated after each ACK.

Transmission can be repeated without new chip address.

Auto increment

If bit I in the subaddress byte is set to "1", the autoincrement of the subaddress is enabled.

TRANSMITTED DATA (send mode)

MSB				LSB			
X	X	X	X	ST	SM	X	X

SM = Soft mute activated

ST = Stereo

X = Not Used

SUBADDRESS (receive mode)

MSB				LSB				FUNCTION
X	AZ	T	P	A3	A2	A1	A0	
				0	0	0	0	Input selector
				0	0	0	1	Loudness / Auto-Zero
				0	0	1	0	Volume
				0	0	1	1	Softmute / Beep
				0	1	0	0	Bass / Treble Attenuator
				0	1	0	1	Bass / Treble Configuration
				0	1	1	0	Speaker attenuator LF
				0	1	1	1	Speaker attenuator LR
				1	0	0	0	Speaker attenuator RF
				1	0	0	1	Speaker attenuator RR / Blanktime adjust
				1	0	1	0	Stereodecoder
				1	0	1	1	Noiseblanker
				1	1	0	0	Fieldstrength Control
				1	1	0	1	Configuration
				1	1	1	0	Stereodecoder Adjustment
				1	1	1	1	Testing

T = Testmode

P = Paging

AZ = AutoZero Remain

X = not used

DATA BYTE SPECIFICATION

Input Selector

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
					0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1	Source Selector CD Cassette Phone AM Stereodecoder not allowed Mute not allowed
				0 1				CD Mode CD-full-diff. CD-quasi-diff
			1 0 0 1		0 0 1 1	1 1 0 0	1 1 0 0	AM/FM-Mode AM mono AM stereo AM through Stereodecoder FM- Stereodecoder
0 0 : 1 1	0 0 : 1 1	0 1 : 0 1						In-Gain 14dB 12dB : 2 dB 0 dB

For example to select the CD input in quasi-differential-mode with gain of 8dB the Data Byte is: 0/01111000

Loudness

MSB							LSB	LOUDNESS
D7	D6	D5	D4	D3	D2	D1	D0	
				0 0 : 1 1	0 0 : 1 1	0 0 : 1 1	0 1 : 0 1	Attenuation 0dB -1dB : -14dB -15dB
			0 1					Filter on off (flat)
		0 1						Center Frequency 200Hz 400Hz
	0 1							Loudness Q low normal
1								must be "1"

Note: The attenuation is specified at high frequencies. Around the center frequency the value is different depending on the programmed attenuation (see Loudness-frequency-response).

Mute, Beep and Mixing

MSB								LSB	MUTE/BEEP/MIXING
D7	D6	D5	D4	D3	D2	D1	D0		
								0 1	Mute enable Softmute disable oftmute Mutetime =0.48 ms Mutetime =0.96 ms Mutetime =40.4 ms Mutetime =324 ms Stereodecoder-Softmute-Influence = off (Note2) Stereodecoder-Softmute-Influence = on
			0 1						Beep Beep Frequency = 600Hz Beep Frequency = 1.2Hz
0 0 1 1	0 1 0 1	0 1							Mixing Mix-Source = Beep Mix-Source = Phone full Mix-Signal Source -12dB + Mix-Signal -2.5dB Source -6dB + Mix-Signal -6dB full Source

Note: For more information to the Stereodecoder-Softmute-Influence please refer to the stereodecoder description.

Volume

MSB								LSB	ATTENUATION
D7	D6	D5	D4	D3	D2	D1	D0		
	0 0 : 0 0 0 : 0 0 : 1 1	0 0 : 0 0 0 : 0 1 1 1 1	0 0 : 0 0 0 : 1 0 0 0 0	0 0 : 1 1 1 : 0 1 1 1 1	0 0 : 1 1 1 : 0 1 1 1 1	0 0 : 0 1 1 : 0 1 1 1 1	0 1 : 0 1 0 : 0 0 : 1 1		Gain/Attenuation (+32dB) (Note 3) (+31dB) : +20dB +19dB +18dB : +1dB 0dB - 1dB : -78dB -79dB
0 1									Softstep Softstep-Volume = off Softstep-Volume = on

Note: It is not recommended to use a gain more than 20dB for system performance reason. In general, the max. gain should be limited by software to the maximum value, which is needed for the system.

Bass & Treble Attenuation

MSB							LSB	BASS & TREBLE ATTENUATION
D7	D6	D5	D4	D3	D2	D1	D0	
				0	0	0	0	Treble Steps -14dB -12dB : -2dB 0dB 0dB +2dB : +12dB +14dB
				0	0	0	1	
				:	:	:	:	
				0	1	1	0	
				0	1	1	1	
				1	1	1	1	
				1	1	1	0	
				:	:	:	:	
				1	0	0	1	
				1	0	0	0	
0	0	0	0					Bass Steps -14dB -12dB : -2dB 0dB 0dB +2dB : +12dB +14dB
0	0	0	1					
:	:	:	:					
0	1	1	0					
0	1	1	1					
1	1	1	1					
1	1	1	0					
:	:	:	:					
1	0	0	1					
1	0	0	0					

For example 12dB Treble and -8dB Bass give the following DATA BYTE : 0 0 1 1 1 0 0 1.

Bass & Treble Filter Characteristics

MSB							LSB	BASS & TREBLE FILTER
D7	D6	D5	D4	D3	D2	D1	D0	
						0	0	Treble Center Frequency = 10 KHz Center Frequency = 12.5 KHz Center Frequency = 15 KHz Center Frequency = 17.5 KHz
						0	1	
						1	0	
						1	1	
				0	0			Bass Center Frequency = 60 Hz Center Frequency = 70 Hz Center Frequency = 80 Hz Center Frequency = 100Hz Center Frequency = 150Hz (Note 4) Quality factor = 1 Quality factor = 1.25 Quality factor = 1.5 Quality factor = 2 DC-Gain = 0dB DC-Gain = ± 5 dB
				0	1			
				1	0			
				1	1			
				1	1			
		1	1					
		0	0					
		0	1					
		1	0					
		1	1					
	0							must be "1"
	1							
1								

Note 4: For more information please refer to section Bass description

For example Treble center-frequency = 15kHz, Bass center-frequency = 100Hz, Bass-Q = 1 and DC = 0dB give the following DATA BYTE: 1 0 0 0 1 1 1 0

Stereodecoder

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
							0 1	STD Muted STD Unmuted
					0 1 0 1	0 1 0 1		IN-Gain 11dB IN-Gain 8.5dB IN-Gain 6dB IN-Gain 3.5dB
				1				must be "1"
		1 1	0 1					Forced MONO MONO/STEREO switch automatically
	0 1							Pilot Threshold HIGH Pilot Threshold LOW
0 1								Deemphasis 50µs Deemphasis 75µs

Noiseblanker

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
					0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1	Low Threshold 65mV Low Threshold 60mV Low Threshold 55mV Low Threshold 50mV Low Threshold 45mV Low Threshold 40mV Low Threshold 35mV Low Threshold 30mV
			0 0 1 1	0 1 0 1				Noise Controlled Threshold 320mV Noise Controlled Threshold 260mV Noise Controlled Threshold 200mV Noise Controlled Threshold 140mV
		0 1						Noiseblanker OFF Noiseblanker ON
0 0 1 1	0 1 0 1							Overdeviation Adjust 2.8V Overdeviation Adjust 2.0V Overdeviation Adjust 1.2V Overdeviation Detector OFF

Fieldstrength Control

MSB								LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0		
						0	0		Noiseblanker Fieldstrength Adjust 2.3V
						0	1		Noiseblanker Fieldstrength Adjust 1.8V
						1	0		Noiseblanker Fieldstrength Adjust 1.3V
						1	1		Noiseblanker Fieldstrength Adjust OFF
				0	0				VSBL at 33% REF 5V
				0	1				VSBL at 42% REF 5V
				1	0				VSBL at 50% REF 5V
				1	1				VSBL at 58% REF 5V
		0	0						VHCH at 25% REF 5V
		0	1						VHCH at 33% REF 5V
		1	0						VHCH at 42% REF 5V
		1	1						VHCH at 50% REF 5V
	0								VHCL at 17% VHCH
	1								VHCL at 33% VHCH
0									Highcut OFF
1									Highcut ON

Configuration

MSB								LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0		
						0	0		Must be "0"
				0	0				Multipath Detector Bandpass Gain
				0	1				6dB
				1	0				12dB
				1	1				16dB
				1	1				18dB
			0						Multipath Detector internal influence
			1						ON
									OFF
		0							Multipath ON/OFF
		1							ON
									OFF
0	0								Multipath Detector Reflection Gain
0	1								Gain = 7.6dB
1	0								Gain = 4.6dB
1	1								Gain = 0dB
									Gain = -10dBdB

Stereodecoder Adjustment

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
					0 0 0 : 1 : 1	0 0 1 : 0 : 1	0 1 0 : 0 : 1	Roll-Off Compensation not allowed 20.2% 21.9% : 25.5% : 31.0%
	0 0 0 : 1	0 0 0 : 1	0 0 1 : 1	0 1 0 : 1				LEVEL Gain 0dB 0.66dB 1.33dB : 10dB
0 1								Temperature compensation at LEVEL input TC = 0 TC = 16.7mV/K (3300ppm)

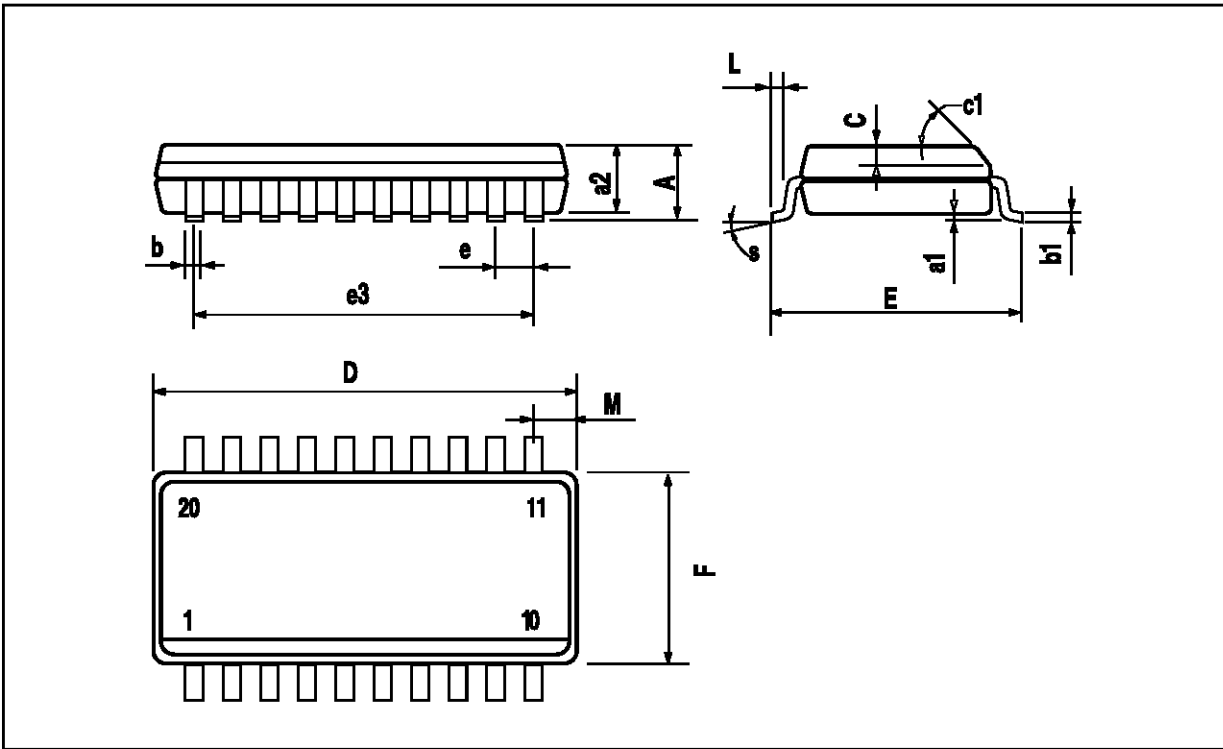
Testing

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
							0 1	Stereodecoder Testsignals OFF Testsignals enabled if bit D5 of the subaddress (Testmode-bit) is set to "1", too
						0 1		External Clock Internal Clock
		0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1	0 0 0 0 1 1 1 1 0 0 0 1 1 1 1 1	0 0 1 1 0 1 1 1 0 0 0 1 0 1 1 1	0 1 0 1 0 1 1 1 0 0 1 0 0 1 0 1			Testsignals at CASS_R VHCH level intern Pilot magnitude VCOCON; VCO Control Voltage Pilot threshold HOLDN NB threshold F228 VHCCCL VSBL not used not used PEAK not used REF5V not used
	0 1							VCO OFF ON
0 1								Audioprocessor Testmode enabled if bit D5 of the subaddress (Testmode-bit) is set to "1", too OFF

Note : This byte is used for testing or evaluation purposes only and must not set to other values than the default "11111110" in the application!

SO20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	12.6		13.0	0.496		0.512
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.4		7.6	0.291		0.299
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8° (max.)					



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