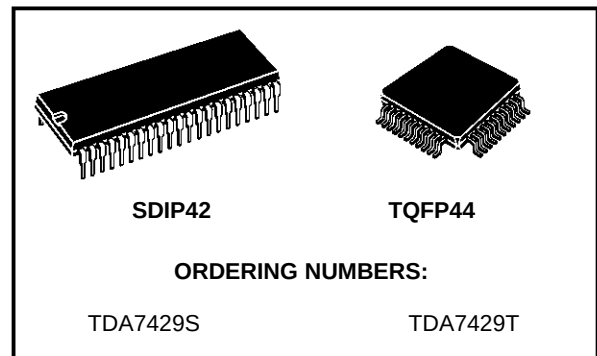


DIGITALLY CONTROLLED AUDIO PROCESSOR WITH SURROUND SOUND MATRIX

- 3 STEREO/4 STEREO INPUTS
- INPUT ATTENUATION CONTROL IN 0.5dB STEP
- TREBLE MIDDLE AND BASS CONTROL
- THREE SURROUND MODES ARE AVAILABLE:
 - MUSIC: 4 SELECTABLE RESPONSES
 - MOVIE AND SIMULATED: 256 SELECTABLE RESPONSES
- FOUR SPEAKERS ATTENUATORS:
 - 4 INDEPENDENT SPEAKERS CONTROL IN 1dB STEPS FOR BALANCE FACILITY
 - INDEPENDENT MUTE FUNCTION
- ALL FUNCTIONS PROGRAMMABLE VIA SERIAL BUS

DESCRIPTION

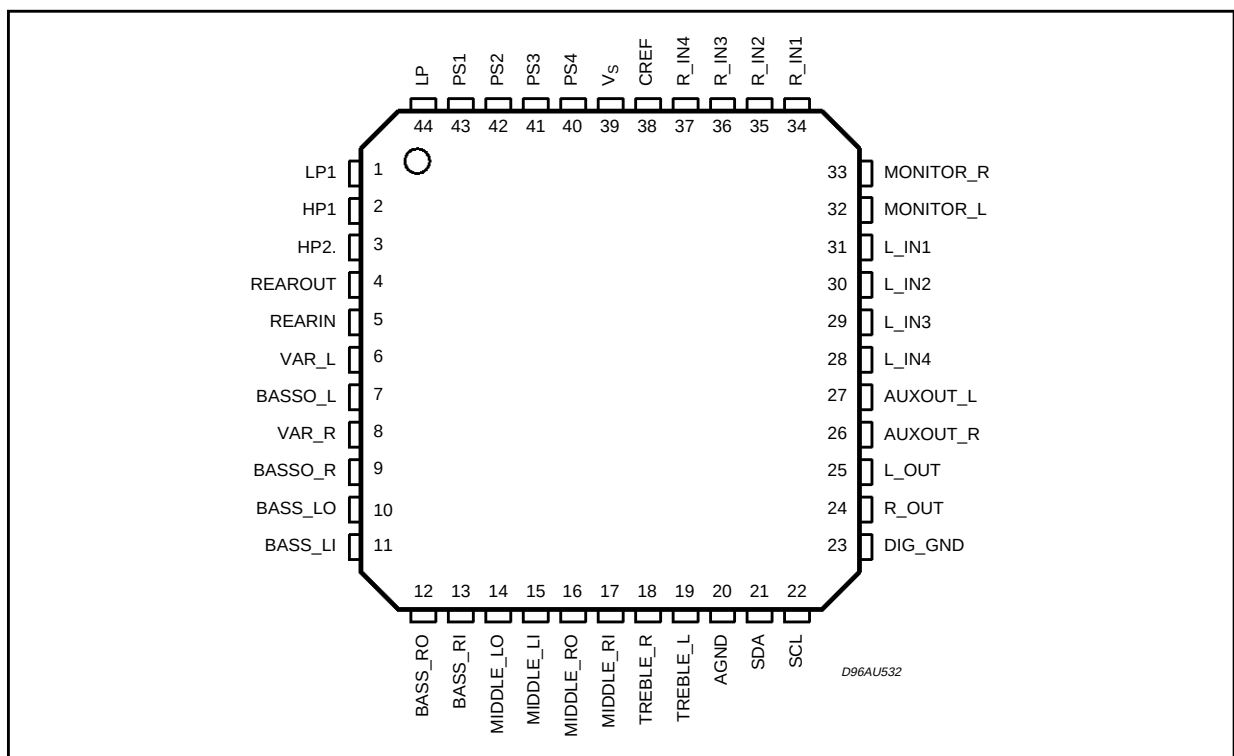
The TDA7429 is volume tone (bass middle and treble) balance (Left/Right) processors for quality audio applications in TV and Hi-Fi systems.



It reproduces surround sound by using programmable phase shifters and a signal matrix. Control of all the functions is accomplished by serial bus. The AC signal setting is obtained by resistor networks and switches combined with operational amplifiers.

Thanks to the used BIPOLAR/CMOS Technology, Low Distortion, Low Noise and DC stepping are obtained.

PIN CONNECTION (TQFP44)

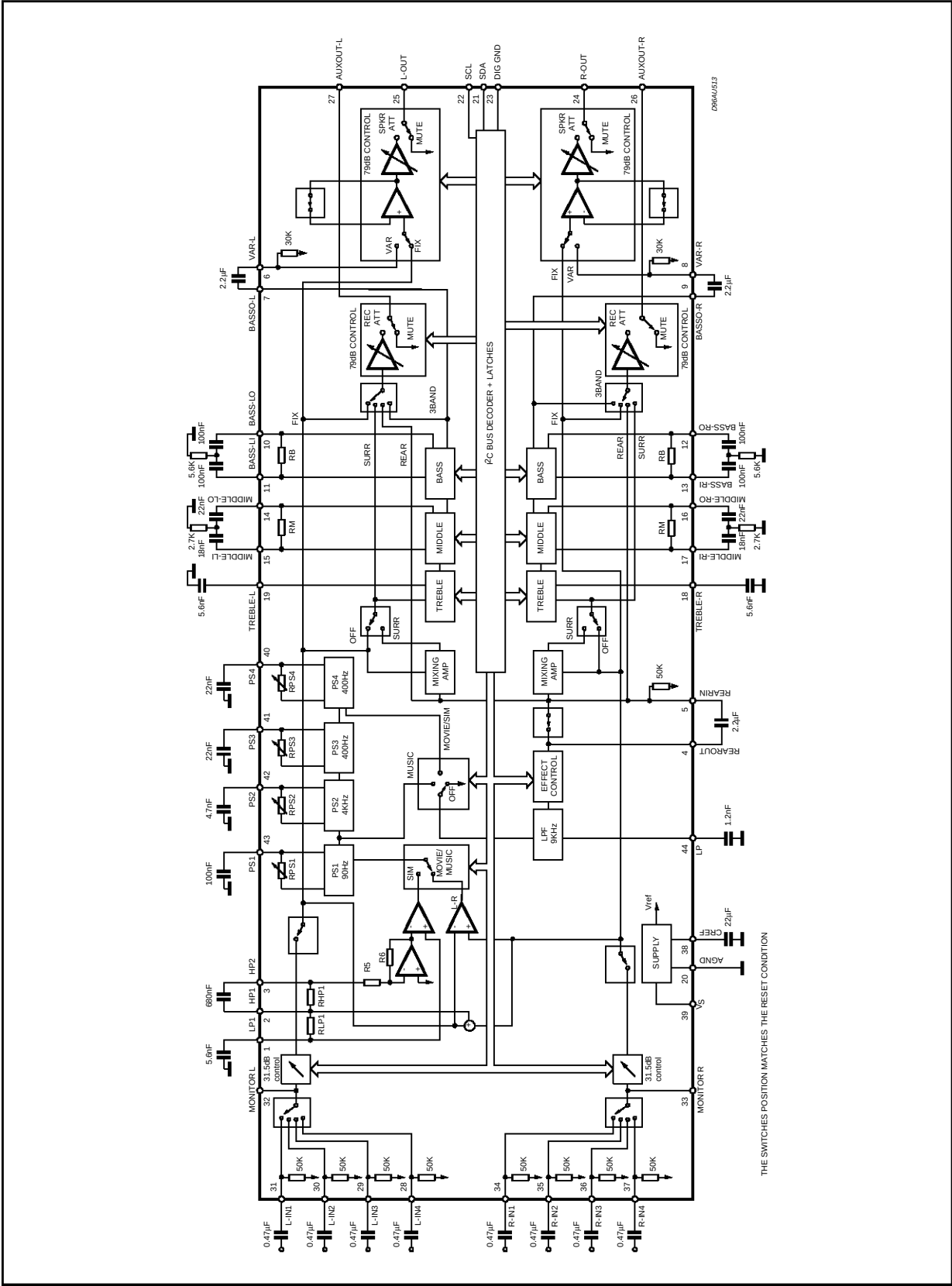




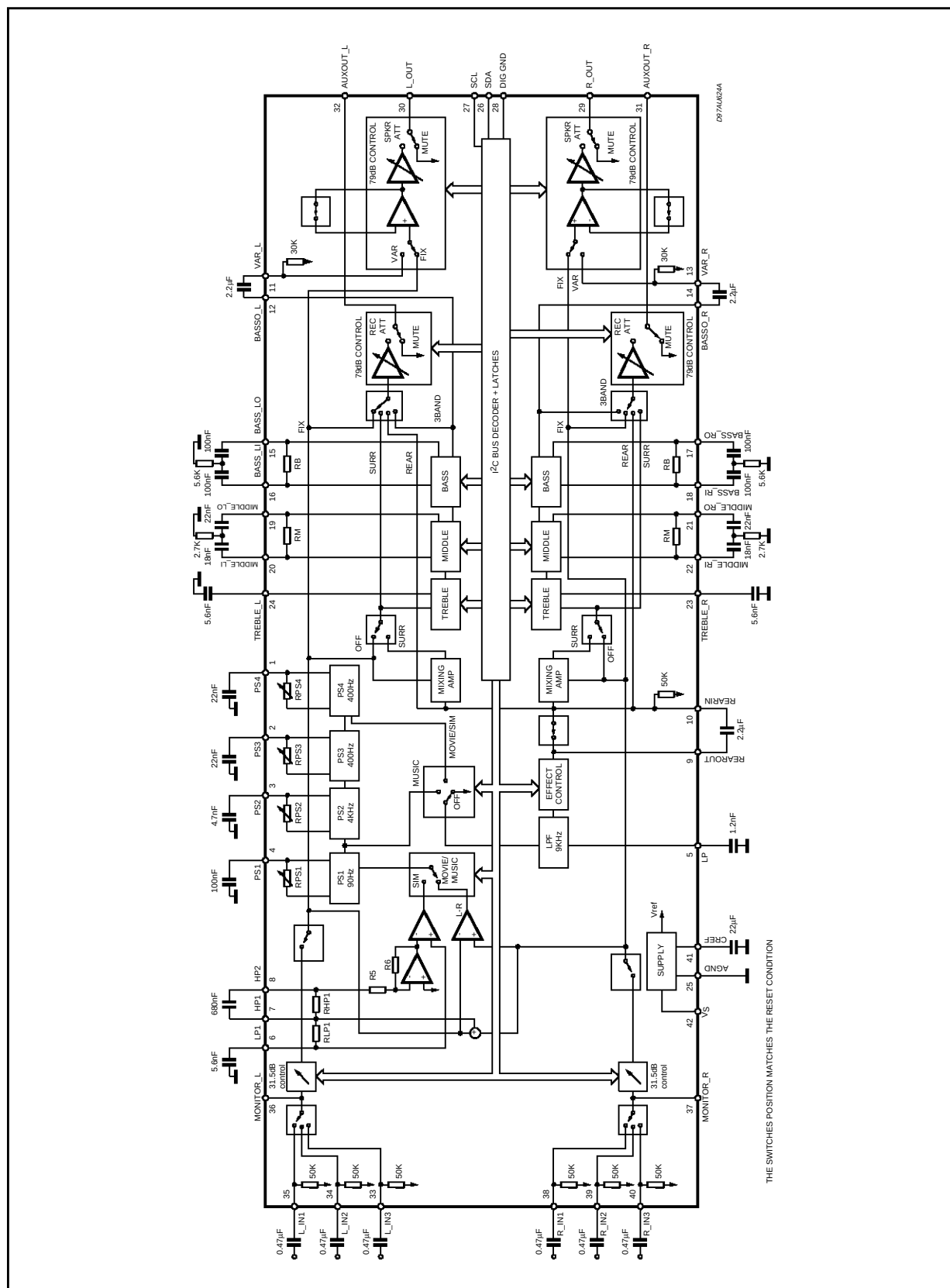
TEST CIRCUIT (TDA7429T)



BLOCK DIAGRAM (TDA7429T)



BLOCK DIAGRAM (TDA7429S)



THERMAL DATA

Symbol	Description	Value	Unit
$R_{thj-pins}$	Thermal Resistance Junction-pins	Max. 85	°C/W

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Operating Supply Voltage	11	V
T_{amb}	Operating Ambient Temperature	-10 to 85	°C
T_{stg}	Storage Temperature Range	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (refer to the test circuit $T_{amb} = 25^{\circ}\text{C}$, $V_S = 9\text{V}$, $R_L = 10\text{K}\Omega$, $V_{in} = 1\text{V}_{rms}$; $R_G = 600\Omega$, all controls flat ($G = 0\text{dB}$), Effect Ctrl = -6dB , MODE = OFF; $f = 1\text{KHz}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
--------	-----------	----------------	------	------	------	------

SUPPLY

V_S	Supply Voltage		7	9	10.2	V
I_S	Supply Current		10	18	26	mA
SVR	Ripple Rejection	LCH / RCH out, Mode = OFF	60	80		dB

INPUT STAGE

R_{IN}	Input Resistance		35	50	65	K Ω
V_{CL}	Clipping Level	THD = 0.3%	2	2.5		V _{rms}
C_{RANGE}	Control Range			31.5		dB
A_{VMIN}	Min. Attenuation		-1	0	1	dB
A_{VMAX}	Max. Attenuation		31	31.5	32	dB
A_{STEP}	Step Resolution			0.5	1	dB

BASS CONTROL

G_b	Control Range	Max. Boost/cut	± 11.5	± 14.0	± 16.0	dB
B_{STEP}	Step Resolution		1	2	3	dB
R_b	Internal Feedback Resistance		32	44	56	K Ω

MIDDLE CONTROL

G_m	Control Range	Max. Boost/cut	± 11.5	± 14.0	± 16.0	dB
M_{STEP}	Step Resolution		1	2	3	dB
R_m	Internal Feedback Resistance		17.5	25	32.5	K Ω

TREBLE CONTROL

G_t	Control Range	Max. Boost/cut	± 13.0	± 14.0	± 15.0	dB
T_{STEP}	Step Resolution		1	2	3	dB

EFFECT CONTROL

C_{RANGE}	Control Range		- 21		- 6	dB
S_{STEP}	Step Resolution		0.5	1	1.5	dB

SURROUND SOUND MATRIX PHASE

R_{PS10}	Phase Shifter 1: D1 = 0, D0 = 0		8.3	11.8	15.2	K Ω
R_{PS11}	Phase Shifter 1: D1 = 0, D0 = 1		10	14.1	18.3	K Ω
R_{PS12}	Phase Shifter 1: D1 = 1, D0 = 0		12.6	17.9	23.3	K Ω
R_{PS13}	Phase Shifter 1: D1 = 1, D0 = 1		26.4	37.3	48.85	K Ω
R_{PS20}	Phase Shifter 2: D3 = 0, D2 = 0		4	5.6	7.2	K Ω

ELECTRICAL CHARACTERISTICS (continued)**SURROUND SOUND MATRIX**

TEST CONDITION (Phase Resistor Selection D0=0, D1=1, D2=0, D3=1, D4=0, D5=1, D6=0, D7=1)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
R _{PS21}	Phase Shifter 2: D3 = 0, D2 = 1		4.8	6.8	8.7	K Ω
R _{PS22}	Phase Shifter 2: D3 = 1, D2 = 0		6	8.4	10.9	K Ω
R _{PS23}	Phase Shifter 2: D3 = 1, D2 = 1		12.9	18.3	23.7	K Ω
R _{PS30}	Phase Shifter 3: D5 = 0, D4 = 0		8.5	12.1	15.6	K Ω
R _{PS31}	Phase Shifter 3: D5 = 0, D4 = 1		10.2	14.5	18.7	K Ω
R _{PS32}	Phase Shifter 3: D5 = 1, D4 = 0		12.7	18.1	23.3	K Ω
R _{PS33}	Phase Shifter 3: D5 = 1, D4 = 1		27.4	39.1	50.75	K Ω
R _{PS40}	Phase Shifter 4: D7 = 0, D6 = 0		8.5	12.1	15.6	K Ω
R _{PS41}	Phase Shifter 4: D7 = 0, D6 = 1		10.2	14.5	18.7	K Ω
R _{PS42}	Phase Shifter 4: D7 = 1, D6 = 0		12.7	18.1	23.3	K Ω
R _{PS43}	Phase Shifter 4: D7 = 1, D6 = 1		27.4	39.1	50.75	K Ω
G _{OFF}	In-phase Gain (OFF)	Mode OFF, Input signal of 1kHz, 1.4 V _{p-p} , R _{in} → R _{out} L _{in} → L _{out}	-1	0	1	dB
D _{G_{OFF}}	LR In-phase Gain Difference (OFF)	Mode OFF, Input signal of 1kHz, 1.4 V _{p-p} R _{in} → R _{out} , L _{in} → L _{out}	-1	0	1	dB
G _{MOV}	In-phase Gain (Movie)	Movie mode, Effect Ctrl = -6dB Input signal of 1kHz, 1.4 V _{p-p} R _{in} → R _{out} , L _{in} → L _{out}		8		dB
D _{G_{MOV}}	LR In-phase Gain Difference (Movie)	Movie mode, Effect Ctrl = -6dB Input signal of 1kHz, 1.4 V _{p-p} (R _{in} → R _{out}) - (L _{in} → L _{out})		0		dB
G _{MUS}	In-phase Gain (Music)	Music mode, Effect Ctrl = -6dB Input signal of 1kHz, 1.4 V _{p-p} (R _{in} → R _{out}), (L _{in} → L _{out})		7		dB
D _{G_{MUS}}	LR In-phase Gain Difference (Music)	Music mode, Effect Ctrl = -6dB Input signal of 1kHz, 1.4 V _{p-p} (R _{in} → R _{out}) - (L _{in} → L _{out})		0		dB
L _{MON1}	Simulated L Output 1	Simulated Mode, Effect Ctrl = -6dB Input signal of 250Hz, 1.4 V _{p-p} , R _{in} and L _{in} → L _{out}		4.5		dB
L _{MON2}	Simulated L Output 2	Simulated Mode, Effect Ctrl = -6dB Input signal of 1kHz, 1.4 V _{p-p} , R _{in} and L _{in} → L _{out}		-4.0		dB
L _{MON3}	Simulated L Output 3	Simulated Mode, Effect Ctrl = -6dB Input signal of 3.6kHz, 1.4 V _{p-p} , R _{in} and L _{in} → L _{out}		7.0		dB
R _{MON1}	Simulated R Output 1	Simulated Mode, Effect Ctrl = -6dB Input signal of 250Hz, 1.4 V _{p-p} , R _{in} and L _{in} → R _{out}		-4.5		dB
R _{MON2}	Simulated R Output 2	Simulated Mode, Effect Ctrl = -6dB Input signal of 1kHz, 1.4 V _{p-p} , R _{in} and L _{in} → R _{out}		3.8		dB
R _{MON3}	Simulated R Output 3	Simulated Mode, Effect Ctrl = -6dB Input signal of 3.6kHz, 1.4 V _{p-p} , R _{in} and L _{in} → R _{out}		-20		dB
R _{LP1}	Low Pass Filter Resistance		7	10	13	K Ω
R _{HPI}	High Pass Filter Resistance		42	60	78	K Ω
R _{LPF}	LP Pin Impedance		7	10	13	K Ω

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SPEAKER & AUX ATTENUATORS						
C_{range}	Control Range			79		dB
S_{STEP}	Step Resolution		-0.5	1	1.5	dB
E_A	Attenuation set error	$A_v = 0$ to -20dB	-1.5	0	1.5	dB
		$A_v = -20$ to -79dB	-3	0	2	dB
V_{DC}	DC Steps	adjacent att. steps	-3	0	3	mV
A_{MUTE}	Output Mute Condition		+70	100		dB
R_{VEA}	Input Impedance		21	30	39	K Ω
AUDIO OUTPUTS						
$N_{O(OFF)}$	Output Noise (OFF)	Output Mute, Flat $B_W = 20\text{Hz to } 20\text{KHz}$		4 5		μVrms μVrms
$N_{O(MOV)}$	Output Noise (Movie)	Mode = Movie , $B_W = 20\text{Hz to } 20\text{KHz}$		30		μVrms
$N_{O(MUS)}$	Output Noise (Music)	Mode = Music , $B_W = 20\text{Hz to } 20\text{KHz}$		30		mVrms
$N_{O(MON)}$	Output Noise (Simulated)	Mode = Simulated, $B_W = 20\text{Hz to } 20\text{KHz}$		30		μVrms
d	Distorsion	$A_v = 0$; $V_{in} = 1\text{Vrms}$		0.01	0.1	%
S_C	Channel Separation		70	90		dB
V_{OCL}	Clipping Level	$d = 0.3\%$	2	2.5		Vrms
R_{OUT}	Output Resistance		10	30	50	Ω
V_{OUT}	DC Voltage Level			3.8		V
MONITOR OUTPUTS						
d	Distorsion	$A_v = 0$; $V_{in} = 1\text{Vrms}$		0.01	0.1	%
S_C	Channel Separation		70	90		dB
V_{OCL}	Clipping Level	$d = 0.3\%$	2	2.5		Vrms
R_{OUT}	Output Resistance		10	20	50	Ω
V_{OUT}	DC Voltage Level			4.5		V
BUS INPUTS						
V_{IL}	Input Low Voltage				1	V
V_{IH}	Input High Voltage		3			V
I_{IN}	Input Current		-5		+5	μA
V_O	Output Voltage SDA Acknowledge	$I_O = 1.6\text{mA}$			0.4	V

I²C BUS INTERFACE

Data transmission from microprocessor to the TDA7429 and viceversa takes place through the 2 wires I²C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected).

Data Validity

As shown in fig. 3, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

Start and Stop Conditions

As shown in fig.4 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

Byte Format

Every byte transferred on the SDA line must contain 8 bits. Each byte must be followed by an ac-

knowledge bit. The MSB is transferred first.

Acknowledge

The master (μ P) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 5). The peripheral (audioprocessor) that acknowledges has to pull-down (LOW) the SDA line during this clock pulse.

The audioprocessor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

Transmission without Acknowledge

Avoiding to detect the acknowledge of the audioprocessor, the μ P can use a simpler transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data.

This approach of course is less protected from misworking.

Figure 3: Data Validity on the I²C BUS

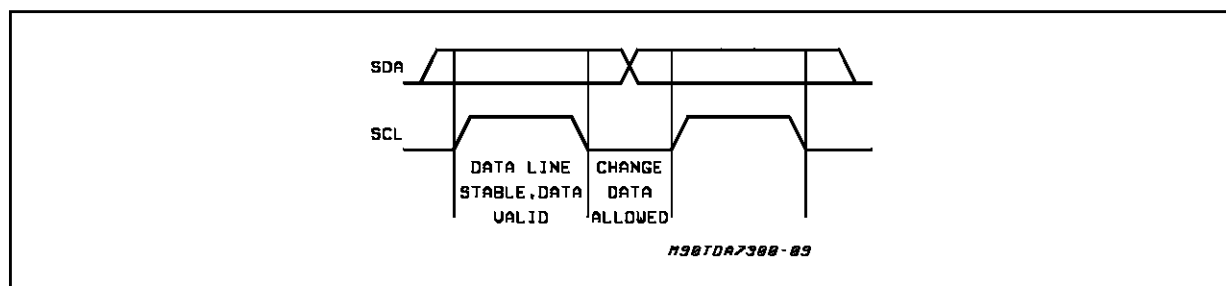


Figure 4: Timing Diagram of I²C BUS

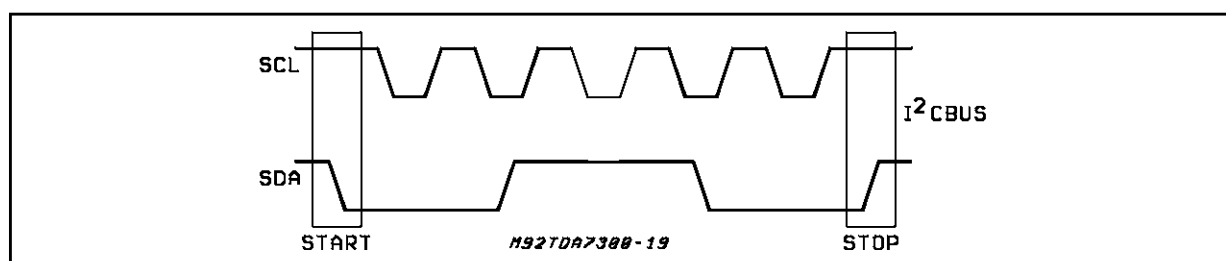
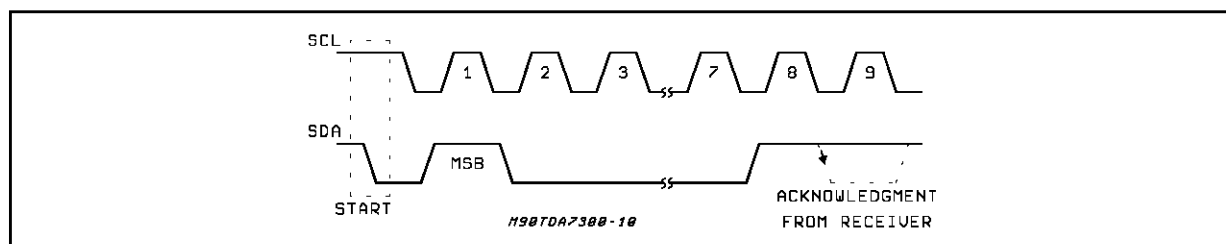


Figure 5: Acknowledge on the I²C BUS



TDA7429

SOFTWARE SPECIFICATION

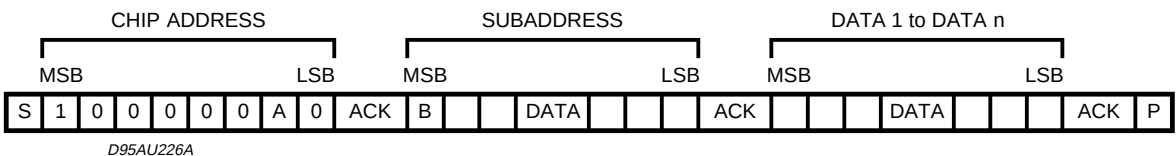
Interface Protocol

The interface protocol comprises:

- A start condition (S)
- A chip address byte, containing the TDA7429

address

- A subaddress bytes
- A sequence of data (N byte + acknowledge)
- A stop condition (P)



ACK = Acknowledge

S = Start

P = Stop

A = Address

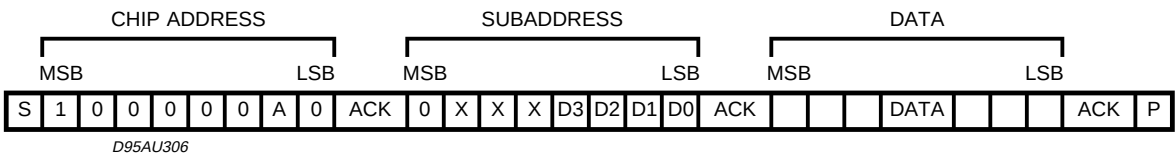
B = Auto Increment

EXAMPLES

No Incremental Bus

The TDA7429 receives a start condition, the cor-

rect chip address, a subaddress with the MSB = 0 (no incremental bus), N-datas (all these datas concern the subaddress selected), a stop condition.

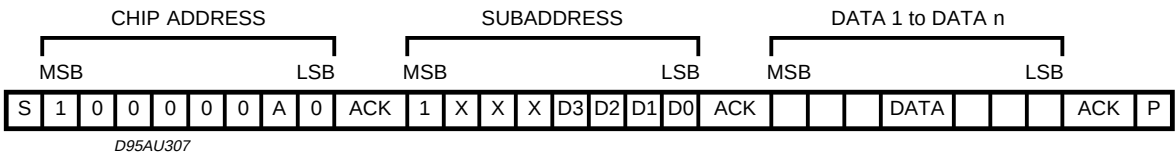


Incremental Bus

The TDA7429 receive s a start condition, the correct chip address, a subaddress with the MSB = 1 (incremental bus): now it is in a loop condition with an autoincrease of the subaddress whereas

SUBADDRESS from "1XXX1010" to "1XXX1111" of DATA are ignored.

The DATA 1 concern the subaddress sent, and the DATA 2 concern the subaddress sent plus one in the loop etc, and at the end it receives the stop condition.



DATA BYTES

Address = 80(HEX)

FUNCTION SELECTION:

The first byte (subaddress)

MSB							LSB	SUBADDRESS
D7	D6	D5	D4	D3	D2	D1	D0	
B	X	X	X	0	0	0	0	INPUT ATTENUATION
B	X	X	X	0	0	0	1	SURROUND & OUT & EFFECT CONTROL
B	X	X	X	0	0	1	0	PHASE RESISTOR
B	X	X	X	0	0	1	1	BASS & NATURAL BASE
B	X	X	X	0	1	0	0	MIDDLE & TREBLE
B	X	X	X	0	1	0	1	SPEAKER ATTENUATION "L"
B	X	X	X	0	1	1	0	SPEAKER ATTENUATION "R"
B	X	X	X	0	1	1	1	AUX ATTENUATION "L"
B	X	X	X	1	0	0	0	AUX ATTENUATION "R"
B	X	X	X	1	0	0	1	INPUT MULTIPLEXER, & AUX OUT

B = 1 incremental bus; active

B = 0 no incremental bus;

X = indifferent 0,1

INPUT ATTENUATION SELECTION

MSB							LSB	INPUT ATTENUATION
D7	D6	D5	D4	D3	D2	D1	D0	0.5 dB STEPS
					0	0	0	0
					0	0	1	-0.5
					0	1	0	-1
					0	1	1	-1.5
					1	0	0	-2
					1	0	1	-2.5
					1	1	0	-3
					1	1	1	-3.5
								4 dB STEPS
		0	0	0				0
		0	0	1				-4
		0	1	0				-8
		0	1	1				-12
		1	0	0				-16
		1	0	1				-20
		1	1	0				-24
		1	1	1				-28

INPUT ATTENUATION = 0 ~ -31.5dB

D7	D6	D5	D4	D3	D2	D1	D0	REAR SWITCH
	0							REARIN, REAROUT PIN ACTIVE
	1							NO REARIN, REAROUT PIN

SURROUND SELECTION

MSB							LSB	
D7	D6	D5	D4	D3	D2	D1	D0	SURROUND MODE
						0	0	SIMULATED
						0	1	MUSIC
						1	0	OFF
						1	1	MOVIE
								OUT
					0			VAR
					1			FIX
								EFFECT CONTROL
	0	0	0	0				-6
	0	0	0	1				-7
	0	0	1	0				-8
	0	0	1	1				-9
	0	1	0	0				-10
	0	1	0	1				-11
	0	1	1	0				-12
	0	1	1	1				-13
	1	0	0	0				-14
	1	0	0	1				-15
	1	0	1	0				-16
	1	0	1	1				-17
	1	1	0	0				-18
	1	1	0	1				-19
	1	1	1	0				-20
	1	1	1	1				-21
PHASE RESISTOR SELECTION								
MSB							LSB	SURROUND PHASE RESISTOR
D7	D6	D5	D4	D3	D2	D1	D0	PHASE SHIFT 1 (K Ω)
						0	0	12
						0	1	14
						1	0	18
						1	1	37
								PHASE SHIFT 2 (KΩ)
				0	0			6
				0	1			7
				1	0			8
				1	1			18
								PHASE SHIFT 3 (KΩ)
		0	0					12
		0	1					14
		1	0					18
		1	1					39
								PHASE SHIFT 4 (KΩ)
0	0							12
0	1							14
1	0							18
1	1							39

BASS SELECTION								
MSB							LSB	BASS
D7	D6	D5	D4	D3	D2	D1	D0	2 dB STEPS
				0	0	0	0	-14
				0	0	0	1	-12
				0	0	1	0	-10
				0	0	1	1	-8
				0	1	0	0	-6
				0	1	0	1	-4
				0	1	1	0	-2
				0	1	1	1	0
				1	1	1	1	0
				1	1	1	0	2
				1	1	0	1	4
				1	1	0	0	6
				1	0	1	1	8
				1	0	1	0	10
				1	0	0	1	12
				1	0	0	0	14
SPEAKER/AUX ATT. R & L SELECTION								
MSB							LSB	SPEAKER/AUX ATT
D7	D6	D5	D4	D3	D2	D1	D0	1 dB STEPS
					0	0	0	0
					0	0	1	-1
					0	1	0	-2
					0	1	1	-3
					1	0	0	-4
					1	0	1	-5
					1	1	0	-6
					1	1	1	-7
								8 dB STEPS
	0	0	0	0				0
	0	0	0	1				-8
	0	0	1	0				-16
	0	0	1	1				-24
	0	1	0	0				-32
	0	1	0	1				-40
	0	1	1	0				-48
	0	1	1	1				-56
	1	0	0	0				-64
	1	0	0	1				-72
								MUTE
	1	0	1	X				
	1	1	X	X				

X = INDIFFERENT 0,1

SPEAKER/AUX ATTENUATION = 0dB ~ -79dB

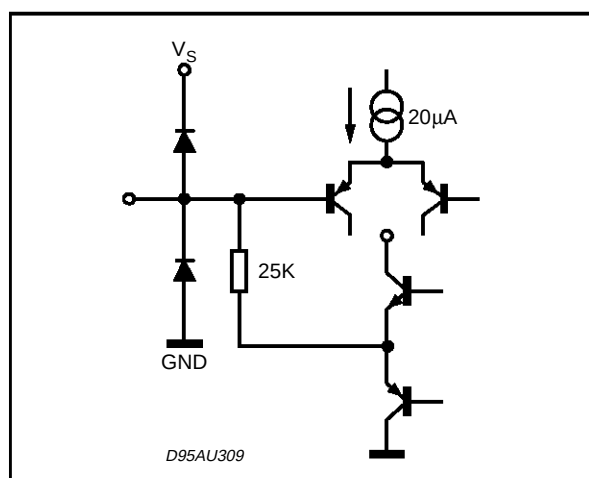
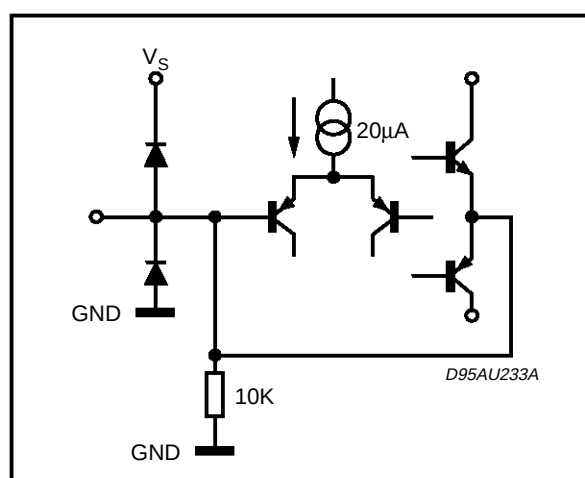
MIDDLE & TREBLE SELECTION								
MSB							LSB	MIDDLE
D7	D6	D5	D4	D3	D2	D1	D0	2 dB STEPS
				0	0	0	0	-14
				0	0	0	1	-12
				0	0	1	0	-10
				0	0	1	1	-8
				0	1	0	0	-6
				0	1	0	1	-4
				0	1	1	0	-2
				0	1	1	1	0
				1	1	1	1	0
				1	1	1	0	2
				1	1	0	1	4
				1	1	0	0	6
				1	0	1	1	8
				1	0	1	0	10
				1	0	0	1	12
				1	0	0	0	14
								TREBLE
								2 dB STEPS
0	0	0	0					-14
0	0	0	1					-12
0	0	1	0					-10
0	0	1	1					-8
0	1	0	0					-6
0	1	0	1					-4
0	1	1	0					-2
0	1	1	1					0
1	1	1	1					0
1	1	1	0					2
1	1	0	1					4
1	1	0	0					6
1	0	1	1					8
1	0	1	0					10
1	0	0	1					12
1	0	0	0					14

INPUT/RECOUL L & R SELECTION

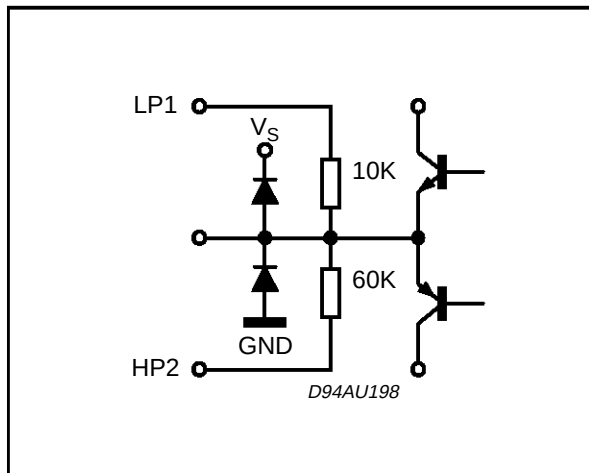
MSB							LSB	INPUT MULTIPLEXER
D7	D6	D5	D4	D3	D2	D1	D0	
					0	0		IN2
					0	1		IN3
					1	0		IN4
					1	1		IN1
								AUX OUT "L"
			0	0				VER 1 (3BAND)
			0	1				VER 2 (SURR)
			1	0				VER 3 (REAR)
			1	1				FIX
								AUX OUT "R"
	0	0						VER 1 (3BAND)
	0	1						VER 2 (SURR)
	1	0						VER 3 (REAR)
	1	1						FIX

POWER ON RESET

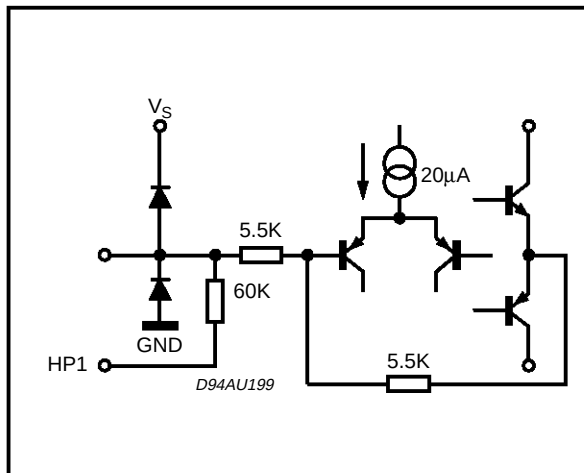
BASS & MIDDLE	2dB
TREBLE	0dB
SURROUND & OUT CONTROL+ EFFECT CONTROL	OFF + FIX + MAX ATTENUATION
SPEAKER/AUX ATTENUATION L & R	MUTE
INPUT ATTENUATION + REAR SWITCH	MAX ATTENUATION + ON
NATURAL BASE	OFF
INPUT	IN1

PIN: TREBLE-L, TREBLE-R**PIN: VOUT REF**

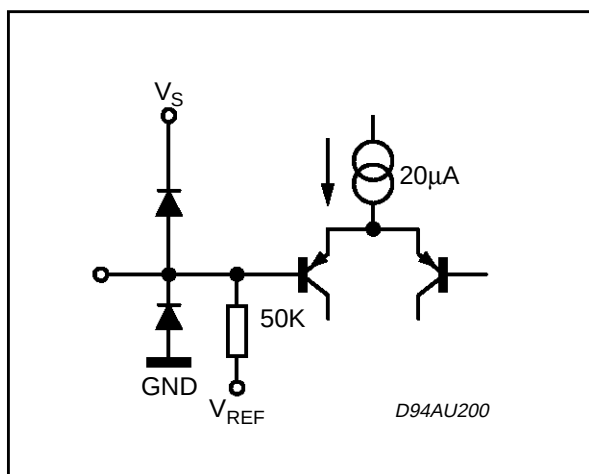
PIN: HP1



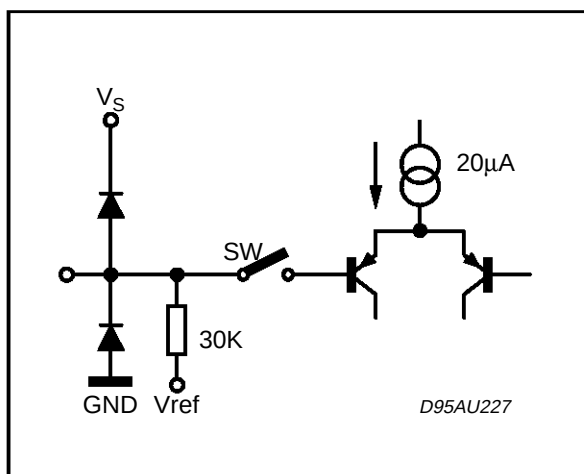
PIN: HP2



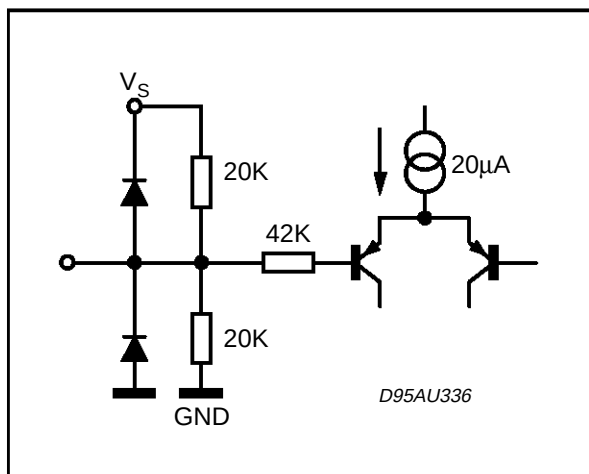
PIN: L-IN, R-IN, L-IN2, R-IN2, L-IN3, R-IN3, L-IN4, R-IN4,



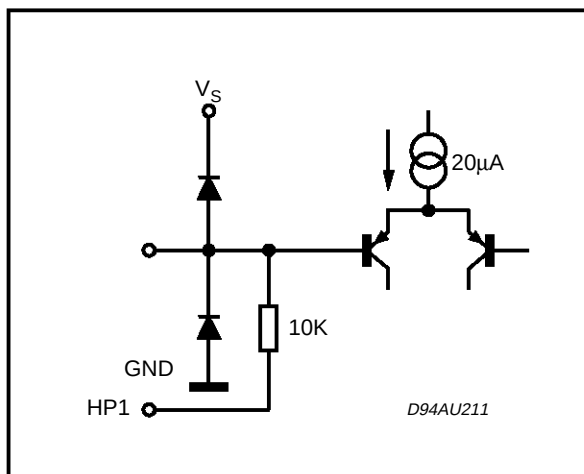
PIN: VAR-L, VAR-R,



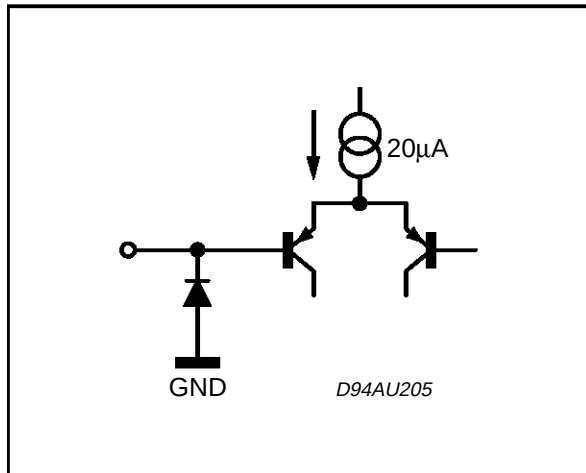
PIN: CREF



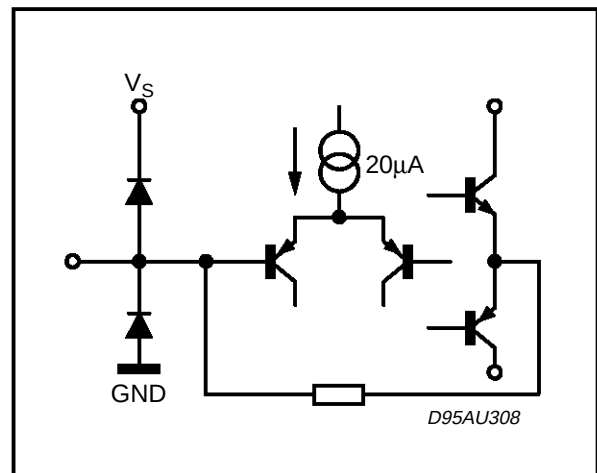
PIN: LP1



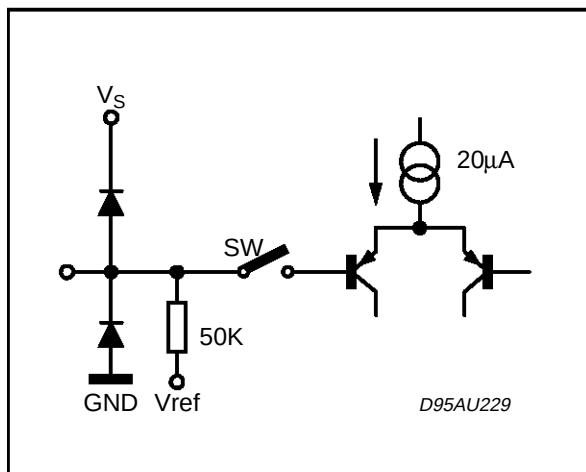
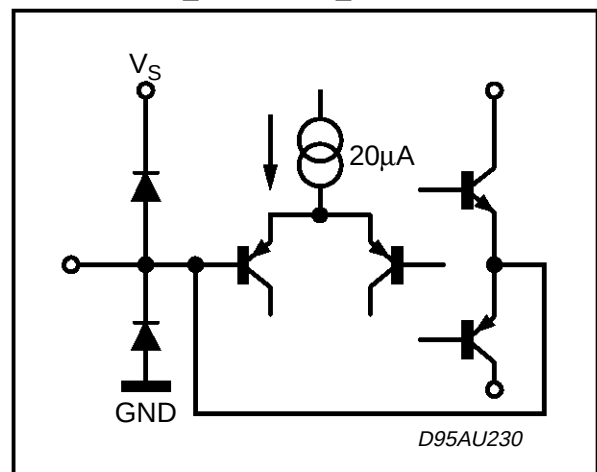
PIN: SCL, SDA



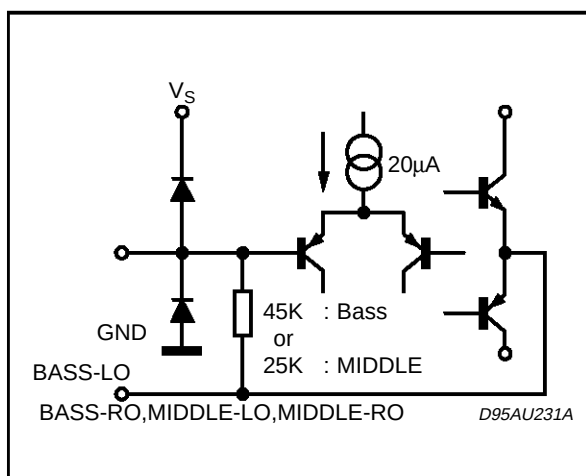
PIN: PS1, PS2, PS3, PS4, LP



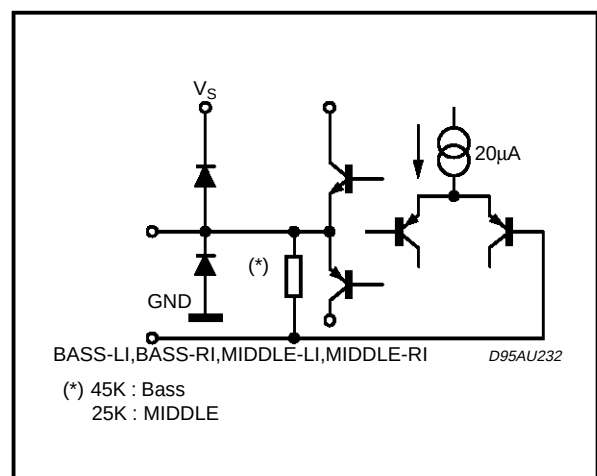
PIN: REARIN

PIN: L-OUT, R-OUT, MONITOR-L, MONITOR-R
REAROUT, BASSO-L, BASSO-R,
AUXOUT_L, AUXOUT_R

PIN: BASS-LI, BASS-RI, MIDDLE-LI, MIDDLE-RI,

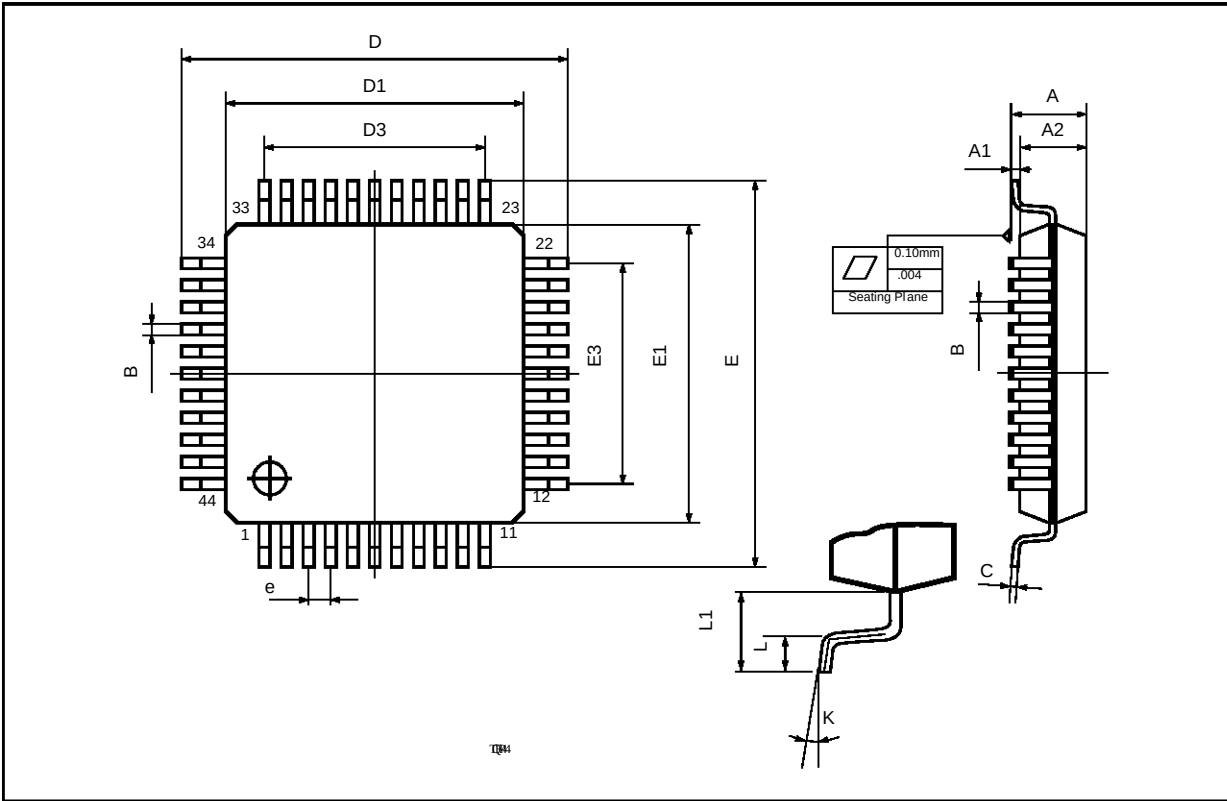


PIN: BASS-LO, BASS-RO, MIDDLE-LO, MIDDLE-RO,



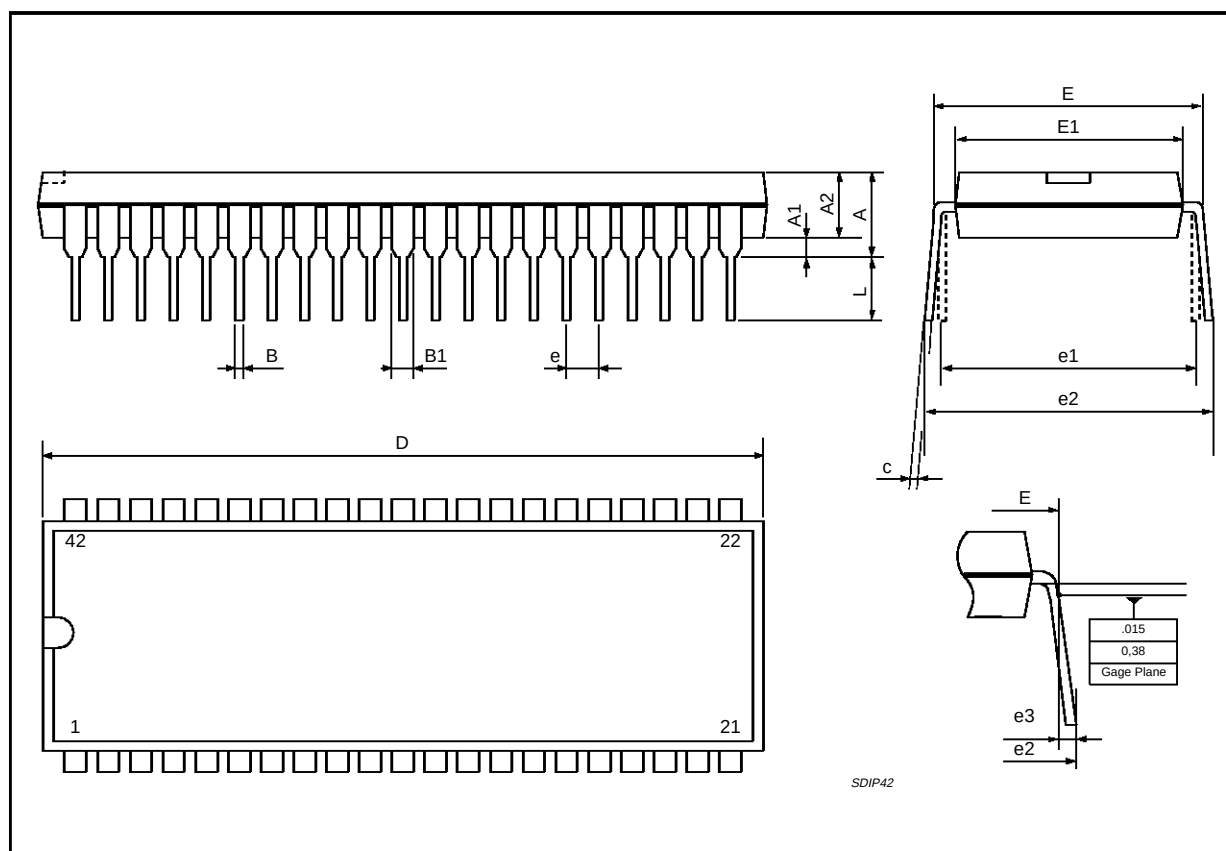
TQFP44 (10 x 10) PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.014	0.018
C	0.09		0.20	0.004		0.008
D		12.00			0.472	
D1		10.00			0.394	
D3		8.00			0.315	
e		0.80			0.031	
E		12.00			0.472	
E1		10.00			0.394	
E3		8.00			0.315	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0°(min.), 3.5°(typ.), 7°(max.)					



SDIP42 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5.08			0.20
A1	0.51			0.020		
A2	3.05	3.81	4.57	0.120	0.150	0.180
B	0.38	0.46	0.56	0.0149	0.0181	0.0220
B1	0.89	1.02	1.14	0.035	0.040	0.045
c	0.23	0.25	0.38	0.0090	0.0098	0.0150
D	36.58	36.83	37.08	1.440	1.450	1.460
E	15.24		16.00	0.60		0.629
E1	12.70	13.72	14.48	0.50	0.540	0.570
e		1.778			0.070	
e1		15.24			0.60	
e2			18.54			0.730
e3			1.52			0.060
L	2.54	3.30	3.56	0.10	0.130	0.140



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