

TV-Stereo-Surround Sound Interface IC

TDA 6811

Preliminary Data

Bipolar IC

Features

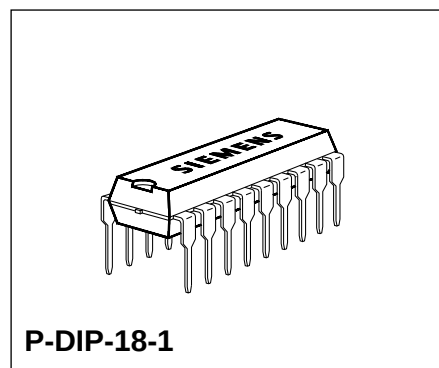
The TDA 6811 contains I²C Bus controlled functions, which are required as a supplement to a Dolby surround sound audio system. The circuit is divided into two functional blocks:

High-Quality Sound Processing

- Fine-step stereo level control for adjustment of the Dolby® decoder
- Volume control for the rear channel

Control Circuit

- I²C Bus interface
- Control of AF sound processing
- Switch outputs (seven)



Type	Ordering Code	Package
TDA 6811	Q67000-A5145	P-DIP-18-1

Dolby® is a registered trademark of Dolby Laboratories Corporation.
Purchase of Siemens I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips.

Signal Circuit

The integrated circuit contains the components required for extending a conventional stereo sound system from a two-channel arrangement to a three-channel Dolby surround system with Dolby decoder.

The first component is a fine-step two-channel AF-level controller. It is used for adjusting the Dolby decoder. Its operating range is ± 3 dB with 0.2 dB steps. The left and right channels can be adjusted separately.

The second component, a mono volume control with a maximum gain of 10 dB, is used for the rear channel generated in the Dolby decoder. 56 steps of 1.25 dB each provide a control range of 68.75 dB.

A total of seven switch outputs are provided for controlling the Dolby decoder via the I²C Bus.

Control Circuit

An I²C Bus interface with listen/talk action controls all functions. The currently valid data are stored in a latch block.

The telegram structure is as follows:

Start condition – chip address – any number of data bytes – stop condition.

The following conditions apply to data bytes:

The actual data byte (containing the data information) must **always** be preceded by a subaddress byte.

Various subaddresses can be accessed within a message (ie. without new start condition).

Chip Address

	MSB	.	.	.	.	.	.	LSB
	1	0	0	1	0	0	1	0

Subaddress Bytes

	MSB	.	.	.	.	.	.	LSB
Fine adjust, left	X	X	X	X	0	0	0	0
Fine adjust, right	X	X	X	X	0	0	0	1
Volume control	X	X	X	X	0	0	1	0
Switch outputs	X	X	X	X	0	0	1	1

a) Volume Control

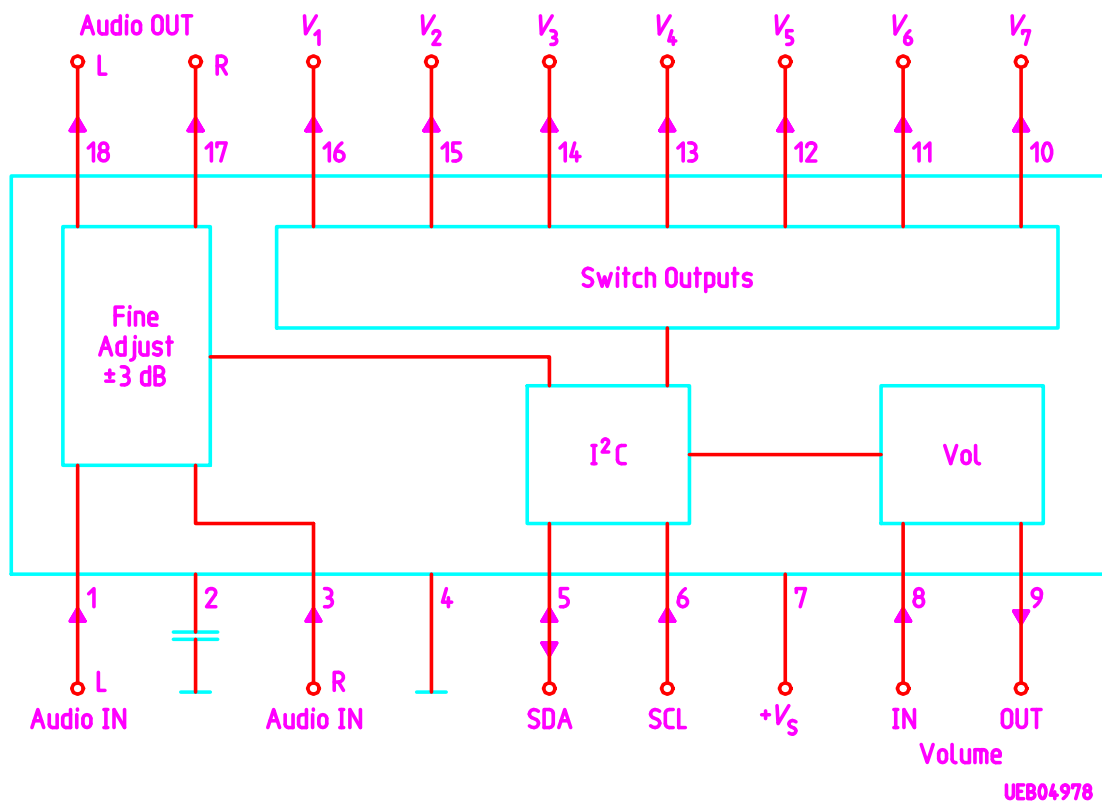
	MSB	.	.	.	.	.	.	LSB
Maximal volume	X	X	1	1	1	1	1	1
Max – 1	X	X	1	1	1	1	1	0
Max – 15	X	X	1	1	0	0	0	0
Max – 55	X	X	0	0	1	0	0	0
MUTE	X	X	0	0	0	X	X	X
Power ON	0	0	0	0	0	0	0	1

b) Fine Adjust Left/Right

	MSB	.	.	.	.	.	.	LSB
Maximal gain	X	X	X	1	1	1	1	1
Max – 1	X	X	X	1	1	1	1	0
Gain 0 dB	X	X	X	1	0	0	0	0
Minimum gain	X	X	X	0	0	0	0	1
Minimum gain	X	X	X	0	0	0	0	X
Power ON	X	X	X	0	0	0	0	1

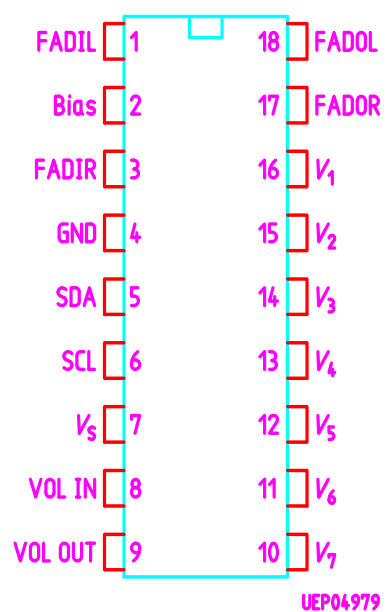
c) Switch Byte

	MSB	.	.	.	.	.	.	LSB
	P7	P6	P5	P4	P3	P2	P1	X
P1 = 0	Port 1 (open collector) low (low-impedance); power ON							
P1 = 1	Port 1 high (high-impedance)							
P2 = 0	Port 2 (open collector) low (low-impedance); power ON							
P2 = 1	Port 2 high (high-impedance)							
P3 = 0	Port 3 (open collector) low (low-impedance); power ON							
P3 = 1	Port 3 high (high-impedance)							
P4 = 0	Port 4 (open collector) low (low-impedance); power ON							
P4 = 1	Port 4 high (high-impedance)							
P5 = 0	Port 5 (open collector) low (low-impedance); power ON							
P5 = 1	Port 5 high (high-impedance)							
P6 = 0	Port 6 (open collector) low (low-impedance); power ON							
P6 = 1	Port 6 high (high-impedance)							
P7 = 0	Port 7 (open collector) low (low-impedance); power ON							
P7 = 1	Port 7 high (high-impedance)							



Block Diagram

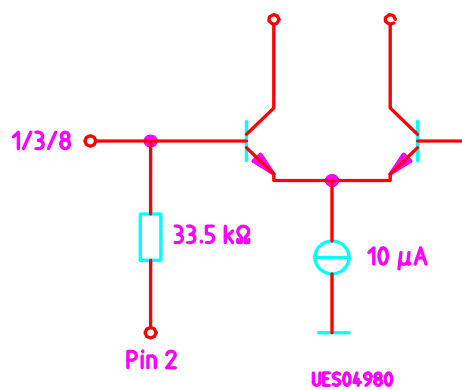
Pin Configuration (top view)



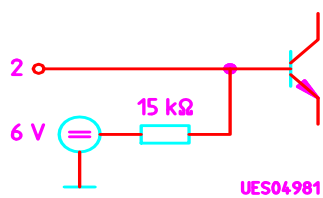
Pin Functions

Pin No.	Symbol	Function
1	FADIL	Fine adjust input left
2	Bias	Bias for AF operation
3	FADIR	Fine adjust input right
4	GND	Ground
5	SDA	I ² C Bus SDA
6	SCL	I ² C Bus SCL
7	V_s	Supply voltage + V_s
8	VOL IN	Volume control input
9	VOL OUT	Volume control output
10	V_7	Switch output 7
11	V_6	Switch output 6
12	V_5	Switch output 5
13	V_4	Switch output 4
14	V_3	Switch output 3
15	V_2	Switch output 2
16	V_1	Switch output 1
17	FADOR	Fine adjust output right
18	FADOL	Fine adjust output left

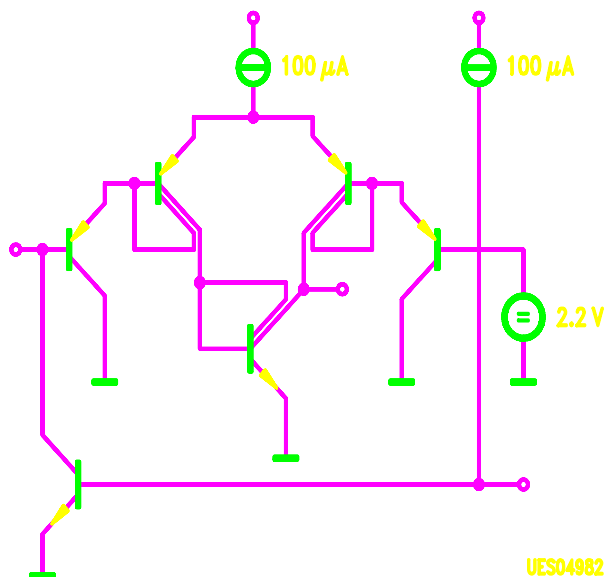
Pin Description



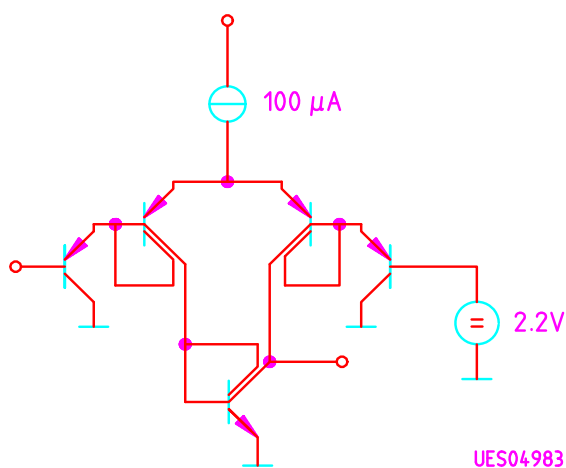
AF Inputs (Pin 1/3/8)



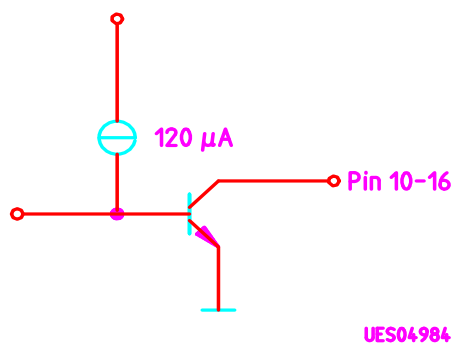
Bias for AF Operation Point (Pin 2)



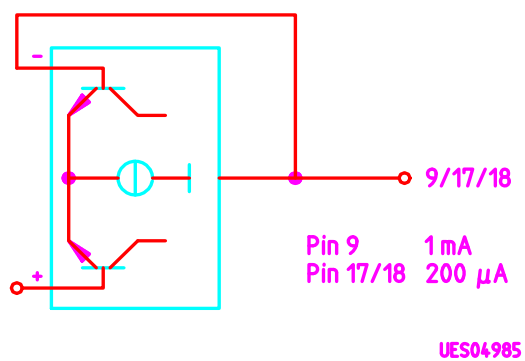
I²C Bus SDA (Pin 5)



I²C Bus SCL (Pin 6)



Port Outputs (Pin 10-16)



AF Outputs (Pin 9/17/18)

Absolute Maximum Ratings $T_A = 0$ to 70°C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_7	0	14	V	
Max. DC voltage	V_1	0	V_7	V	
Max. DC voltage	V_2	0	V_7	V	
Max. DC voltage	V_6	0	V_7	V	
Max. DC voltage	V_8	0	V_7	V	
Max. DC current	I_5	0	3	mA	
Max. DC current	I_9	0	2	mA	
Max. DC current	I_{10}	0	3	mA	
Max. DC current	I_{11}	0	3	mA	
Max. DC current	I_{12}	0	3	mA	
Max. DC current	I_{13}	0	3	mA	
Max. DC current	I_{14}	0	3	mA	
Max. DC current	I_{15}	0	3	mA	
Max. DC current	I_{16}	0	3	mA	
Max. DC current	I_{17}	0	2	mA	
Max. DC current	I_{18}	0	2	mA	
ESD voltage	V_{ESD}	– 2	2	kV	HBM ($R = 1.5\text{ k}\Omega$, $C = 100\text{ pF}$)
Junction temperature	T_j		150	$^\circ\text{C}$	
Storage temperature	T_{stg}	– 40	125	$^\circ\text{C}$	
Thermal resistance (system-air)	$R_{\text{th SA}}$		68	K/W	

Operating Range

Supply voltage	V_S	10	13.2	V
Ambient temperature	T_A	0	70	$^\circ\text{C}$
Input frequency range	f_i	0.01	20	kHz

AC/DC Characteristics

$V_S = 12\text{ V}$; $T_A = 25\text{ °C}$, in accordance with test circuit

I²C Bus preset: start-92-00, 10 – 01, 0 – 02, 3F – 03, FE

Adr. Fine adjust lin., Vol. max, Ports high

The basic setting for each point in the specification is always preset; only settings which are deviate from this, are given in the test conditions. Detail in *italics* only provide explanation of the hexadecimal code and which switch bits on the setbytes are stated.

AF reference level 0 dB = 300 mV, if not different defined. f_i 20 Hz – 20 kHz

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current consumption	I_7		17		mA	

Signal Section

Volume control						
Max. gain	G_{9-8}		10		dB	
Min. gain	G_{9-8}		– 58.75	55	dB	02, 10, Vol 8
Volume step width	ΔG_9		1.25	2.5	dB	02, X – 02, (X ± 1) <i>Vol X – Vol (X ± 1)</i>
Max. input voltage	V_8	2			Vrms	$THD_9 < 1\%$
Max. output voltage	V_9	2.2			Vrms	$THD_9 < 1\%$; 02, X; any setting
Distortion factor	THD_9		0.01	0.05	%	$V_8 = 300\text{ Vrms}$
Unweighted signal/ noise ratio	$a_{S/N9}$	90	97		dB	$V_8 = 600\text{ mVrms}$
Noise voltage	V_{N9}		15	30	μV	02, 10, <i>Vol 8</i>
Attenuation MUTE	a_{9-8}	80			dB	02, 00, <i>MUTE</i>
DC jump Δ 1 bit	ΔV_9			± 6	mV	02, X – 02, (X ± 1) <i>Vol X – Vol (X ± 1)</i>
Fine adjustment						
Max. gain	G_{18-1}	2.5	3	3.5	dB	00, 1 F, <i>Adj, 31</i>
Max. gain	G_{17-3}	2.5	3	3.5	dB	01, 1 F, <i>Adj, 31</i>
Max. gain	G_{18-1}	– 3.5	– 3	– 2.5	dB	00, 01, <i>Adj, 1</i>
Max. gain	G_{17-3}	– 3.5	– 3	– 2.5	dB	01, 01, <i>Adj, 1</i>
Adjust step width	ΔG_{18}			0.2	dB	
Adjust step width	ΔG_{17}			0.2	dB	00, X – 00, (X ± 1) <i>Adj, X – Adj, (X ± 1)</i> 01, X – 01, (X ± 1) <i>Adj, X – Adj, (X ± 1)</i>

AC/DC Characteristics (cont'd)

$V_S = 12\text{ V}$; $T_A = 25\text{ °C}$, in accordance with test circuit

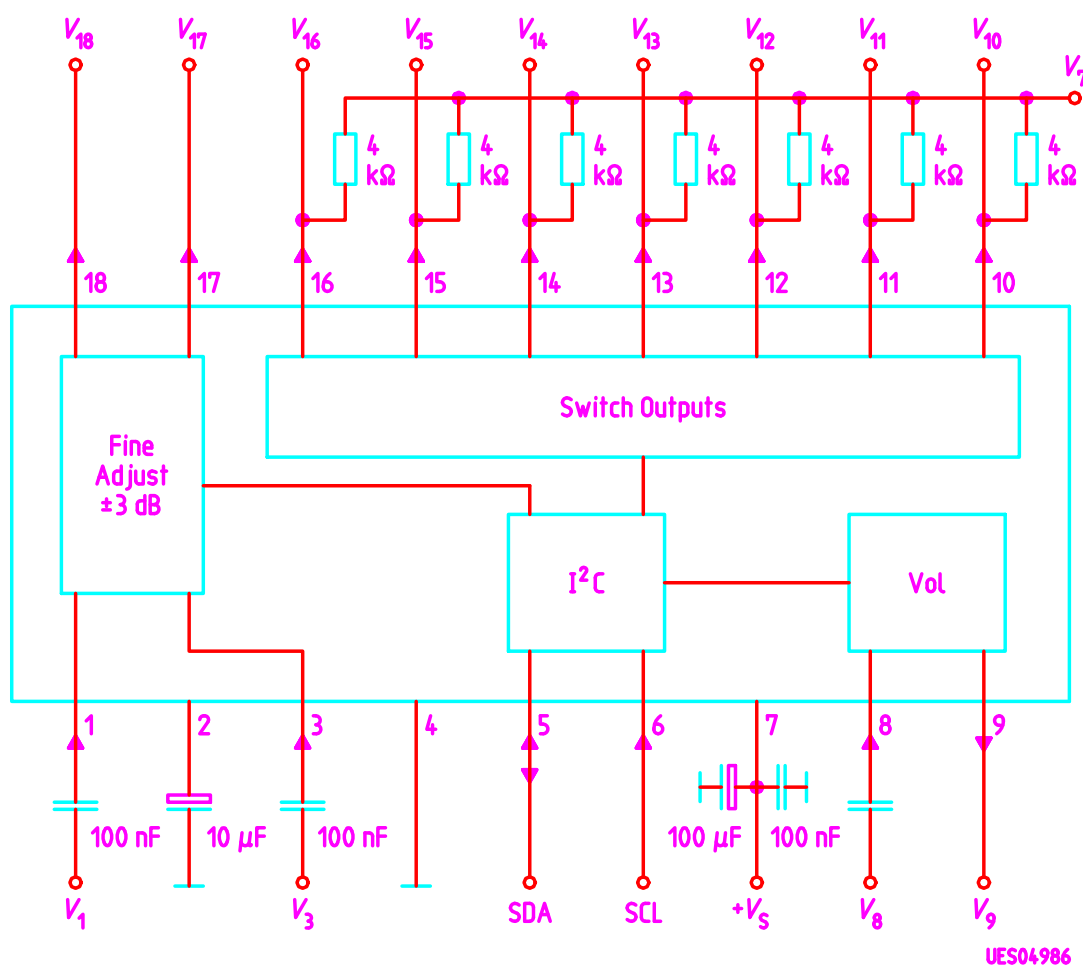
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Max. input voltage	V_1	1.4			Vrms	00, X; any setting
Max. input voltage	V_3	1.4			Vrms	01, X; any setting
Max. output voltage	V_{17}	2			Vrms	01, X; any setting
Max. output voltage	V_{18}	2			Vrms	00, X; any setting
Distortion factor	THD_{17}		0.01	0.05	%	$V_3 = 300\text{ mVrms}$
Distortion factor	THD_{18}		0.01	0.05	%	$V_1 = 300\text{ mVrms}$
Unweighted signal/ noise ratio	$a_{S/N17}$		97		dB	$V_3 = 600\text{ mVrms}$
Unweighted signal/ noise ratio	$a_{S/N18}$		97		dB	$V_1 = 600\text{ mVrms}$
DC jump $\Delta 1$ bit	ΔV_{17}			± 4	mV	01, X – 01, $(X \pm 1)$ $Adj_r X - Adj_r, (X \pm 1)$
DC jump $\Delta 1$ bit	ΔV_{18}			± 4	mV	00, X – 00, $(X \pm 1)$ $Adj_l X - Adj_l, (X \pm 1)$
PSRR	a_{PSRR9}		70		dB	$V_{I\text{ interf.}} = 1\text{ Vrms}$
(Power Supply	a_{PSRR17}		70		dB	$f_{I\text{ interf.}} = 50\text{ Hz} - 20\text{ kHz}$
Ripple Rejection)	a_{PSRR18}		70		dB	$R_G = 220\text{ }\Omega$ unweighted

Design Hints

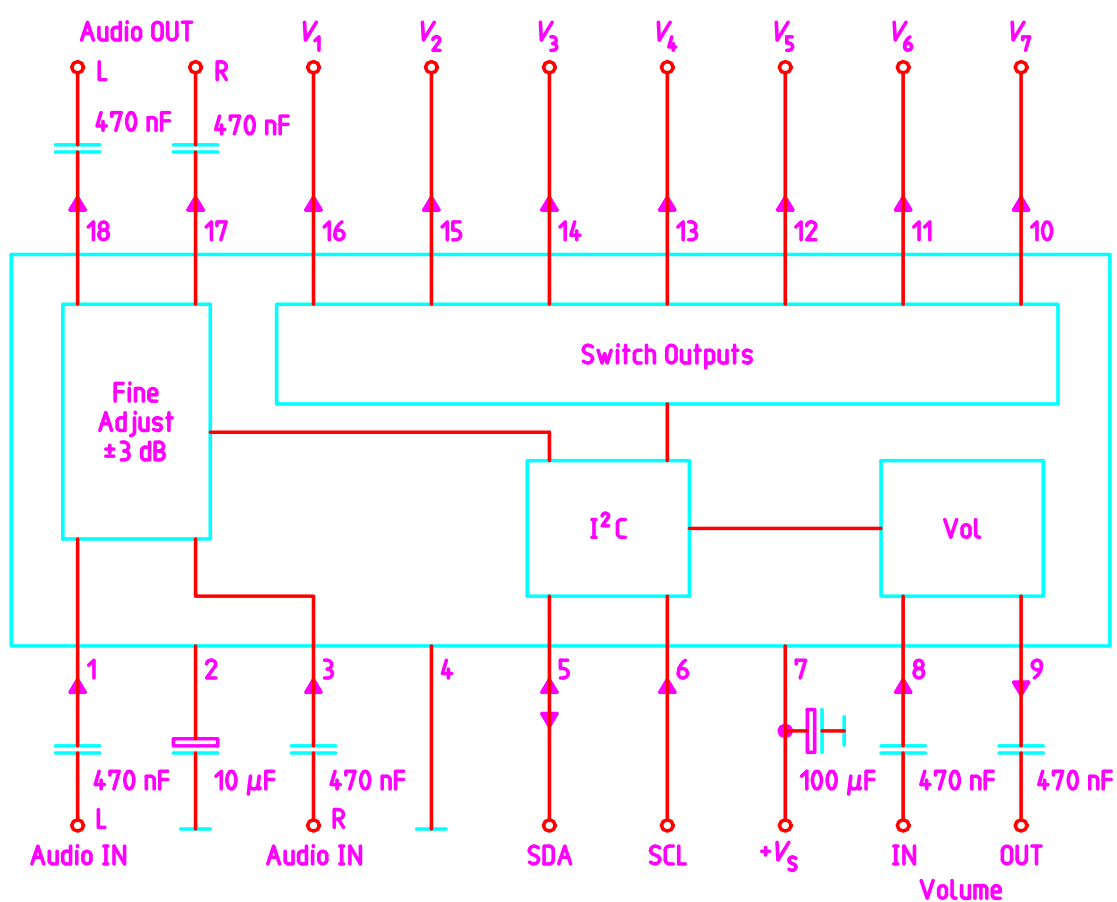
Input resistance	R_1	30			k Ω	
Input resistance	R_3	30			k Ω	
Input resistance	R_8	30			k Ω	
Output resistance	R_9			70	Ω	
Output resistance	R_{17}			70	Ω	
Output resistance	R_{18}			70	Ω	

AC/DC Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
I ² C Bus (SCL, SDA)						
Pulse edges SCL, SDA						
Rise time	t _R			1	μs	
Decay time	t _F			300	ns	
Clock SCL						
Frequency	f _{SCL}	0		100	kHz	
H-pulse width	t _{HIGH}	4			μs	
L-pulse width	t _{LOW}	4			μs	
Start						
Set-up time	t _{SUSTA}	4			μs	
Hold time	t _{HDSTA}	4			μs	
Stop						
Set-up time	t _{SUSTO}	4			μs	
Bus free	t _{BUF}	4			μs	
Data transfer						
Set-up time	t _{SUDAT}	1			μs	
Hold time	t _{HDDAT}	300			ns	
Inputs SCL, SDA						
Input voltage	V _{QH} V _{QL}	3		5.5 1,5	V V	
Input current	I _{QH} I _{QL}			50 100	μA μA	
Output SDA (open collector)						
Output voltage	V _{QH} V _{QL}	5.4		0.4	V V	R _L = 2.5 Ω I _{QL} = 3 mA
Output voltage	V _H			V _S	V	R _L = 4 Ω
Port	V _L			0.4	V	I _{QL} = 3 mA

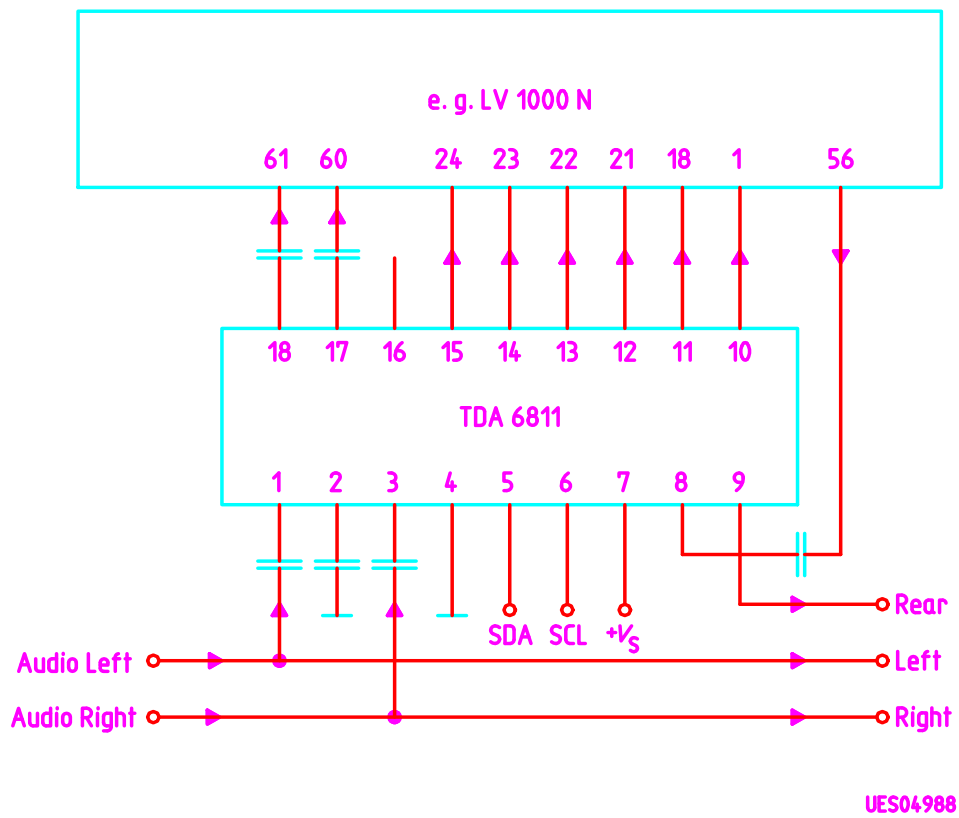


Test Circuit

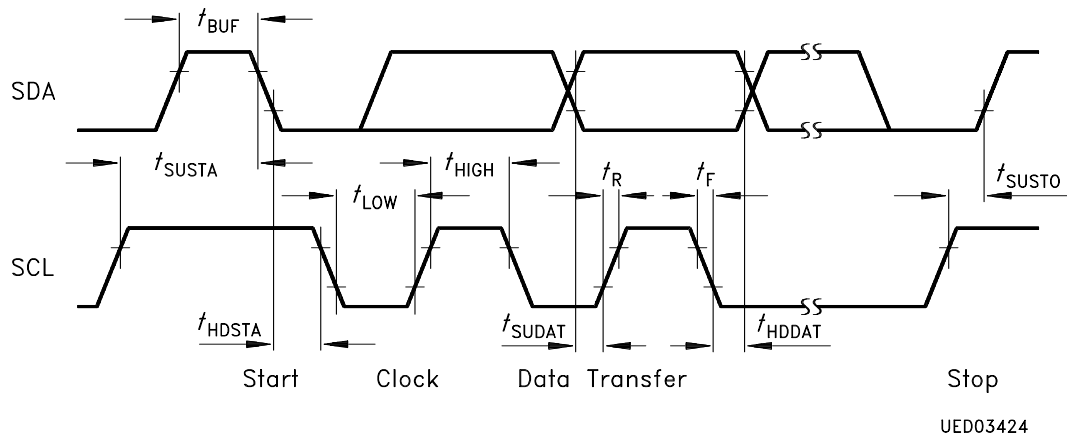


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Application Circuit 1



Application Circuit 2

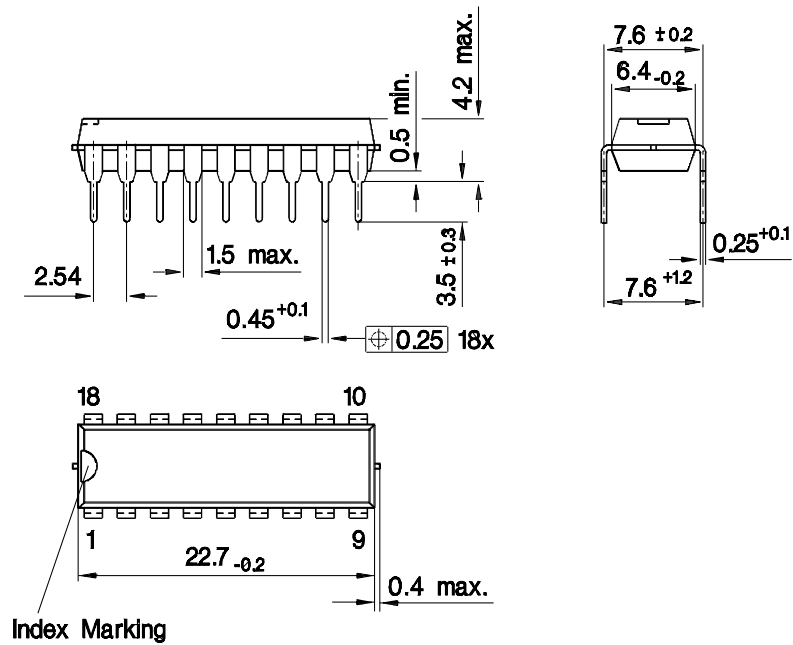


I²C Bus Timing Diagram

t_{SUSTA}	Set-up time (start)
t_{HDSTA}	Hold time (start)
t_{HIGH}	HIGH pulse width (clock)
t_{LOW}	LOW pulse width (clock)
t_{SUDAT}	Set-up time (data transfer)
t_{HDDAT}	Hold time (data transfer)
t_{SUSTO}	Set-up time (stop)
t_{BUF}	Bus free time
t_F	Fall time
t_R	Rise time

All times are referenced to the V_{IH} and V_{IL} values.

Plastic Package, P-DIP-18-1 (Plastic Dual-in-Line Package)



Sorts of Packing

Package outlines for tubes, trays ect. are contained in our Data Book "Package Information"

Dimensions in mm